T1024, T1014
QorIQ T1024, T1014
Datasheet DS1193

FEATURES

- e5500 cores built on Power Architecture® technology,
  - T1024 has two cores and T1014 has a single core
  - Each core has a private 256KB L2 cache
- 256 KB shared L3 CoreNet platform cache (CPC)
- Hierarchical interconnect fabric
  - CoreNet Coherency manager supporting coherent and non-coherent transactions with prioritization and bandwidth allocation amongst CoreNet end-points
  - 150Gbps coherent read bandwidth
- One 32-/64-bit DDR3L/DDR4 SDRAM memory controllers
  - ECC and interleaving support
- Data Path Acceleration Architecture (DPAA) incorporating acceleration for the following functions:
  - Packet parsing, classification, and distribution
  - Queue management for scheduling, packet sequencing, and congestion management
  - Hardware buffer management for buffer allocation and de-allocation
  - Cryptography Acceleration
  - IEEE Std 1588™ support
- Parallel Ethernet interfaces
  - Up to two RGMII interface
- Four SerDes lanes for high-speed peripheral interfaces
  - Three PCI Express 2.0 controllers
  - One Serial ATA (SATA 3Gb/s) controller
  - Up to three SGMII interface supporting 1000 Mbps
  - Up to three SGMII interface supporting 2500Mbps
  - Up to one XFI (10GbE) interface
  - Up to one QSGMII interface
  - Supports 1000Base-KX
  - Supports 10GBase-KR
- Additional peripheral interfaces
  - Two high-speed USB 2.0 controllers with integrated PHY
  - Enhanced secure digital host controller with support for high capacity memory card(SD/eSDHC/eMMC)
  - Enhanced Serial peripheral interface (eSPI)
  - Four I2C controllers
  - Two DUARTs
  - Integrated flash controller supporting NAND and NOR flash
  - Display interface unit (DIU) with 12-bit dual data rate
  - Multicore programmable interrupt controller (MPIC)
- QUICC Engine block
  - 32-bit RISC controller for flexible support of the communications peripherals
  - Serial DMA channel for receive and transmit on all serial channels
  - Two universal communication controllers, supporting TDM, HDLC and UART
- 780 FC-PBGA package, 23 mm x 23 mm

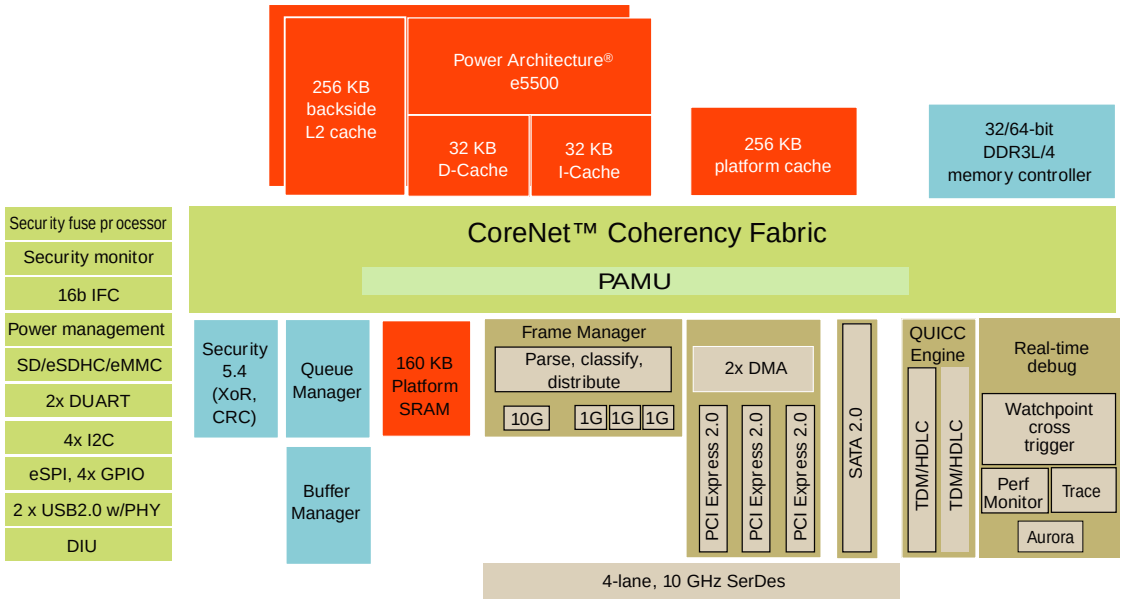
1 OVERVIEW

T1024 QorIQ advanced multicore processor combines two 64-bit ISA Power Architecture® processor cores with high-performance data path acceleration and network and peripheral bus interfaces required for networking, telecom/datacom, wireless infrastructure, and military/aerospace applications.

This chip can be used for combined control, data path, and application layer processing in routers, switches, gateways, and general-purpose embedded computing systems. Its high level of integration offers significant performance benefits compared to multiple discrete devices, while also simplifying board design.

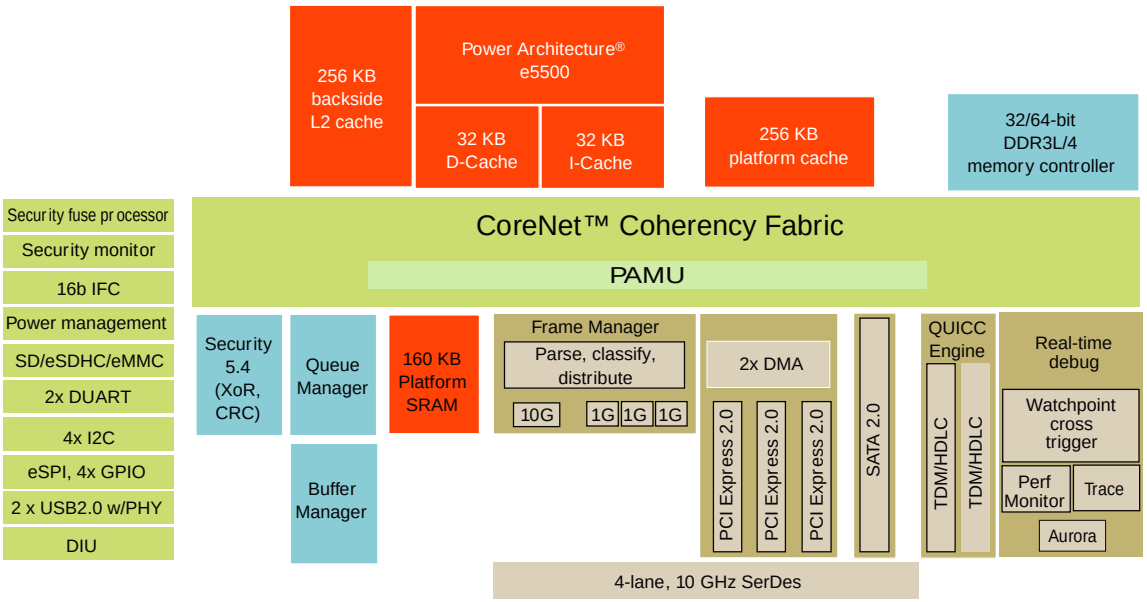
This figure shows the block diagram of the chip.

Figure 1: T1024 Block diagram



This figure shows the block diagram of the chip.

Figure 2: T1014 Block diagram



2 PIN ASSIGNMENTS

2.1 780 ball layout diagrams

This figure shows the complete view of the T1024 ball map diagram. Figure 4, Figure 5, Figure 6, and Figure 7 show quadrant views.

Figure 3: Complete BGA Map for the T1024

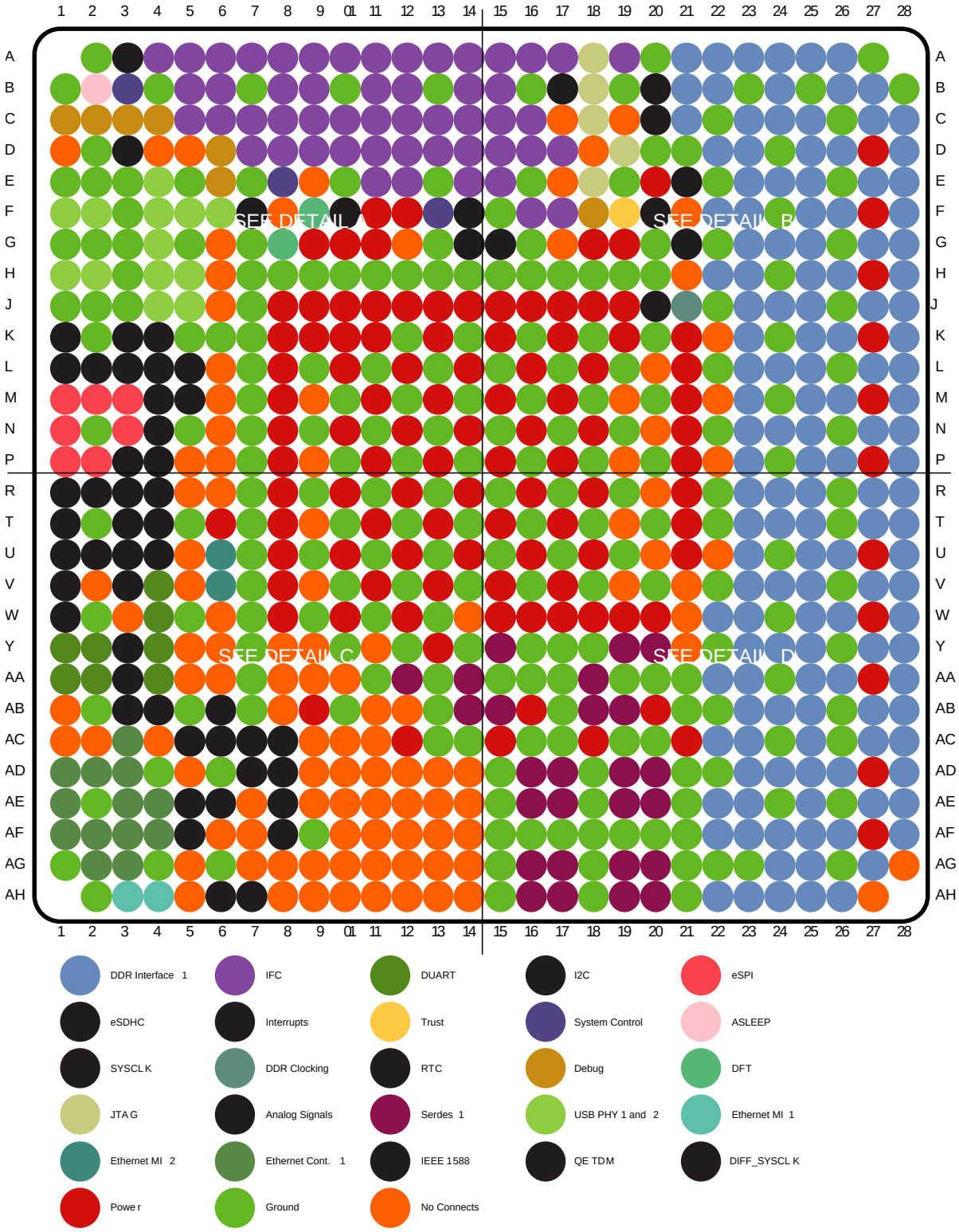


Figure 4: Detail A

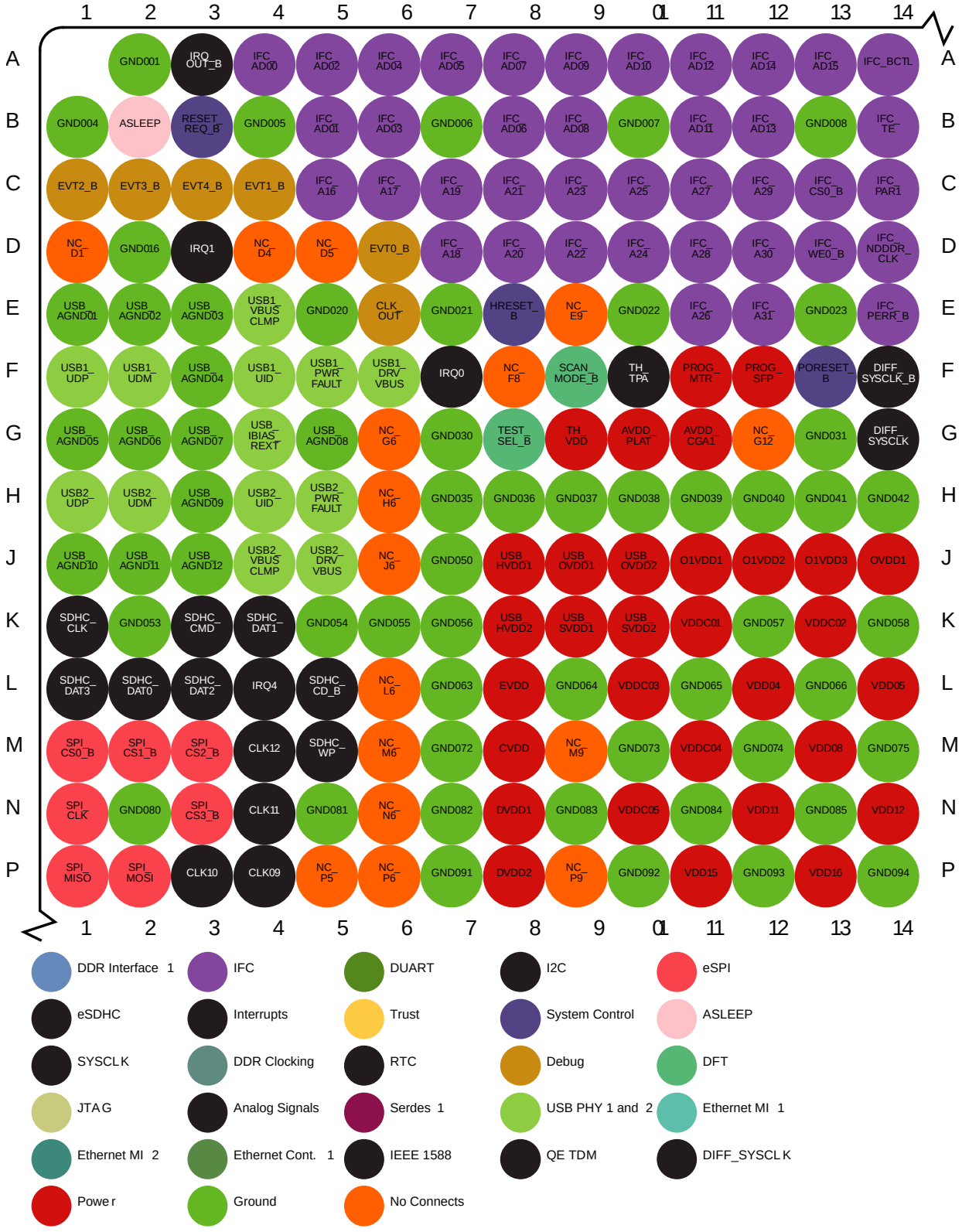


Figure 5: Detail B

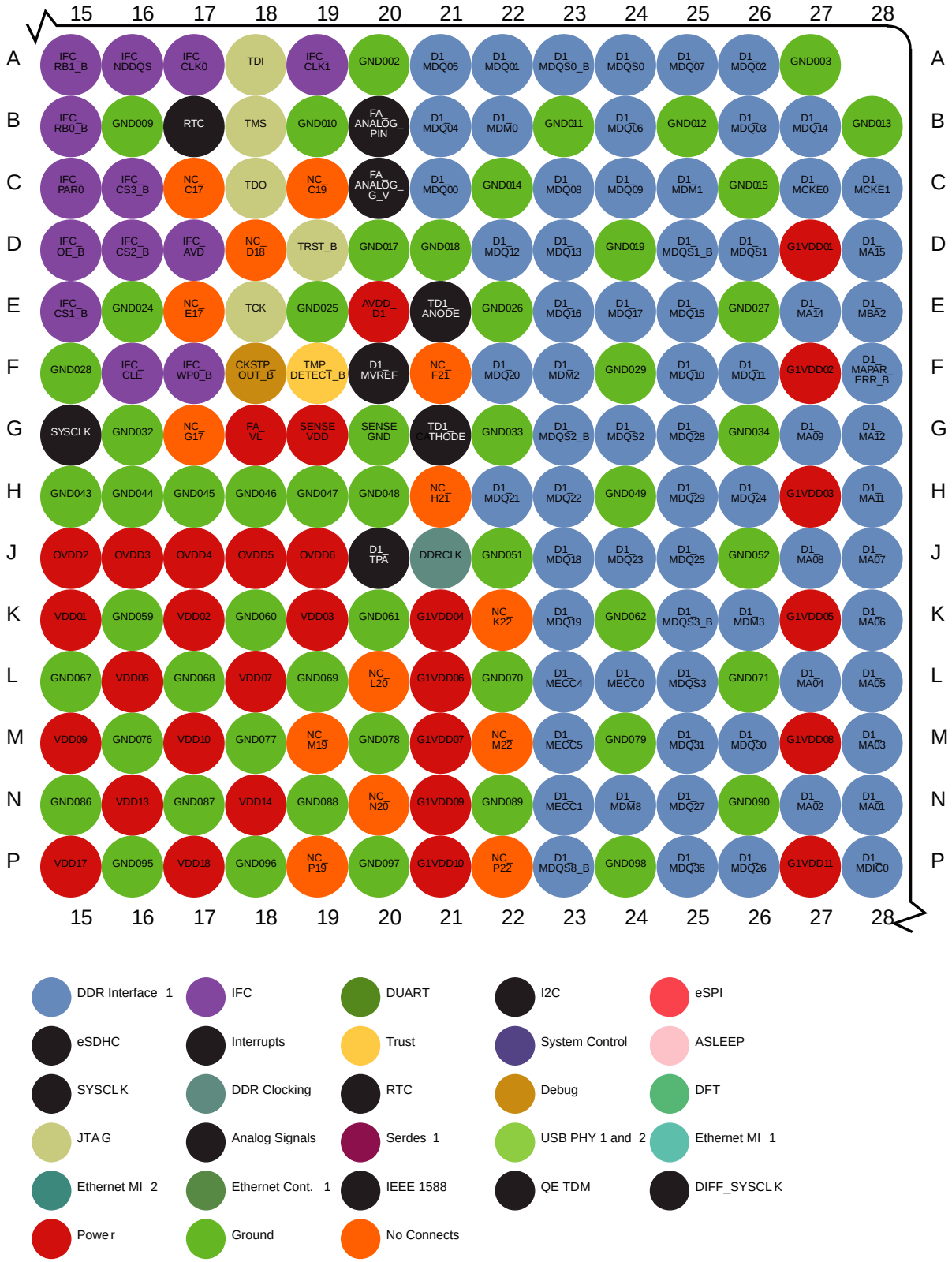


Figure 6: Detail C

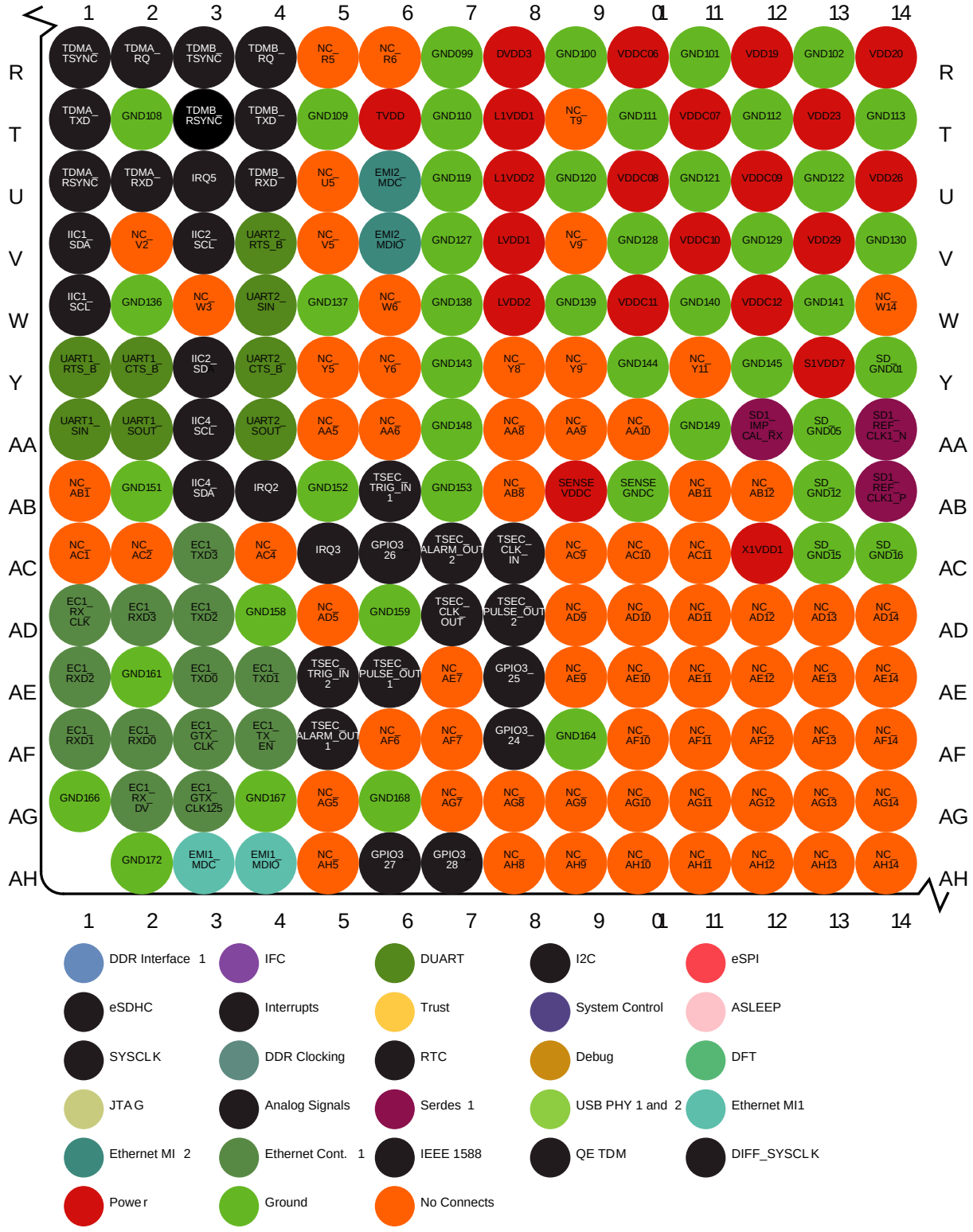
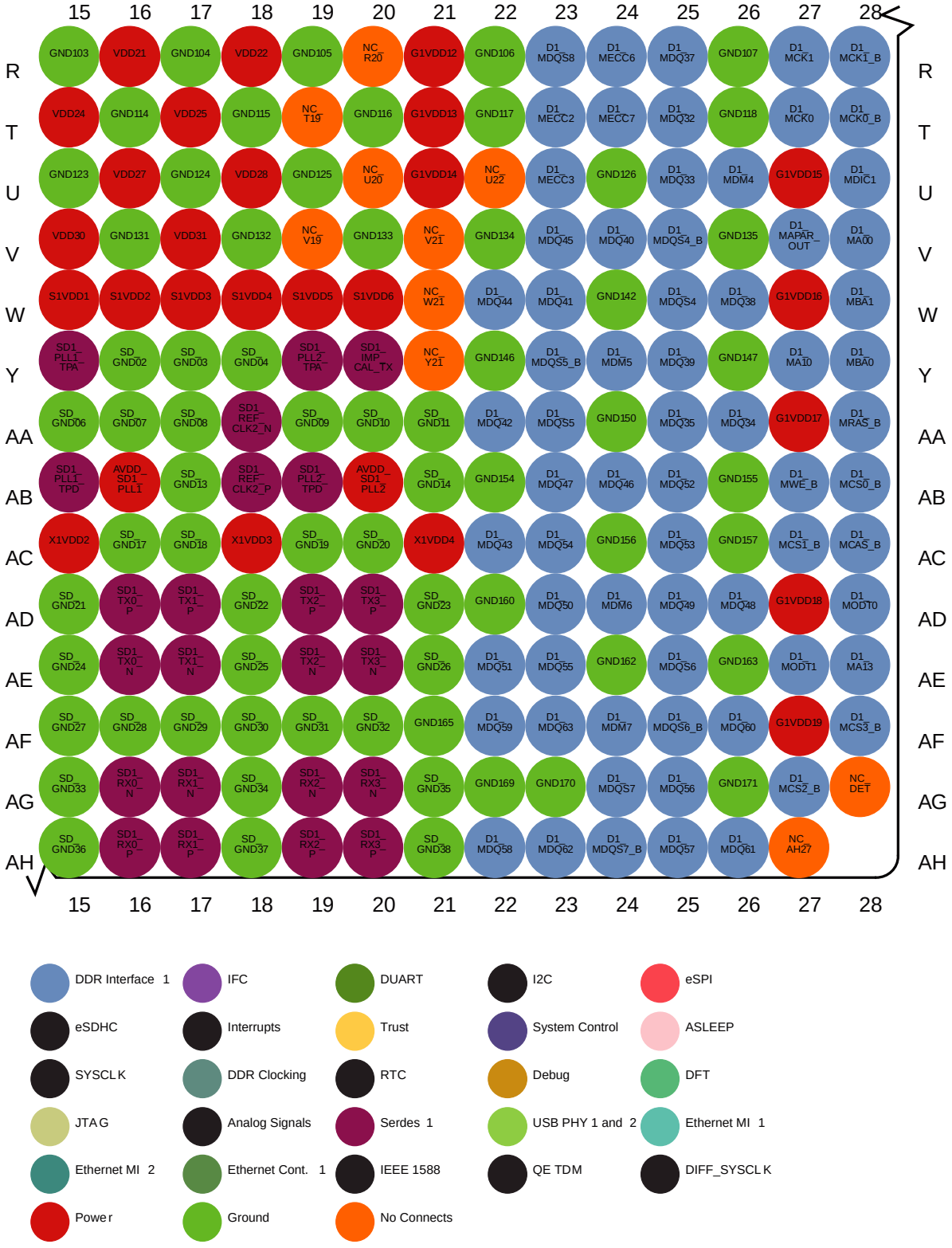


Figure 7: Detail D



2.2 Pinout list

This table provides the pinout listing for the T1024 by bus. Primary functions are **bolded** in the table.

Table 1: Pinout list by bus

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
DDR SDRAM Memory Interface					
D1_MA00	Address	V28	O	$G1V_{DD}$	–
D1_MA01	Address	N28	O	$G1V_{DD}$	–
D1_MA02	Address	N27	O	$G1V_{DD}$	–
D1_MA03	Address	M28	O	$G1V_{DD}$	–
D1_MA04	Address	L27	O	$G1V_{DD}$	–
D1_MA05	Address	L28	O	$G1V_{DD}$	–
D1_MA06	Address	K28	O	$G1V_{DD}$	–
D1_MA07	Address	J28	O	$G1V_{DD}$	–
D1_MA08	Address	J27	O	$G1V_{DD}$	–
D1_MA09	Address	G27	O	$G1V_{DD}$	–
D1_MA10	Address	Y27	O	$G1V_{DD}$	–
D1_MA11	Address	H28	O	$G1V_{DD}$	–
D1_MA12	Address	G28	O	$G1V_{DD}$	–
D1_MA13	Address	AE28	O	$G1V_{DD}$	–
D1_MA14	Address	E27	O	$G1V_{DD}$	25
D1_MA15	Address	D28	O	$G1V_{DD}$	25
D1_MAPAR_ERR_B	Address Parity Error	F28	I	$G1V_{DD}$	1, 6, 25
D1_MAPAR_OUT	Address Parity Out	V27	O	$G1V_{DD}$	25
D1_MBA0	Bank Select	Y28	O	$G1V_{DD}$	–
D1_MBA1	Bank Select	W28	O	$G1V_{DD}$	–
D1_MBA2	Bank Select	E28	O	$G1V_{DD}$	25
D1_MCAS_B	Column Address Strobe	AC28	O	$G1V_{DD}$	25
D1_MCK0	Clock	T27	O	$G1V_{DD}$	–
D1_MCK0_B	Clock Complement	T28	O	$G1V_{DD}$	–
D1_MCK1	Clock	R27	O	$G1V_{DD}$	–
D1_MCK1_B	Clock Complement	R28	O	$G1V_{DD}$	–
D1_MCKE0	Clock Enable	C27	O	$G1V_{DD}$	2
D1_MCKE1	Clock Enable	C28	O	$G1V_{DD}$	2
D1_MCS0_B	Chip Select	AB28	O	$G1V_{DD}$	–
D1_MCS1_B	Chip Select	AC27	O	$G1V_{DD}$	–
D1_MCS2_B	Chip Select	AG27	O	$G1V_{DD}$	–
D1_MCS3_B	Chip Select	AF28	O	$G1V_{DD}$	–
D1_MDIC0	Driver Impedence Calibration	P28	IO	$G1V_{DD}$	3
D1_MDIC1	Driver Impedence Calibration	U28	IO	$G1V_{DD}$	3
D1_MDM0	Data Mask	B22	O	$G1V_{DD}$	1, 25
D1_MDM1	Data Mask	C25	O	$G1V_{DD}$	1, 25
D1_MDM2	Data Mask	F23	O	$G1V_{DD}$	1, 25
D1_MDM3	Data Mask	K26	O	$G1V_{DD}$	1, 25

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MDM4	Data Mask	U26	O	$G1V_{DD}$	1, 25
D1_MDM5	Data Mask	Y24	O	$G1V_{DD}$	1, 25
D1_MDM6	Data Mask	AD24	O	$G1V_{DD}$	1, 25
D1_MDM7	Data Mask	AF24	O	$G1V_{DD}$	1, 25
D1_MDM8	Data Mask	N24	O	$G1V_{DD}$	1, 25
D1_MDQ00	Data	C21	IO	$G1V_{DD}$	–
D1_MDQ01	Data	A22	IO	$G1V_{DD}$	–
D1_MDQ02	Data	A26	IO	$G1V_{DD}$	–
D1_MDQ03	Data	B26	IO	$G1V_{DD}$	–
D1_MDQ04	Data	B21	IO	$G1V_{DD}$	–
D1_MDQ05	Data	A21	IO	$G1V_{DD}$	–
D1_MDQ06	Data	B24	IO	$G1V_{DD}$	–
D1_MDQ07	Data	A25	IO	$G1V_{DD}$	–
D1_MDQ08	Data	C23	IO	$G1V_{DD}$	–
D1_MDQ09	Data	C24	IO	$G1V_{DD}$	–
D1_MDQ10	Data	F25	IO	$G1V_{DD}$	–
D1_MDQ11	Data	F26	IO	$G1V_{DD}$	–
D1_MDQ12	Data	D22	IO	$G1V_{DD}$	–
D1_MDQ13	Data	D23	IO	$G1V_{DD}$	–
D1_MDQ14	Data	B27	IO	$G1V_{DD}$	–
D1_MDQ15	Data	E25	IO	$G1V_{DD}$	–
D1_MDQ16	Data	E23	IO	$G1V_{DD}$	–
D1_MDQ17	Data	E24	IO	$G1V_{DD}$	–
D1_MDQ18	Data	J23	IO	$G1V_{DD}$	–
D1_MDQ19	Data	K23	IO	$G1V_{DD}$	–
D1_MDQ20	Data	F22	IO	$G1V_{DD}$	–
D1_MDQ21	Data	H22	IO	$G1V_{DD}$	–
D1_MDQ22	Data	H23	IO	$G1V_{DD}$	–
D1_MDQ23	Data	J24	IO	$G1V_{DD}$	–
D1_MDQ24	Data	H26	IO	$G1V_{DD}$	–
D1_MDQ25	Data	J25	IO	$G1V_{DD}$	–
D1_MDQ26	Data	P26	IO	$G1V_{DD}$	–
D1_MDQ27	Data	N25	IO	$G1V_{DD}$	–
D1_MDQ28	Data	G25	IO	$G1V_{DD}$	–
D1_MDQ29	Data	H25	IO	$G1V_{DD}$	–
D1_MDQ30	Data	M26	IO	$G1V_{DD}$	–
D1_MDQ31	Data	M25	IO	$G1V_{DD}$	–
D1_MDQ32	Data	T25	IO	$G1V_{DD}$	–
D1_MDQ33	Data	U25	IO	$G1V_{DD}$	–
D1_MDQ34	Data	AA26	IO	$G1V_{DD}$	–
D1_MDQ35	Data	AA25	IO	$G1V_{DD}$	–
D1_MDQ36	Data	P25	IO	$G1V_{DD}$	–
D1_MDQ37	Data	R25	IO	$G1V_{DD}$	–

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MDQ38	Data	W26	IO	$G1V_{DD}$	–
D1_MDQ39	Data	Y25	IO	$G1V_{DD}$	–
D1_MDQ40	Data	V24	IO	$G1V_{DD}$	–
D1_MDQ41	Data	W23	IO	$G1V_{DD}$	–
D1_MDQ42	Data	AA22	IO	$G1V_{DD}$	–
D1_MDQ43	Data	AC22	IO	$G1V_{DD}$	–
D1_MDQ44	Data	W22	IO	$G1V_{DD}$	–
D1_MDQ45	Data	V23	IO	$G1V_{DD}$	–
D1_MDQ46	Data	AB24	IO	$G1V_{DD}$	–
D1_MDQ47	Data	AB23	IO	$G1V_{DD}$	–
D1_MDQ48	Data	AD26	IO	$G1V_{DD}$	–
D1_MDQ49	Data	AD25	IO	$G1V_{DD}$	–
D1_MDQ50	Data	AD23	IO	$G1V_{DD}$	–
D1_MDQ51	Data	AE22	IO	$G1V_{DD}$	–
D1_MDQ52	Data	AB25	IO	$G1V_{DD}$	–
D1_MDQ53	Data	AC25	IO	$G1V_{DD}$	–
D1_MDQ54	Data	AC23	IO	$G1V_{DD}$	–
D1_MDQ55	Data	AE23	IO	$G1V_{DD}$	–
D1_MDQ56	Data	AG25	IO	$G1V_{DD}$	–
D1_MDQ57	Data	AH25	IO	$G1V_{DD}$	–
D1_MDQ58	Data	AH22	IO	$G1V_{DD}$	–
D1_MDQ59	Data	AF22	IO	$G1V_{DD}$	–
D1_MDQ60	Data	AF26	IO	$G1V_{DD}$	–
D1_MDQ61	Data	AH26	IO	$G1V_{DD}$	–
D1_MDQ62	Data	AH23	IO	$G1V_{DD}$	–
D1_MDQ63	Data	AF23	IO	$G1V_{DD}$	–
D1_MDQS0	Data Strobe	A24	IO	$G1V_{DD}$	–
D1_MDQS0_B	Data Strobe	A23	IO	$G1V_{DD}$	–
D1_MDQS1	Data Strobe	D26	IO	$G1V_{DD}$	–
D1_MDQS1_B	Data Strobe	D25	IO	$G1V_{DD}$	–
D1_MDQS2	Data Strobe	G24	IO	$G1V_{DD}$	–
D1_MDQS2_B	Data Strobe	G23	IO	$G1V_{DD}$	–
D1_MDQS3	Data Strobe	L25	IO	$G1V_{DD}$	–
D1_MDQS3_B	Data Strobe	K25	IO	$G1V_{DD}$	–
D1_MDQS4	Data Strobe	W25	IO	$G1V_{DD}$	–
D1_MDQS4_B	Data Strobe	V25	IO	$G1V_{DD}$	–
D1_MDQS5	Data Strobe	AA23	IO	$G1V_{DD}$	–
D1_MDQS5_B	Data Strobe	Y23	IO	$G1V_{DD}$	–
D1_MDQS6	Data Strobe	AE25	IO	$G1V_{DD}$	–
D1_MDQS6_B	Data Strobe	AF25	IO	$G1V_{DD}$	–
D1_MDQS7	Data Strobe	AG24	IO	$G1V_{DD}$	–
D1_MDQS7_B	Data Strobe	AH24	IO	$G1V_{DD}$	–
D1_MDQS8	Data Strobe	R23	IO	$G1V_{DD}$	–

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MDQS8_B	Data Strobe	P23	IO	$G1V_{DD}$	–
D1_MECC0	Error Correcting Code	L24	IO	$G1V_{DD}$	–
D1_MECC1	Error Correcting Code	N23	IO	$G1V_{DD}$	–
D1_MECC2	Error Correcting Code	T23	IO	$G1V_{DD}$	–
D1_MECC3	Error Correcting Code	U23	IO	$G1V_{DD}$	–
D1_MECC4	Error Correcting Code	L23	IO	$G1V_{DD}$	–
D1_MECC5	Error Correcting Code	M23	IO	$G1V_{DD}$	–
D1_MECC6	Error Correcting Code	R24	IO	$G1V_{DD}$	–
D1_MECC7	Error Correcting Code	T24	IO	$G1V_{DD}$	–
D1_MODT0	On Die Termination	AD28	O	$G1V_{DD}$	2
D1_MODT1	On Die Termination	AE27	O	$G1V_{DD}$	2
D1_MRAS_B	Row Address Strobe	AA28	O	$G1V_{DD}$	25
D1_MWE_B	Write Enable	AB27	O	$G1V_{DD}$	1, 25
Integrated Flash Controller					
IFC_A16	IFC Address	C5	O	OV_{DD}	1, 5
IFC_A17	IFC Address	C6	O	OV_{DD}	1, 5
IFC_A18	IFC Address	D7	O	OV_{DD}	1, 5
IFC_A19	IFC Address	C7	O	OV_{DD}	1, 5
IFC_A20	IFC Address	D8	O	OV_{DD}	1, 5
IFC_A21/cfg_dram_type	IFC Address	C8	O	OV_{DD}	1, 4
IFC_A22	IFC Address	D9	O	OV_{DD}	1
IFC_A23	IFC Address	C9	O	OV_{DD}	1
IFC_A24	IFC Address	D10	O	OV_{DD}	1
IFC_A25/GPIO2_25/ IFC_WP1_B/IFC_CS4_B	IFC Address	C10	O	OV_{DD}	1
IFC_A26/GPIO2_26/ IFC_WP2_B/IFC_CS5_B	IFC Address	E11	O	OV_{DD}	1
IFC_A27/GPIO2_27/ IFC_WP3_B/IFC_CS6_B	IFC Address	C11	O	OV_{DD}	1
IFC_A28/GPIO2_28	IFC Address	D11	O	OV_{DD}	1
IFC_A29/GPIO2_29/ IFC_RB2_B	IFC Address	C12	O	OV_{DD}	1
IFC_A30/GPIO2_30/ IFC_RB3_B	IFC Address	D12	O	OV_{DD}	1
IFC_A31/GPIO2_31	IFC Address	E12	O	OV_{DD}	1
IFC_AD00/cfg_gpinput0	IFC Address / Data	A4	IO	OV_{DD}	4
IFC_AD01/cfg_gpinput1	IFC Address / Data	B5	IO	OV_{DD}	4
IFC_AD02/cfg_gpinput2	IFC Address / Data	A5	IO	OV_{DD}	4
IFC_AD03/cfg_gpinput3	IFC Address / Data	B6	IO	OV_{DD}	4
IFC_AD04/cfg_gpinput4	IFC Address / Data	A6	IO	OV_{DD}	4
IFC_AD05/cfg_gpinput5	IFC Address / Data	A7	IO	OV_{DD}	4
IFC_AD06/cfg_gpinput6	IFC Address / Data	B8	IO	OV_{DD}	4
IFC_AD07/cfg_gpinput7	IFC Address / Data	A8	IO	OV_{DD}	4
IFC_AD08/cfg_rcw_src0	IFC Address / Data	B9	IO	OV_{DD}	4
IFC_AD09/cfg_rcw_src1	IFC Address / Data	A9	IO	OV_{DD}	4
IFC_AD10/cfg_rcw_src2	IFC Address / Data	A10	IO	OV_{DD}	4

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
IFC_AD11/cfg_rcw_src3	IFC Address / Data	B11	IO	OV_{DD}	4
IFC_AD12/cfg_rcw_src4	IFC Address / Data	A11	IO	OV_{DD}	4
IFC_AD13/cfg_rcw_src5	IFC Address / Data	B12	IO	OV_{DD}	4
IFC_AD14/cfg_rcw_src6	IFC Address / Data	A12	IO	OV_{DD}	4
IFC_AD15/cfg_rcw_src7	IFC Address / Data	A13	IO	OV_{DD}	4
IFC_AVD	IFC Address Valid	D17	O	OV_{DD}	1, 5
IFC_BCTL	IFC Buffer control	A14	O	OV_{DD}	1
IFC_CLE/cfg_rcw_src8	IFC Command Latch Enable / Write Enable	F16	O	OV_{DD}	1, 4
IFC_CLK0	IFC Clock	A17	O	OV_{DD}	1,
IFC_CLK1	IFC Clock	A19	O	OV_{DD}	1,
IFC_CS0_B	IFC Chip Select	C13	O	OV_{DD}	1, 6
IFC_CS1_B/GPIO2_10	IFC Chip Select	E15	O	OV_{DD}	1, 6
IFC_CS2_B/GPIO2_11	IFC Chip Select	D16	O	OV_{DD}	1, 6
IFC_CS3_B/GPIO2_12	IFC Chip Select	C16	O	OV_{DD}	1, 6
IFC_CS4_B/**IFC_A25**/ GPIO2_25/IFC_WP1_B	IFC Chip Select	C10	O	OV_{DD}	1
IFC_CS5_B/**IFC_A26**/ GPIO2_26/IFC_WP2_B	IFC Chip Select	E11	O	OV_{DD}	1
IFC_CS6_B/**IFC_A27**/ GPIO2_27/IFC_WP3_B	IFC Chip Select	C11	O	OV_{DD}	1
IFC_NDDDR_CLK	IFC NAND DDR Clock	D14	O	OV_{DD}	1
IFC_NDDQS	IFC DQS Strobe	A16	IO	OV_{DD}	–
IFC_OE_B/cfg_eng_use1	IFC Output Enable	D15	O	OV_{DD}	1, 21
IFC_PAR0/GPIO2_13	IFC Address & Data Parity	C15	IO	OV_{DD}	–
IFC_PAR1/GPIO2_14	IFC Address & Data Parity	C14	IO	OV_{DD}	–
IFC_PERR_B/GPIO2_15	IFC Parity Error	E14	I	OV_{DD}	1, 6
IFC_RB0_B	IFC Ready / Busy CS0	B15	I	OV_{DD}	6
IFC_RB1_B	IFC Ready / Busy CS1	A15	I	OV_{DD}	6
IFC_RB2_B/**IFC_A29**/ GPIO2_29	IFC Ready/Busy CS 2	C12	I	OV_{DD}	1
IFC_RB3_B/**IFC_A30**/ GPIO2_30	IFC Ready/Busy CS 3	D12	I	OV_{DD}	1
IFC_TE/cfg_ifc_te	IFC External Transceiver Enable	B14	O	OV_{DD}	1, 4
IFC_WE0_B/cfg_eng_use0	IFC Write Enable	D13	O	OV_{DD}	1, 21
IFC_WP0_B/cfg_eng_use2	IFC Write Protect	F17	O	OV_{DD}	1, 21
IFC_WP1_B/**IFC_A25**/ GPIO2_25/IFC_CS4_B	IFC Write Protect	C10	O	OV_{DD}	1
IFC_WP2_B/**IFC_A26**/ GPIO2_26/IFC_CS5_B	IFC Write Protect	E11	O	OV_{DD}	1
IFC_WP3_B/**IFC_A27**/ GPIO2_27/IFC_CS6_B	IFC Write Protect	C11	O	OV_{DD}	1
DUART					
UART1_CTS_B/GPIO1_21/ UART3_SIN	Clear To Send	Y2	I	DV_{DD}	1
UART1_RTS_B/GPIO1_19/ UART3_SOUT	Ready to Send	Y1	O	DV_{DD}	1
UART1_SIN/GPIO1_17	Receive Data	AA1	I	DV_{DD}	1
UART1_SOUT/GPIO1_15	Transmit Data	AA2	O	DV_{DD}	1

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
UART2_CTS_B/GPIO1_22/ UART4_SIN/EVT8_B	Clear To Send	Y4	I	DV_{DD}	1
UART2_RTS_B/GPIO1_20/ UART4_SOUT/EVT7_B	Ready to Send	V4	O	DV_{DD}	1
UART2_SIN/GPIO1_18	Receive Data	W4	I	DV_{DD}	1
UART2_SOUT/GPIO1_16	Transmit Data	AA4	O	DV_{DD}	1
UART3_SIN/**UART1_CTS_B**/ GPIO1_21	Receive Data	Y2	I	DV_{DD}	1
UART3_SOUT/ **UART1_RTS_B/**GPIO1_19	Transmit Data	Y1	O	DV_{DD}	1
UART4_SIN/**UART2_CTS_B**/ GPIO1_22/EVT8_B	Receive Data	Y4	I	DV_{DD}	1
UART4_SOUT/ **UART2_RTS_B**/GPIO1_20/ EVT7_B	Transmit Data	V4	O	DV_{DD}	1
I2C					
IIC1_SCL	Serial Clock (supports PBL)	W1	IO	DV_{DD}	7, 8
IIC1_SDA	Serial Data (supports PBL)	V1	IO	DV_{DD}	7, 8
IIC2_SCL/GPIO4_27	Serial Clock	V3	IO	DV_{DD}	7, 8
IIC2_SDA/GPIO4_28	Serial Data	Y3	IO	DV_{DD}	7, 8
IIC3_SCL/**SDHC_CD_B**/ GPIO4_24	Serial Clock	L5	IO	CV_{DD}	–
IIC3_SDA/**SDHC_WP**/ GPIO4_25	Serial Data	M5	IO	CV_{DD}	–
IIC4_SCL/GPIO4_02/EVT5_B/ DIU_HSYNC	Serial Clock	AA3	IO	DV_{DD}	7, 8
IIC4_SDA/GPIO4_03/EVT6_B/ DIU_VSYNC	Serial Data	AB3	IO	DV_{DD}	7, 8
eSPI Interface					
SPI_CLK	SPI Clock	N1	O	CV_{DD}	1
SPI_CS0_B/GPIO2_00/ SDHC_DAT4	SPI Chip Select	M1	O	CV_{DD}	1
SPI_CS1_B/GPIO2_01/ SDHC_DAT5/ SDHC_CMD_DIR	SPI Chip Select	M2	O	CV_{DD}	1
SPI_CS2_B/GPIO2_02/ SDHC_DAT6/ SDHC_DAT0_DIR	SPI Chip Select	M3	O	CV_{DD}	1
SPI_CS3_B/GPIO2_03/ SDHC_DAT7/ SDHC_CLK_SYNC_OUT/ SDHC_DAT123_DIR	SPI Chip Select	N3	O	CV_{DD}	1
SPI_MISO	Master In Slave Out	P1	I	CV_{DD}	1
SPI_MOSI/SPI_BASE0	Master Out Slave In	P2	IO	CV_{DD}	–
eSDHC					
SDHC_CD_B/GPIO4_24/ IIC3_SCL	SDHC Card Detect	L5	I	CV_{DD}	1
SDHC_CLK/GPIO2_09/ DMA2_DDONE0_B	Host to Card Clock	K1	O	EV_{DD}	1
SDHC_CLK_SYNC_IN/**IRQ4**/ GPIO1_24	IN	L4	I	CV_{DD}	1
SDHC_CLK_SYNC_OUT/ **SPI_CS3_B**/GPIO2_03/ SDHC_DAT7/ SDHC_DAT123_DIR	OUT	N3	O	CV_{DD}	1

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SDHC_CMD/GPIO2_04/ DMA1_DREQ0_B	Command/Response	K3	IO	EV_{DD}	–
SDHC_CMD_DIR/**SPI_CS1_B**/ GPIO2_01/SDHC_DAT5	DIR	M2	O	CV_{DD}	1
SDHC_DAT0/GPIO2_05/ DMA1_DACK0_B	Data	L2	IO	EV_{DD}	–
SDHC_DAT0_DIR/ **SPI_CS2_B**/GPIO2_02/ SDHC_DAT6	DIR	M3	O	CV_{DD}	1
SDHC_DAT1/GPIO2_06/ DMA1_DDONE0_B	Data	K4	IO	EV_{DD}	–
SDHC_DAT123_DIR/ **SPI_CS3_B**/GPIO2_03/ SDHC_DAT7/ SDHC_CLK_SYNC_OUT	DIR	N3	O	CV_{DD}	1
SDHC_DAT2/GPIO2_07/ DMA2_DREQ0_B	Data	L3	IO	EV_{DD}	–
SDHC_DAT3/GPIO2_08/ DMA2_DACK0_B	Data	L1	IO	EV_{DD}	–
SDHC_DAT4/**SPI_CS0_B**/ GPIO2_00	Data	M1	IO	CV_{DD}	–
SDHC_DAT5/**SPI_CS1_B**/ GPIO2_01/SDHC_CMD_DIR	Data	M2	IO	CV_{DD}	–
SDHC_DAT6/**SPI_CS2_B**/ GPIO2_02/SDHC_DAT0_DIR	Data	M3	IO	CV_{DD}	–
SDHC_DAT7/**SPI_CS3_B**/ GPIO2_03/ SDHC_CLK_SYNC_OUT/ SDHC_DAT123_DIR	Data	N3	IO	CV_{DD}	–
SDHC_VS/**IRQ1**/USBCLK	VS	D3	O	$O1V_{DD}$	1
SDHC_WP/GPIO4_25/ IIC3_SDA	SDHC Write Protect	M5	I	CV_{DD}	1
Programmable Interrupt Controller					
IRQ0	External Interrupt	F7	I	$O1V_{DD}$	1
IRQ1/USBCLK/SDHC_VS	External Interrupt	D3	I	$O1V_{DD}$	1
IRQ2	External Interrupt	AB4	I	$L1V_{DD}$	1
IRQ3/GPIO1_23	External Interrupt	AC5	I	$L1V_{DD}$	1
IRQ4/GPIO1_24/ SDHC_CLK_SYNC_IN	External Interrupt	L4	I	CV_{DD}	1
IRQ5/GPIO1_25	External Interrupt	U3	I	DV_{DD}	1
IRQ_OUT_B/EVT9_B	Interrupt Output	A3	O	$O1V_{DD}$	1, 6, 7
Trust					
TMP_DETECT_B	Tamper Detect	F19	I	OV_{DD}	1
System Control					
HRESET_B	Hard Reset	E8	IO	$O1V_{DD}$	7, 27
PORESET_B	Power On Reset	F13	I	$O1V_{DD}$	26
RESET_REQ_B	Reset Request (POR or Hard)	B3	O	$O1V_{DD}$	1, 5
Power Management					
ASLEEP/GPIO1_13	Asleep	B2	O	$O1V_{DD}$	1
SYSCLK					
SYSCLK	System Clock	G15	I	$O1V_{DD}$	18

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
DDR Clocking					
DDRCLK	DDR Controller Clock	J21	I	OV_{DD}	18
RTC					
RTC/GPIO1_14	Real Time Clock	B17	I	OV_{DD}	1
Debug					
CKSTP_OUT_B	Checkstop Out	F18	O	OV_{DD}	1, 6, 7
CLK_OUT	Clock Out	E6	O	$O1V_{DD}$	2
EVT0_B	Event 0	D6	IO	$O1V_{DD}$	9
EVT1_B	Event 1	C4	IO	$O1V_{DD}$	–
EVT2_B	Event 2	C1	IO	$O1V_{DD}$	6, 22
EVT3_B	Event 3	C2	IO	$O1V_{DD}$	–
EVT4_B	Event 4	C3	IO	$O1V_{DD}$	–
EVT5_B/**IIC4_SCL**/GPIO4_02/ DIU_HSYNC	Event 5	AA3	IO	DV_{DD}	–
EVT6_B/**IIC4_SDA**/GPIO4_03/ DIU_VSYNC	Event 6	AB3	IO	DV_{DD}	–
EVT7_B/**UART2_RTS_B**/ GPIO1_20/UART4_SOUT	Event 7	V4	IO	DV_{DD}	–
EVT8_B/**UART2_CTS_B**/ GPIO1_22/UART4_SIN	Event 8	Y4	IO	DV_{DD}	–
EVT9_B/**IRQ_OUT_B**	Event 9	A3	IO	$O1V_{DD}$	–
DFT					
SCAN_MODE_B	Reserved	F9	I	$O1V_{DD}$	10
TEST_SEL_B	Reserved	G8	I	$O1V_{DD}$	23
JTAG					
TCK	Test Clock	E18	I	OV_{DD}	–
TDI	Test Data In	A18	I	OV_{DD}	9
TDO	Test Data Out	C18	O	OV_{DD}	2
TMS	Test Mode Select	B18	I	OV_{DD}	9
TRST_B	Test Reset	D19	I	OV_{DD}	9
Analog Signals					
D1_MVREF	SSTL Reference Voltage	F20	IO	$G1V_{DD}/2$	–
D1_TPA	Reserved	J20	IO		12
FA_ANALOG_G_V	Reserved	C20	IO		15
FA_ANALOG_PIN	Reserved	B20	IO		15
TD1_ANODE	Thermal diode anode	E21	IO		17
TD1_CATHODE	Thermal diode cathode	G21	IO		17
TH_**TPA**	Reserved	F10	–	–	12
Serdes 1					
SD1_IMP_CAL_RX	SerDes Receive Impedence Calibration	AA12	I	$S1V_{DD}$	11
SD1_IMP_CAL_TX	SerDes Transmit Impedance Calibration	Y20	I	$X1V_{DD}$	16
SD1_PLL1_TPA	Reserved	Y15	O	AVDD_SD1_PLL1	12
SD1_PLL1_TPD	Reserved	AB15	O	$X1V_{DD}$	12

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD1_PLL2_TPA	Reserved	Y19	O	AVDD_SD1_PLL2	12
SD1_PLL2_TPD	Reserved	AB19	O	$X1V_{DD}$	12
SD1_REF_CLK1_N	SerDes PLL 1 Reference Clock Complement	AA14	I	$S1V_{DD}$	–
SD1_REF_CLK1_P	SerDes PLL 1 Reference Clock	AB14	I	$S1V_{DD}$	–
SD1_REF_CLK2_N	SerDes PLL 2 Reference Clock Complement	AA18	I	$S1V_{DD}$	–
SD1_REF_CLK2_P	SerDes PLL 2 Reference Clock	AB18	I	$S1V_{DD}$	–
SD1_RX0_N	SerDes Receive Data (negative)	AG16	I	$S1V_{DD}$	–
SD1_RX0_P	SerDes Receive Data (positive)	AH16	I	$S1V_{DD}$	–
SD1_RX1_N	SerDes Receive Data (negative)	AG17	I	$S1V_{DD}$	–
SD1_RX1_P	SerDes Receive Data (positive)	AH17	I	$S1V_{DD}$	–
SD1_RX2_N	SerDes Receive Data (negative)	AG19	I	$S1V_{DD}$	–
SD1_RX2_P	SerDes Receive Data (positive)	AH19	I	$S1V_{DD}$	–
SD1_RX3_N	SerDes Receive Data (negative)	AG20	I	$S1V_{DD}$	–
SD1_RX3_P	SerDes Receive Data (positive)	AH20	I	$S1V_{DD}$	–
SD1_TX0_N	SerDes Transmit Data (negative)	AE16	O	$X1V_{DD}$	–
SD1_TX0_P	SerDes Transmit Data (positive)	AD16	O	$X1V_{DD}$	–
SD1_TX1_N	SerDes Transmit Data (negative)	AE17	O	$X1V_{DD}$	–
SD1_TX1_P	SerDes Transmit Data (positive)	AD17	O	$X1V_{DD}$	–
SD1_TX2_N	SerDes Transmit Data (negative)	AE19	O	$X1V_{DD}$	–
SD1_TX2_P	SerDes Transmit Data (positive)	AD19	O	$X1V_{DD}$	–
SD1_TX3_N	SerDes Transmit Data (negative)	AE20	O	$X1V_{DD}$	–
SD1_TX3_P	SerDes Transmit Data (positive)	AD20	O	$X1V_{DD}$	–
USB PHY 1 & 2					
IRQ1/USBCLK/SDHC_VS	USB Clock	D3	I	$O1V_{DD}$	1
USB1_DRVVBUS	USB PHY Digital signal – Drive VBUS	F6	O	USB_HV_{DD}	–
USB1_PWRFAULT	USB PHY Digital signal – Power Fault	F5	I	USB_HV_{DD}	–
USB1_UDM	USB PHY Data Minus	F2	IO	USB_HV_{DD}	–
USB1_UDP	USB PHY Data Plus	F1	IO	USB_HV_{DD}	–
USB1_UID	USB PHY ID Detect	F4	I	USB_OV_{DD}	–
USB1_VBUSCLMP	USB PHY VBUS	E4	I	USB_HV_{DD}	–
USB2_DRVVBUS	USB PHY Digital signal – Drive VBUS	J5	O	USB_HV_{DD}	–
USB2_PWRFAULT	USB PHY Digital signal – Power Fault	H5	I	USB_HV_{DD}	–
USB2_UDM	USB PHY Data Minus	H2	IO	USB_HV_{DD}	–
USB2_UDP	USB PHY Data Plus	H1	IO	USB_HV_{DD}	–
USB2_UID	USB PHY ID Detect	H4	I	USB_OV_{DD}	–
USB2_VBUSCLMP	USB PHY VBUS	J4	I	USB_HV_{DD}	–
USB_IBIAS_REXT	USB PHY Impedance Calibration	G4	IO	USB_OV_{DD}	20
Ethernet Management Interface 1					
EMI1_MDC/GPIO3_08	Management Data Clock	AH3	O	$L1V_{DD}$	–

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
EMI1_MDIO/GPIO3_09	Management Data In/Out	AH4	IO	$L1V_{DD}$	–
Ethernet Management Interface 2					
EMI2_MDC	Management Data Clock	U6	O	TV_{DD}	7, 13
EMI2_MDIO	Management Data In/Out	V6	IO	TV_{DD}	7, 13
Ethernet Controller 1					
EC1_GTX_CLK/GPIO3_16	Transmit Clock Out	AF3	O	$L1V_{DD}$	1
EC1_GTX_CLK125/GPIO3_17	Reference Clock	AG3	I	$L1V_{DD}$	1
EC1_RXD0/GPIO3_21	Receive Data	AF2	I	$L1V_{DD}$	1
EC1_RXD1/GPIO3_20	Receive Data	AF1	I	$L1V_{DD}$	1
EC1_RXD2/GPIO3_19	Receive Data	AE1	I	$L1V_{DD}$	1
EC1_RXD3/GPIO3_18	Receive Data	AD2	I	$L1V_{DD}$	1
EC1_RX_CLK/GPIO3_23	Receive Clock	AD1	I	$L1V_{DD}$	1
EC1_RX_DV/GPIO3_22	Receive Data Valid	AG2	I	$L1V_{DD}$	1
EC1_TXD0/GPIO3_14	Transmit Data	AE3	O	$L1V_{DD}$	1
EC1_TXD1/GPIO3_13	Transmit Data	AE4	O	$L1V_{DD}$	1
EC1_TXD2/GPIO3_12	Transmit Data	AD3	O	$L1V_{DD}$	1
EC1_TXD3/GPIO3_11	Transmit Data	AC3	O	$L1V_{DD}$	1
EC1_TX_EN/GPIO3_15	Transmit Enable	AF4	O	$L1V_{DD}$	1, 14
IEEE 1588					
TSEC_1588_ALARM_OUT1/ GPIO3_03/EC2_RX_CLK	Alarm Out 1	AF5	O	LV_{DD}	1
TSEC_1588_ALARM_OUT2/ GPIO3_04/EC2_TXD0	Alarm Out 2	AC7	O	LV_{DD}	1
TSEC_1588_CLK_IN/ GPIO3_00/EC2_GTX_CLK	Clock In	AC8	I	LV_{DD}	1
TSEC_1588_CLK_OUT/ GPIO3_05/EC2_TXD1	Clock Out	AD7	O	LV_{DD}	1
TSEC_1588_PULSE_OUT1/ GPIO3_06/EC2_RXD2	Pulse Out 1	AE6	O	LV_{DD}	1
TSEC_1588_PULSE_OUT2/ GPIO3_07/EC2_TX_EN	Pulse Out 2	AD8	O	LV_{DD}	1
TSEC_1588_TRIG_IN1/ GPIO3_01/EC2_TXD2	Trigger In 1	AB6	I	LV_{DD}	1
TSEC_1588_TRIG_IN2/ GPIO3_02/EC2_GTX_CLK125	Trigger In 2	AE5	I	LV_{DD}	1
QUICC Engine – TDM					
CLK09/GPIO4_15/BRGO2/ DIU_D10	External Clock	P4	I	DV_{DD}	1
CLK10/GPIO4_22/BRGO3/ DIU_D11	External Clock	P3	I	DV_{DD}	1
CLK11/GPIO4_16/BRGO4/ DIU_DE	External Clock	N4	I	DV_{DD}	1
CLK12/GPIO4_23/BRGO1/ DIU_CLK_OUT	External Clock	M4	I	DV_{DD}	1
TDMA_RQ/GPIO4_14/ UC1_CDB_RXER/DIU_D4	Request	R2	O	DV_{DD}	1
TDMA_RSYNC/GPIO4_11/ UC1_CTSB_RXDV/DIU_D1	Receive Sync	U1	I	DV_{DD}	1
TDMA_RXD/GPIO4_10/ UC1_RXD7/DIU_D0	Receive Data	U2	I	DV_{DD}	1

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
TDMA_TSYNC/GPIO4_13/ UC1_RTSB_TXEN/DIU_D3	Transmit Sync	R1	I	DV_{DD}	1
TDMA_TXD/GPIO4_12/ UC1_TXD7/DIU_D2	Transmit Data	T1	O	DV_{DD}	1
TDMB_RQ/GPIO4_21/ UC3_CDB_RXER/DIU_D9	Request	R4	O	DV_{DD}	1
TDMB_RSYNC/GPIO4_18/ UC3_CTSB_RXDV/DIU_D6	Receive Sync	T3	I	DV_{DD}	1
TDMB_RXD/GPIO4_17/ UC3_RXD7/DIU_D5	Receive Data	U4	I	DV_{DD}	1
TDMB_TSYNC/GPIO4_20/ UC3_RTSB_TXEN/DIU_D8	Transmit Sync	R3	I	DV_{DD}	1
TDMB_TXD/GPIO4_19/ UC3_TXD7/DIU_D7	Transmit Data	T4	O	DV_{DD}	1
DSYSCLK					
DIFF_SYSCLK	Single Source System Clock Differential (positive)	G14	I	$O1V_{DD}$	19
DIFF_SYSCLK_B	Single Source System Clock Differential (negative)	F14	I	$O1V_{DD}$	19
Power-On-Reset Configuration					
cfg_dram_type/**IFC_A21**	Power-on-Reset Configuration	C8	I	OV_{DD}	1, 4
cfg_gpinput0/**IFC_AD00**	Power-on-Reset Configuration	A4	I	OV_{DD}	1, 4
cfg_gpinput1/**IFC_AD01**	Power-on-Reset Configuration	B5	I	OV_{DD}	1, 4
cfg_gpinput2/**IFC_AD02**	Power-on-Reset Configuration	A5	I	OV_{DD}	1, 4
cfg_gpinput3/**IFC_AD03**	Power-on-Reset Configuration	B6	I	OV_{DD}	1, 4
cfg_gpinput4/**IFC_AD04**	Power-on-Reset Configuration	A6	I	OV_{DD}	1, 4
cfg_gpinput5/**IFC_AD05**	Power-on-Reset Configuration	A7	I	OV_{DD}	1, 4
cfg_gpinput6/**IFC_AD06**	Power-on-Reset Configuration	B8	I	OV_{DD}	1, 4
cfg_gpinput7/**IFC_AD07**	Power-on-Reset Configuration	A8	I	OV_{DD}	1, 4
cfg_ifc_te/**IFC_TE**	Power-on-Reset Configuration	B14	I	OV_{DD}	1, 4
cfg_rcw_src0/**IFC_AD08**	Power-on-Reset Configuration	B9	I	OV_{DD}	1, 4
cfg_rcw_src1/**IFC_AD09**	Power-on-Reset Configuration	A9	I	OV_{DD}	1, 4
cfg_rcw_src2/**IFC_AD10**	Power-on-Reset Configuration	A10	I	OV_{DD}	1, 4
cfg_rcw_src3/**IFC_AD11**	Power-on-Reset Configuration	B11	I	OV_{DD}	1, 4
cfg_rcw_src4/**IFC_AD12**	Power-on-Reset Configuration	A11	I	OV_{DD}	1, 4
cfg_rcw_src5/**IFC_AD13**	Power-on-Reset Configuration	B12	I	OV_{DD}	1, 4
cfg_rcw_src6/**IFC_AD14**	Power-on-Reset Configuration	A12	I	OV_{DD}	1, 4
cfg_rcw_src7/**IFC_AD15**	Power-on-Reset Configuration	A13	I	OV_{DD}	1, 4
cfg_rcw_src8/**IFC_CLE**	Power-on-Reset Configuration	F16	I	OV_{DD}	1, 4
QUICC Engine					
UC1_CDB_RXER/**TDMA_RQ**/ GPIO4_14/DIU_D4	Receive Error	R2	I	DV_{DD}	1
UC1_CTSB_RXDV/ **TDMA_RSYNC**/GPIO4_11/ DIU_D1	Receive Data	U1	I	DV_{DD}	1
UC1_RTSB_TXEN/ **TDMA_TSYNC**/GPIO4_13/ DIU_D3	Transmit Enable	R1	O	DV_{DD}	1
UC1_RXD7/**TDMA_RXD**/ GPIO4_10/DIU_D0	Receive Data	U2	I	DV_{DD}	1

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
UC1_TXD7/**TDMA_TXD**/ GPIO4_12/DIU_D2	Transmit Data	T1	O	DV_{DD}	1
UC3_CDB_RXER/**TDMB_RQ**/ GPIO4_21/DIU_D9	Receive Error	R4	I	DV_{DD}	1
UC3_CTSB_RXDV/ **TDMB_RSYNC**/GPIO4_18/ DIU_D6	Receive Data	T3	I	DV_{DD}	1
UC3_RTSB_TXEN/ **TDMB_TSYNC**/GPIO4_20/ DIU_D8	Transmit Enable	R3	O	DV_{DD}	1
UC3_RXD7/**TDMB_RXD**/ GPIO4_17/DIU_D5	Receive Data	U4	I	DV_{DD}	1
UC3_TXD7/**TDMB_TXD**/ GPIO4_19/DIU_D7	Transmit Data	T4	O	DV_{DD}	1
Direct Memory Access					
DMA1_DACK0_B/ **SDHC_DAT0**/GPIO2_05	DMA1 channel 0 acknowledge	L2	O	EV_{DD}	1
DMA1_DDONE0_B/ **SDHC_DAT1**/GPIO2_06	DMA1 channel 0 done	K4	IO	EV_{DD}	–
DMA1_DREQ0_B/ **SDHC_CMD**/GPIO2_04	DMA1 channel 0 request	K3	I	EV_{DD}	1
DMA2_DACK0_B/ **SDHC_DAT3**/GPIO2_08	DMA2 channel 0 acknowledge	L1	IO	EV_{DD}	–
DMA2_DDONE0_B/ **SDHC_CLK**/GPIO2_09	DMA2 channel 0 done	K1	O	EV_{DD}	1
DMA2_DREQ0_B/ **SDHC_DAT2**/GPIO2_07	DMA2 channel 0 request	L3	IO	EV_{DD}	–
Ethernet controller 2					
EC2_GTX_CLK/ **TSEC_1588_CLK_IN**/ GPIO3_00	Transmit Clock Out	AC8	O	LV_{DD}	1
EC2_GTX_CLK125/ **TSEC_1588_TRIG_IN2**/ GPIO3_02	Reference Clock	AE5	I	LV_{DD}	1
EC2_RXD0/**GPIO3_25**	Receive Data 0	AE8	I	LV_{DD}	1
EC2_RXD1/**GPIO3_28**	Receive Data 1	AH7	I	LV_{DD}	1
EC2_RXD2/ **TSEC_1588_PULSE_OUT1**/ GPIO3_06	Receive Data 2	AE6	I	LV_{DD}	1
EC2_RXD3/**GPIO3_27**	Receive Data 3	AH6	I	LV_{DD}	1
EC2_RX_CLK/ **TSEC_1588_ALARM_OUT1**/ GPIO3_03	Receive Clock	AF5	I	LV_{DD}	1
EC2_RX_DV/**GPIO3_24**	Receive Data Valid	AF8	I	LV_{DD}	1
EC2_TXD0/ **TSEC_1588_ALARM_OUT2**/ GPIO3_04	Transmit Data 0	AC7	O	LV_{DD}	1
EC2_TXD1/ **TSEC_1588_CLK_OUT**/ GPIO3_05	Transmit Data 1	AD7	O	LV_{DD}	1
EC2_TXD2/ **TSEC_1588_TRIG_IN1**/ GPIO3_01	Transmit Data 2	AB6	O	LV_{DD}	1
EC2_TXD3/**GPIO3_26**	Transmit Data 3	AC6	O	LV_{DD}	1
EC2_TX_EN/ **TSEC_1588_PULSE_OUT2**/ GPIO3_07	Transmit Enable	AD8	O	LV_{DD}	1
Display Interface Unit					

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
DIU_CLK_OUT/**CLK12**/ GPIO4_23/BRGO1	Pixel Clock	M4	O	DV_{DD}	1
DIU_D0/**TDMA_RXD**/ GPIO4_10/UC1_RXD7	DIU Data	U2	O	DV_{DD}	1
DIU_D1/**TDMA_RSYNC**/ GPIO4_11/UC1_CTSB_RXDV	DIU Data	U1	O	DV_{DD}	1
DIU_D10/**CLK09**/GPIO4_15/ BRGO2	DIU Data	P4	O	DV_{DD}	1
DIU_D11/**CLK10**/GPIO4_22/ BRGO3	DIU Data	P3	O	DV_{DD}	1
DIU_D2/**TDMA_TXD**/ GPIO4_12/UC1_TXD7	DIU Data	T1	O	DV_{DD}	1
DIU_D3/**TDMA_TSYNC**/ GPIO4_13/UC1_RTSB_TXEN	DIU Data	R1	O	DV_{DD}	1
DIU_D4/**TDMA_RQ**/ GPIO4_14/UC1_CDB_RXER	DIU Data	R2	O	DV_{DD}	1
DIU_D5/**TDMB_RXD**/ GPIO4_17/UC3_RXD7	DIU Data	U4	O	DV_{DD}	1
DIU_D6/**TDMB_RSYNC**/ GPIO4_18/UC3_CTSB_RXDV	DIU Data	T3	O	DV_{DD}	1
DIU_D7/**TDMB_TXD**/ GPIO4_19/UC3_TXD7	DIU Data	T4	O	DV_{DD}	1
DIU_D8/**TDMB_TSYNC**/ GPIO4_20/UC3_RTSB_TXEN	DIU Data	R3	O	DV_{DD}	1
DIU_D9/**TDMB_RQ**/ GPIO4_21/UC3_CDB_RXER	DIU Data	R4	O	DV_{DD}	1
DIU_DE/**CLK11**/GPIO4_16/ BRGO4	Data Enable	N4	O	DV_{DD}	1
DIU_HSYNC/**IIC4_SCL**/ GPIO4_02/EVT5_B	Horizontal Sync	AA3	O	DV_{DD}	1
DIU_VSYNC/**IIC4_SDA**/ GPIO4_03/EVT6_B	Vertical Sync	AB3	O	DV_{DD}	1
Baud rate generator					
BRGO1/**CLK12**/GPIO4_23/ DIU_CLK_OUT	BRGO1	M4	O	DV_{DD}	1
BRGO2/**CLK09**/GPIO4_15/ DIU_D10	BRGO2	P4	O	DV_{DD}	1
BRGO3/**CLK10**/GPIO4_22/ DIU_D11	BRGO3	P3	O	DV_{DD}	1
BRGO4/**CLK11**/GPIO4_16/ DIU_DE	BRGO4	N4	O	DV_{DD}	1
GPIO					
GPIO1_13/**ASLEEP**	General Purpose Input/Output	B2	O	$O1V_{DD}$	1
GPIO1_14/**RTC**	General Purpose Input/Output	B17	IO	OV_{DD}	–
GPIO1_15/UART1_SOUT	General Purpose Input/Output	AA2	IO	DV_{DD}	–
GPIO1_16/UART2_SOUT	General Purpose Input/Output	AA4	IO	DV_{DD}	–
GPIO1_17/**UART1_SIN**	General Purpose Input/Output	AA1	IO	DV_{DD}	–
GPIO1_18/**UART2_SIN**	General Purpose Input/Output	W4	IO	DV_{DD}	–
GPIO1_19/**UART1_RTS_B**/ UART3_SOUT	General Purpose Input/Output	Y1	IO	DV_{DD}	–
GPIO1_20/**UART2_RTS_B**/ UART4_SOUT/EVT7_B	General Purpose Input/Output	V4	IO	DV_{DD}	–

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GPIO1_21/**UART1_CTS_B**/ UART3_SIN	General Purpose Input/Output	Y2	IO	DV_{DD}	–
GPIO1_22/**UART2_CTS_B**/ UART4_SIN/EVT8_B	General Purpose Input/Output	Y4	IO	DV_{DD}	–
GPIO1_23/**IRQ3**	General Purpose Input/Output	AC5	IO	$L1V_{DD}$	–
GPIO1_24/**IRQ4**/ SDHC_CLK_SYNC_IN	General Purpose Input/Output	L4	IO	CV_{DD}	–
GPIO1_25/**IRQ5**	General Purpose Input/Output	U3	IO	DV_{DD}	–
GPIO2_00/**SPI_CS0_B**/ SDHC_DAT4	General Purpose Input/Output	M1	IO	CV_{DD}	–
GPIO2_01/**SPI_CS1_B**/ SDHC_DAT5/ SDHC_CMD_DIR	General Purpose Input/Output	M2	IO	CV_{DD}	–
GPIO2_02/**SPI_CS2_B**/ SDHC_DAT6/ SDHC_DAT0_DIR	General Purpose Input/Output	M3	IO	CV_{DD}	–
GPIO2_03/**SPI_CS3_B**/ SDHC_DAT7/ SDHC_CLK_SYNC_OUT/ SDHC_DAT123_DIR	General Purpose Input/Output	N3	IO	CV_{DD}	–
GPIO2_04/**SDHC_CMD**/ DMA1_DREQ0_B	General Purpose Input/Output	K3	IO	EV_{DD}	–
GPIO2_05/**SDHC_DAT0**/ DMA1_DACK0_B	General Purpose Input/Output	L2	IO	EV_{DD}	–
GPIO2_06/**SDHC_DAT1**/ DMA1_DDONE0_B	General Purpose Input/Output	K4	IO	EV_{DD}	–
GPIO2_07/**SDHC_DAT2**/ DMA2_DREQ0_B	General Purpose Input/Output	L3	IO	EV_{DD}	–
GPIO2_08/**SDHC_DAT3**/ DMA2_DACK0_B	General Purpose Input/Output	L1	IO	EV_{DD}	–
GPIO2_09/**SDHC_CLK**/ DMA2_DDONE0_B	General Purpose Input/Output	K1	IO	EV_{DD}	–
GPIO2_10/**IFC_CS1_B**	General Purpose Input/Output	E15	IO	OV_{DD}	–
GPIO2_11/**IFC_CS2_B**	General Purpose Input/Output	D16	IO	OV_{DD}	–
GPIO2_12/**IFC_CS3_B**	General Purpose Input/Output	C16	IO	OV_{DD}	–
GPIO2_13/**IFC_PAR0**	General Purpose Input/Output	C15	IO	OV_{DD}	–
GPIO2_14/**IFC_PAR1**	General Purpose Input/Output	C14	IO	OV_{DD}	–
GPIO2_15/IFC_PERR_B	General Purpose Input/Output	E14	IO	OV_{DD}	–
GPIO2_25/**IFC_A25**/ IFC_WP1_B/IFC_CS4_B	General Purpose Input/Output	C10	IO	OV_{DD}	–
GPIO2_26/**IFC_A26**/ IFC_WP2_B/IFC_CS5_B	General Purpose Input/Output	E11	IO	OV_{DD}	–
GPIO2_27/**IFC_A27**/ IFC_WP3_B/IFC_CS6_B	General Purpose Input/Output	C11	IO	OV_{DD}	–
GPIO2_28/**IFC_A28**	General Purpose Input/Output	D11	IO	OV_{DD}	–
GPIO2_29/**IFC_A29**/ IFC_RB2_B	General Purpose Input/Output	C12	IO	OV_{DD}	–
GPIO2_30/**IFC_A30**/ IFC_RB3_B	General Purpose Input/Output	D12	IO	OV_{DD}	–
GPIO2_31/**IFC_A31**	General Purpose Input/Output	E12	IO	OV_{DD}	–
GPIO3_00/ **TSEC_1588_CLK_IN**/ EC2_GTX_CLK	General Purpose Input/Output	AC8	IO	LV_{DD}	–

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GPIO3_01/ **TSEC_1588_TRIG_IN1**/ EC2_TXD2	General Purpose Input/Output	AB6	IO	LV_{DD}	–
GPIO3_02/ **TSEC_1588_TRIG_IN2**/ EC2_GTX_CLK125	General Purpose Input/Output	AE5	IO	LV_{DD}	–
GPIO3_03/ **TSEC_1588_ALARM_OUT1**/ EC2_RX_CLK	General Purpose Input/Output	AF5	IO	LV_{DD}	–
GPIO3_04/ **TSEC_1588_ALARM_OUT2**/ EC2_TXD0	General Purpose Input/Output	AC7	IO	LV_{DD}	–
GPIO3_05/ **TSEC_1588_CLK_OUT**/ EC2_TXD1	General Purpose Input/Output	AD7	IO	LV_{DD}	–
GPIO3_06/ **TSEC_1588_PULSE_OUT1**/ EC2_RXD2	General Purpose Input/Output	AE6	IO	LV_{DD}	–
GPIO3_07/ **TSEC_1588_PULSE_OUT2**/ EC2_TX_EN	General Purpose Input/Output	AD8	IO	LV_{DD}	–
GPIO3_08/**EMI1_MDC**	General Purpose Input/Output	AH3	IO	$L1V_{DD}$	–
GPIO3_09/**EMI1_MDIO**	General Purpose Input/Output	AH4	IO	$L1V_{DD}$	–
GPIO3_11/**EC1_TXD3**	General Purpose Input/Output	AC3	IO	$L1V_{DD}$	–
GPIO3_12/**EC1_TXD2**	General Purpose Input/Output	AD3	IO	$L1V_{DD}$	–
GPIO3_13/**EC1_TXD1**	General Purpose Input/Output	AE4	IO	$L1V_{DD}$	–
GPIO3_14/**EC1_TXD0**	General Purpose Input/Output	AE3	IO	$L1V_{DD}$	–
GPIO3_15/**EC1_TX_EN**	General Purpose Input/Output	AF4	IO	$L1V_{DD}$	–
GPIO3_16/**EC1_GTX_CLK**	General Purpose Input/Output	AF3	IO	$L1V_{DD}$	–
GPIO3_17/**EC1_GTX_CLK125**	General Purpose Input/Output	AG3	IO	$L1V_{DD}$	–
GPIO3_18/**EC1_RXD3**	General Purpose Input/Output	AD2	IO	$L1V_{DD}$	–
GPIO3_19/**EC1_RXD2**	General Purpose Input/Output	AE1	IO	$L1V_{DD}$	–
GPIO3_20/**EC1_RXD1**	General Purpose Input/Output	AF1	IO	$L1V_{DD}$	–
GPIO3_21/**EC1_RXD0**	General Purpose Input/Output	AF2	IO	$L1V_{DD}$	–
GPIO3_22/**EC1_RX_DV**	General Purpose Input/Output	AG2	IO	$L1V_{DD}$	–
GPIO3_23/**EC1_RX_CLK**	General Purpose Input/Output	AD1	IO	$L1V_{DD}$	–
GPIO3_24/EC2_RX_DV	General Purpose Input/Output	AF8	IO	LV_{DD}	14
GPIO3_25/EC2_RXD0	General Purpose Input/Output	AE8	IO	LV_{DD}	–
GPIO3_26/EC2_TXD3	General Purpose Input/Output	AC6	IO	LV_{DD}	–
GPIO3_27/EC2_RXD3	General Purpose Input/Output	AH6	IO	LV_{DD}	–
GPIO3_28/EC2_RXD1	General Purpose Input/Output	AH7	IO	LV_{DD}	–
GPIO4_02/**IIC4_SCL**/EVT5_B/ DIU_HSYNC	General Purpose Input/Output	AA3	IO	DV_{DD}	–
GPIO4_03/**IIC4_SDA**/EVT6_B/ DIU_VSYNC	General Purpose Input/Output	AB3	IO	DV_{DD}	–
GPIO4_10/**TDMA_RXD**/ UC1_RXD7/DIU_D0	General Purpose Input/Output	U2	IO	DV_{DD}	–
GPIO4_11/**TDMA_RSYNC**/ UC1_CTSB_RXDV/DIU_D1	General Purpose Input/Output	U1	IO	DV_{DD}	–
GPIO4_12/**TDMA_TXD**/ UC1_TXD7/DIU_D2	General Purpose Input/Output	T1	IO	DV_{DD}	–

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GPIO4_13/**TDMA_TSYNC**/ UC1_RTSB_TXEN/DIU_D3	General Purpose Input/Output	R1	IO	DV_{DD}	–
GPIO4_14/**TDMA_RQ**/ UC1_CDB_RXER/DIU_D4	General Purpose Input/Output	R2	IO	DV_{DD}	–
GPIO4_15/**CLK09**/BRGO2/ DIU_D10	General Purpose Input/Output	P4	IO	DV_{DD}	–
GPIO4_16/**CLK11**/BRGO4/ DIU_DE	General Purpose Input/Output	N4	IO	DV_{DD}	–
GPIO4_17/**TDMB_RXD**/ UC3_RXD7/DIU_D5	General Purpose Input/Output	U4	IO	DV_{DD}	–
GPIO4_18/**TDMB_RSYNC**/ UC3_CTSB_RXDV/DIU_D6	General Purpose Input/Output	T3	IO	DV_{DD}	–
GPIO4_19/**TDMB_TXD**/ UC3_TXD7/DIU_D7	General Purpose Input/Output	T4	IO	DV_{DD}	–
GPIO4_20/**TDMB_TSYNC**/ UC3_RTSB_TXEN/DIU_D8	General Purpose Input/Output	R3	IO	DV_{DD}	–
GPIO4_21/**TDMB_RQ**/ UC3_CDB_RXER/DIU_D9	General Purpose Input/Output	R4	IO	DV_{DD}	–
GPIO4_22/**CLK10**/BRGO3/ DIU_D11	General Purpose Input/Output	P3	IO	DV_{DD}	–
GPIO4_23/**CLK12**/BRGO1/ DIU_CLK_OUT	General Purpose Input/Output	M4	IO	DV_{DD}	–
GPIO4_24/**SDHC_CD_B**/ IIC3_SCL	General Purpose Input/Output	L5	IO	CV_{DD}	–
GPIO4_25/**SDHC_WP**/ IIC3_SDA	General Purpose Input/Output	M5	IO	CV_{DD}	–
GPIO4_27/**IIC2_SCL**	General Purpose Input/Output	V3	IO	DV_{DD}	–
GPIO4_28/**IIC2_SDA**	General Purpose Input/Output	Y3	IO	DV_{DD}	–
Power and Ground Signals					
GND001	GND	A2	–	–	–
GND002	GND	A20	–	–	–
GND003	GND	A27	–	–	–
GND004	GND	B1	–	–	–
GND005	GND	B4	–	–	–
GND006	GND	B7	–	–	–
GND007	GND	B10	–	–	–
GND008	GND	B13	–	–	–
GND009	GND	B16	–	–	–
GND010	GND	B19	–	–	–
GND011	GND	B23	–	–	–
GND012	GND	B25	–	–	–
GND013	GND	B28	–	–	–
GND014	GND	C22	–	–	–
GND015	GND	C26	–	–	–
GND016	GND	D2	–	–	–
GND017	GND	D20	–	–	–
GND018	GND	D21	–	–	–
GND019	GND	D24	–	–	–
GND020	GND	E5	–	–	–
GND021	GND	E7	–	–	–
GND022	GND	E10	–	–	–

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND023	GND	E13	–	–	–
GND024	GND	E16	–	–	–
GND025	GND	E19	–	–	–
GND026	GND	E22	–	–	–
GND027	GND	E26	–	–	–
GND028	GND	F15	–	–	–
GND029	GND	F24	–	–	–
GND030	GND	G7	–	–	–
GND031	GND	G13	–	–	–
GND032	GND	G16	–	–	–
GND033	GND	G22	–	–	–
GND034	GND	G26	–	–	–
GND035	GND	H7	–	–	–
GND036	GND	H8	–	–	–
GND037	GND	H9	–	–	–
GND038	GND	H10	–	–	–
GND039	GND	H11	–	–	–
GND040	GND	H12	–	–	–
GND041	GND	H13	–	–	–
GND042	GND	H14	–	–	–
GND043	GND	H15	–	–	–
GND044	GND	H16	–	–	–
GND045	GND	H17	–	–	–
GND046	GND	H18	–	–	–
GND047	GND	H19	–	–	–
GND048	GND	H20	–	–	–
GND049	GND	H24	–	–	–
GND050	GND	J7	–	–	–
GND051	GND	J22	–	–	–
GND052	GND	J26	–	–	–
GND053	GND	K2	–	–	–
GND054	GND	K5	–	–	–
GND055	GND	K6	–	–	–
GND056	GND	K7	–	–	–
GND057	GND	K12	–	–	–
GND058	GND	K14	–	–	–
GND059	GND	K16	–	–	–
GND060	GND	K18	–	–	–
GND061	GND	K20	–	–	–
GND062	GND	K24	–	–	–
GND063	GND	L7	–	–	–
GND064	GND	L9	–	–	–
GND065	GND	L11	–	–	–

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND066	GND	L13	–	–	–
GND067	GND	L15	–	–	–
GND068	GND	L17	–	–	–
GND069	GND	L19	–	–	–
GND070	GND	L22	–	–	–
GND071	GND	L26	–	–	–
GND072	GND	M7	–	–	–
GND073	GND	M10	–	–	–
GND074	GND	M12	–	–	–
GND075	GND	M14	–	–	–
GND076	GND	M16	–	–	–
GND077	GND	M18	–	–	–
GND078	GND	M20	–	–	–
GND079	GND	M24	–	–	–
GND080	GND	N2	–	–	–
GND081	GND	N5	–	–	–
GND082	GND	N7	–	–	–
GND083	GND	N9	–	–	–
GND084	GND	N11	–	–	–
GND085	GND	N13	–	–	–
GND086	GND	N15	–	–	–
GND087	GND	N17	–	–	–
GND088	GND	N19	–	–	–
GND089	GND	N22	–	–	–
GND090	GND	N26	–	–	–
GND091	GND	P7	–	–	–
GND092	GND	P10	–	–	–
GND093	GND	P12	–	–	–
GND094	GND	P14	–	–	–
GND095	GND	P16	–	–	–
GND096	GND	P18	–	–	–
GND097	GND	P20	–	–	–
GND098	GND	P24	–	–	–
GND099	GND	R7	–	–	–
GND100	GND	R9	–	–	–
GND101	GND	R11	–	–	–
GND102	GND	R13	–	–	–
GND103	GND	R15	–	–	–
GND104	GND	R17	–	–	–
GND105	GND	R19	–	–	–
GND106	GND	R22	–	–	–
GND107	GND	R26	–	–	–
GND108	GND	T2	–	–	–

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND109	GND	T5	–	–	–
GND110	GND	T7	–	–	–
GND111	GND	T10	–	–	–
GND112	GND	T12	–	–	–
GND113	GND	T14	–	–	–
GND114	GND	T16	–	–	–
GND115	GND	T18	–	–	–
GND116	GND	T20	–	–	–
GND117	GND	T22	–	–	–
GND118	GND	T26	–	–	–
GND119	GND	U7	–	–	–
GND120	GND	U9	–	–	–
GND121	GND	U11	–	–	–
GND122	GND	U13	–	–	–
GND123	GND	U15	–	–	–
GND124	GND	U17	–	–	–
GND125	GND	U19	–	–	–
GND126	GND	U24	–	–	–
GND127	GND	V7	–	–	–
GND128	GND	V10	–	–	–
GND129	GND	V12	–	–	–
GND130	GND	V14	–	–	–
GND131	GND	V16	–	–	–
GND132	GND	V18	–	–	–
GND133	GND	V20	–	–	–
GND134	GND	V22	–	–	–
GND135	GND	V26	–	–	–
GND136	GND	W2	–	–	–
GND137	GND	W5	–	–	–
GND138	GND	W7	–	–	–
GND139	GND	W9	–	–	–
GND140	GND	W11	–	–	–
GND141	GND	W13	–	–	–
GND142	GND	W24	–	–	–
GND143	GND	Y7	–	–	–
GND144	GND	Y10	–	–	–
GND145	GND	Y12	–	–	–
GND146	GND	Y22	–	–	–
GND147	GND	Y26	–	–	–
GND148	GND	AA7	–	–	–
GND149	GND	AA11	–	–	–
GND150	GND	AA24	–	–	–
GND151	GND	AB2	–	–	–

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND152	GND	AB5	–	–	–
GND153	GND	AB7	–	–	–
GND154	GND	AB22	–	–	–
GND155	GND	AB26	–	–	–
GND156	GND	AC24	–	–	–
GND157	GND	AC26	–	–	–
GND158	GND	AD4	–	–	–
GND159	GND	AD6	–	–	–
GND160	GND	AD22	–	–	–
GND161	GND	AE2	–	–	–
GND162	GND	AE24	–	–	–
GND163	GND	AE26	–	–	–
GND164	GND	AF9	–	–	–
GND165	GND	AF21	–	–	–
GND166	GND	AG1	–	–	–
GND167	GND	AG4	–	–	–
GND168	GND	AG6	–	–	–
GND169	GND	AG22	–	–	–
GND170	GND	AG23	–	–	–
GND171	GND	AG26	–	–	–
GND172	GND	AH2	–	–	–
USB_AGND01	USB PHY Transceiver GND	E1	–	–	–
USB_AGND02	USB PHY Transceiver GND	E2	–	–	–
USB_AGND03	USB PHY Transceiver GND	E3	–	–	–
USB_AGND04	USB PHY Transceiver GND	F3	–	–	–
USB_AGND05	USB PHY Transceiver GND	G1	–	–	–
USB_AGND06	USB PHY Transceiver GND	G2	–	–	–
USB_AGND07	USB PHY Transceiver GND	G3	–	–	–
USB_AGND08	USB PHY Transceiver GND	G5	–	–	–
USB_AGND09	USB PHY Transceiver GND	H3	–	–	–
USB_AGND10	USB PHY Transceiver GND	J1	–	–	–
USB_AGND11	USB PHY Transceiver GND	J2	–	–	–
USB_AGND12	USB PHY Transceiver GND	J3	–	–	–
SD_GND01	Serdes core logic GND	Y14	–	–	–
SD_GND02	Serdes core logic GND	Y16	–	–	–
SD_GND03	Serdes core logic GND	Y17	–	–	–
SD_GND04	Serdes core logic GND	Y18	–	–	–
SD_GND05	Serdes core logic GND	AA13	–	–	–
SD_GND06	Serdes core logic GND	AA15	–	–	–
SD_GND07	Serdes core logic GND	AA16	–	–	–
SD_GND08	Serdes core logic GND	AA17	–	–	–
SD_GND09	Serdes core logic GND	AA19	–	–	–
SD_GND10	Serdes core logic GND	AA20	–	–	–

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD_GND11	Serdes core logic GND	AA21	–	–	–
SD_GND12	Serdes core logic GND	AB13	–	–	–
SD_GND13	Serdes core logic GND	AB17	–	–	–
SD_GND14	Serdes core logic GND	AB21	–	–	–
SD_GND15	Serdes core logic GND	AC13	–	–	–
SD_GND16	Serdes core logic GND	AC14	–	–	–
SD_GND17	Serdes core logic GND	AC16	–	–	–
SD_GND18	Serdes core logic GND	AC17	–	–	–
SD_GND19	Serdes core logic GND	AC19	–	–	–
SD_GND20	Serdes core logic GND	AC20	–	–	–
SD_GND21	Serdes core logic GND	AD15	–	–	–
SD_GND22	Serdes core logic GND	AD18	–	–	–
SD_GND23	Serdes core logic GND	AD21	–	–	–
SD_GND24	Serdes core logic GND	AE15	–	–	–
SD_GND25	Serdes core logic GND	AE18	–	–	–
SD_GND26	Serdes core logic GND	AE21	–	–	–
SD_GND27	Serdes core logic GND	AF15	–	–	–
SD_GND28	Serdes core logic GND	AF16	–	–	–
SD_GND29	Serdes core logic GND	AF17	–	–	–
SD_GND30	Serdes core logic GND	AF18	–	–	–
SD_GND31	Serdes core logic GND	AF19	–	–	–
SD_GND32	Serdes core logic GND	AF20	–	–	–
SD_GND33	Serdes core logic GND	AG15	–	–	–
SD_GND34	Serdes core logic GND	AG18	–	–	–
SD_GND35	Serdes core logic GND	AG21	–	–	–
SD_GND36	Serdes core logic GND	AH15	–	–	–
SD_GND37	Serdes core logic GND	AH18	–	–	–
SD_GND38	Serdes core logic GND	AH21	–	–	–
SENSEGND	GND Sense pin	G20	–	–	–
SENSEGNDC	GND Sense pin	AB10	–	–	–
O1VDD1	General I/O supply - Always on	J11	–	$O1V_{DD}$	–
O1VDD2	General I/O supply - Always on	J12	–	$O1V_{DD}$	–
O1VDD3	General I/O supply - Always on	J13	–	$O1V_{DD}$	–
OVDD1	General I/O supply - Switchable	J14	–	OV_{DD}	–
OVDD2	General I/O supply - Switchable	J15	–	OV_{DD}	–
OVDD3	General I/O supply - Switchable	J16	–	OV_{DD}	–
OVDD4	General I/O supply - Switchable	J17	–	OV_{DD}	–
OVDD5	General I/O supply - Switchable	J18	–	OV_{DD}	–
OVDD6	General I/O supply - Switchable	J19	–	OV_{DD}	–
DVDD1	UART/I2C supply - Switchable	N8	–	DV_{DD}	–
DVDD2	UART/I2C supply - Switchable	P8	–	DV_{DD}	–
DVDD3	UART/I2C supply - Switchable	R8	–	DV_{DD}	–

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
CVDD	SPI supply - Switchable	M8	–	CV_{DD}	–
EVDD	eSDHC supply - switchable	L8	–	EV_{DD}	–
L1VDD1	Ethernet controller 1 and GPIO supply- Always ON	T8	–	$L1V_{DD}$	–
L1VDD2	Ethernet controller 1 and GPIO supply- Always ON	U8	–	$L1V_{DD}$	–
LVDD1	1588/ Ethernet controller 2/ GPIO supply- Switchable	V8	–	LV_{DD}	–
LVDD2	1588/ Ethernet controller 2/ GPIO supply- Switchable	W8	–	LV_{DD}	–
TVDD	1.2 V supply for MDIO interface for 10G Ethernet (EC2)	T6	–	TV_{DD}	–
G1VDD01	DDR supply - Switchable	D27	–	$G1V_{DD}$	–
G1VDD02	DDR supply - Switchable	F27	–	$G1V_{DD}$	–
G1VDD03	DDR supply - Switchable	H27	–	$G1V_{DD}$	–
G1VDD04	DDR supply - Switchable	K21	–	$G1V_{DD}$	–
G1VDD05	DDR supply - Switchable	K27	–	$G1V_{DD}$	–
G1VDD06	DDR supply - Switchable	L21	–	$G1V_{DD}$	–
G1VDD07	DDR supply - Switchable	M21	–	$G1V_{DD}$	–
G1VDD08	DDR supply - Switchable	M27	–	$G1V_{DD}$	–
G1VDD09	DDR supply - Switchable	N21	–	$G1V_{DD}$	–
G1VDD10	DDR supply - Switchable	P21	–	$G1V_{DD}$	–
G1VDD11	DDR supply - Switchable	P27	–	$G1V_{DD}$	–
G1VDD12	DDR supply - Switchable	R21	–	$G1V_{DD}$	–
G1VDD13	DDR supply - Switchable	T21	–	$G1V_{DD}$	–
G1VDD14	DDR supply - Switchable	U21	–	$G1V_{DD}$	–
G1VDD15	DDR supply - Switchable	U27	–	$G1V_{DD}$	–
G1VDD16	DDR supply - Switchable	W27	–	$G1V_{DD}$	–
G1VDD17	DDR supply - Switchable	AA27	–	$G1V_{DD}$	–
G1VDD18	DDR supply - Switchable	AD27	–	$G1V_{DD}$	–
G1VDD19	DDR supply - Switchable	AF27	–	$G1V_{DD}$	–
S1VDD1	SerDes1 core logic supply - Switchable	W15	–	$S1V_{DD}$	–
S1VDD2	SerDes1 core logic supply - Switchable	W16	–	$S1V_{DD}$	–
S1VDD3	SerDes1 core logic supply - Switchable	W17	–	$S1V_{DD}$	–
S1VDD4	SerDes1 core logic supply - Switchable	W18	–	$S1V_{DD}$	–
S1VDD5	SerDes1 core logic supply - Switchable	W19	–	$S1V_{DD}$	–
S1VDD6	SerDes1 core logic supply - Switchable	W20	–	$S1V_{DD}$	–
S1VDD7	SerDes1 core logic supply - Switchable	Y13	–	$S1V_{DD}$	–
X1VDD1	SerDes1 transceiver supply - Switchable	AC12	–	$X1V_{DD}$	–

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
X1VDD2	SerDes1 transceiver supply - Switchable	AC15	–	$X1V_{DD}$	–
X1VDD3	SerDes1 transceiver supply - Switchable	AC18	–	$X1V_{DD}$	–
X1VDD4	SerDes1 transceiver supply - Switchable	AC21	–	$X1V_{DD}$	–
FA_VL	Reserved	G18	–	FA_VL	15
PROG_MTR	Reserved	F11	–	PROG_MTR	15
PROG_SFP	SFP Fuse Programming Override supply	F12	–	PROG_SFP	–
TH_VDD	Thermal Monitor Unit supply	G9	–	TH_V_{DD}	–
VDD01	Supply for cores and platform - Switchable	K15	–	V_{DD}	–
VDD02	Supply for cores and platform - Switchable	K17	–	V_{DD}	–
VDD03	Supply for cores and platform - Switchable	K19	–	V_{DD}	–
VDD04	Supply for cores and platform - Switchable	L12	–	V_{DD}	–
VDD05	Supply for cores and platform - Switchable	L14	–	V_{DD}	–
VDD06	Supply for cores and platform - Switchable	L16	–	V_{DD}	–
VDD07	Supply for cores and platform - Switchable	L18	–	V_{DD}	–
VDD08	Supply for cores and platform - Switchable	M13	–	V_{DD}	–
VDD09	Supply for cores and platform - Switchable	M15	–	V_{DD}	–
VDD10	Supply for cores and platform - Switchable	M17	–	V_{DD}	–
VDD11	Supply for cores and platform - Switchable	N12	–	V_{DD}	–
VDD12	Supply for cores and platform - Switchable	N14	–	V_{DD}	–
VDD13	Supply for cores and platform - Switchable	N16	–	V_{DD}	–
VDD14	Supply for cores and platform - Switchable	N18	–	V_{DD}	–
VDD15	Supply for cores and platform - Switchable	P11	–	V_{DD}	–
VDD16	Supply for cores and platform - Switchable	P13	–	V_{DD}	–
VDD17	Supply for cores and platform - Switchable	P15	–	V_{DD}	–
VDD18	Supply for cores and platform - Switchable	P17	–	V_{DD}	–
VDD19	Supply for cores and platform - Switchable	R12	–	V_{DD}	–
VDD20	Supply for cores and platform - Switchable	R14	–	V_{DD}	–

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
VDD21	Supply for cores and platform - Switchable	R16	–	V_{DD}	–
VDD22	Supply for cores and platform - Switchable	R18	–	V_{DD}	–
VDD23	Supply for cores and platform - Switchable	T13	–	V_{DD}	–
VDD24	Supply for cores and platform - Switchable	T15	–	V_{DD}	–
VDD25	Supply for cores and platform - Switchable	T17	–	V_{DD}	–
VDD26	Supply for cores and platform - Switchable	U14	–	V_{DD}	–
VDD27	Supply for cores and platform - Switchable	U16	–	V_{DD}	–
VDD28	Supply for cores and platform - Switchable	U18	–	V_{DD}	–
VDD29	Supply for cores and platform - Switchable	V13	–	V_{DD}	–
VDD30	Supply for cores and platform - Switchable	V15	–	V_{DD}	–
VDD31	Supply for cores and platform - Switchable	V17	–	V_{DD}	–
VDDC01	Always ON supply	K11	–	$V_{DD}C$	–
VDDC02	Always ON supply	K13	–	$V_{DD}C$	–
VDDC03	Always ON supply	L10	–	$V_{DD}C$	–
VDDC04	Always ON supply	M11	–	$V_{DD}C$	–
VDDC05	Always ON supply	N10	–	$V_{DD}C$	–
VDDC06	Always ON supply	R10	–	$V_{DD}C$	–
VDDC07	Always ON supply	T11	–	$V_{DD}C$	–
VDDC08	Always ON supply	U10	–	$V_{DD}C$	–
VDDC09	Always ON supply	U12	–	$V_{DD}C$	–
VDDC10	Always ON supply	V11	–	$V_{DD}C$	–
VDDC11	Always ON supply	W10	–	$V_{DD}C$	–
VDDC12	Always ON supply	W12	–	$V_{DD}C$	–
AVDD_CGA1	e5501 Cluster Group A PLL1 supply (SDHC /Cores fed through this) - Switchable	G11	–	AVDD_CGA1	–
AVDD_PLAT	Platform PLL supply	G10	–	AVDD_PLAT	–
AVDD_D1	DDR1 PLL supply	E20	–	AVDD_D1	–
AVDD_SD1_PLL1	SerDes1 PLL 1 supply	AB16	–	AVDD_SD1_PLL1	–
AVDD_SD1_PLL2	SerDes1 PLL 2 supply	AB20	–	AVDD_SD1_PLL2	–
SENSEVDD	Vdd Sense pin - Switchable	G19	–	SENSEVDD	–
SENSEVDDC	Vddc Sense pin - Always ON	AB9	–	SENSEVDDC	–
USB_HVDD1	USB PHY Transceiver 3.3V Supply - "Optionally Switchable or Always ON"	J8	–	USB_HV_{DD}	–
USB_HVDD2	USB PHY Transceiver 3.3V Supply - "Optionally Switchable or Always ON"	K8	–	USB_HV_{DD}	–
USB_OVDD1	USB PHY Transceiver 1.8V Supply - "Optionally Switchable or Always ON"	J9	–	USB_OV_{DD}	–

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
USB_OVDD2	USB PHY Transceiver 1.8V Supply - "Optionally Switchable or Always ON"	J10	–	USB_OV_{DD}	–
USB_SVDD1	USB PHY Analog 1.0V Supply - "Optionally Switchable or Always ON"	K9	–	USB_SV_{DD}	–
USB_SVDD2	USB PHY Analog 1.0V Supply - "Optionally Switchable or Always ON"	K10	–	USB_SV_{DD}	–
No Connection Pins					
NC_AA10	No Connection	AA10	–	–	12
NC_AA5	No Connection	AA5	–	–	12
NC_AA6	No Connection	AA6	–	–	12
NC_AA8	No Connection	AA8	–	–	12
NC_AA9	No Connection	AA9	–	–	12
NC_AB1	No Connection	AB1	–	–	12
NC_AB11	No Connection	AB11	–	–	12
NC_AB12	No Connection	AB12	–	–	12
NC_AB8	No Connection	AB8	–	–	12
NC_AC1	No Connection	AC1	–	–	12
NC_AC10	No Connection	AC10	–	–	12
NC_AC11	No Connection	AC11	–	–	12
NC_AC2	No Connection	AC2	–	–	12
NC_AC4	No Connection	AC4	–	–	12
NC_AC9	No Connection	AC9	–	–	12
NC_AD10	No Connection	AD10	–	–	12
NC_AD11	No Connection	AD11	–	–	12
NC_AD12	No Connection	AD12	–	–	12
NC_AD13	No Connection	AD13	–	–	12
NC_AD14	No Connection	AD14	–	–	12
NC_AD5	No Connection	AD5	–	–	12
NC_AD9	No Connection	AD9	–	–	12
NC_AE10	No Connection	AE10	–	–	12
NC_AE11	No Connection	AE11	–	–	12
NC_AE12	No Connection	AE12	–	–	12
NC_AE13	No Connection	AE13	–	–	12
NC_AE14	No Connection	AE14	–	–	12
NC_AE7	No Connection	AE7	–	–	12
NC_AE9	No Connection	AE9	–	–	12
NC_AF10	No Connection	AF10	–	–	12
NC_AF11	No Connection	AF11	–	–	12
NC_AF12	No Connection	AF12	–	–	12
NC_AF13	No Connection	AF13	–	–	12
NC_AF14	No Connection	AF14	–	–	12
NC_AF6	No Connection	AF6	–	–	12

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
NC_AF7	No Connection	AF7	–	–	12
NC_AG10	No Connection	AG10	–	–	12
NC_AG11	No Connection	AG11	–	–	12
NC_AG12	No Connection	AG12	–	–	12
NC_AG13	No Connection	AG13	–	–	12
NC_AG14	No Connection	AG14	–	–	12
NC_AG5	No Connection	AG5	–	–	12
NC_AG7	No Connection	AG7	–	–	12
NC_AG8	No Connection	AG8	–	–	12
NC_AG9	No Connection	AG9	–	–	12
NC_AH10	No Connection	AH10	–	–	12
NC_AH11	No Connection	AH11	–	–	12
NC_AH12	No Connection	AH12	–	–	12
NC_AH13	No Connection	AH13	–	–	12
NC_AH14	No Connection	AH14	–	–	12
NC_AH27	No Connection	AH27	–	–	12
NC_AH5	No Connection	AH5	–	–	12
NC_AH8	No Connection	AH8	–	–	12
NC_AH9	No Connection	AH9	–	–	12
NC_C17	No Connection	C17	–	–	12
NC_C19	No Connection	C19	–	–	12
NC_D1	No Connection	D1	–	–	12
NC_D18	No Connection	D18	–	–	12
NC_D4	No Connection	D4	–	–	12
NC_D5	No Connection	D5	–	–	12
NC_DET	No Connection	AG28	–	–	12
NC_E17	No Connection	E17	–	–	12
NC_E9	No Connection	E9	–	–	12
NC_F21	No Connection	F21	–	–	12
NC_F8	No Connection	F8	–	–	12
NC_G12	No Connection	G12	–	–	12
NC_G17	No Connection	G17	–	–	12
NC_G6	No Connection	G6	–	–	12
NC_H21	No Connection	H21	–	–	12
NC_H6	No Connection	H6	–	–	12
NC_J6	No Connection	J6	–	–	12
NC_K22	No Connection	K22	–	–	12
NC_L20	No Connection	L20	–	–	12
NC_L6	No Connection	L6	–	–	12
NC_M19	No Connection	M19	–	–	12
NC_M22	No Connection	M22	–	–	12
NC_M6	No Connection	M6	–	–	12
NC_M9	No Connection	M9	–	–	12

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
NC_N20	No Connection	N20	–	–	12
NC_N6	No Connection	N6	–	–	12
NC_P19	No Connection	P19	–	–	12
NC_P22	No Connection	P22	–	–	12
NC_P5	No Connection	P5	–	–	12
NC_P6	No Connection	P6	–	–	12
NC_P9	No Connection	P9	–	–	12
NC_R20	No Connection	R20	–	–	12
NC_R5	No Connection	R5	–	–	12
NC_R6	No Connection	R6	–	–	12
NC_T19	No Connection	T19	–	–	12
NC_T9	No Connection	T9	–	–	12
NC_U20	No Connection	U20	–	–	12
NC_U22	No Connection	U22	–	–	12
NC_U5	No Connection	U5	–	–	12
NC_V19	No Connection	V19	–	–	12
NC_V2	No Connection	V2	–	–	12
NC_V21	No Connection	V21	–	–	12
NC_V5	No Connection	V5	–	–	12
NC_V9	No Connection	V9	–	–	12
NC_W14	No Connection	W14	–	–	12
NC_W21	No Connection	W21	–	–	12
NC_W3	No Connection	W3	–	–	12
NC_W6	No Connection	W6	–	–	12
NC_Y11	No Connection	Y11	–	–	12
NC_Y21	No Connection	Y21	–	–	12
NC_Y5	No Connection	Y5	–	–	12
NC_Y6	No Connection	Y6	–	–	12
NC_Y8	No Connection	Y8	–	–	12
NC_Y9	No Connection	Y9	–	–	12

Notes:

1. Functionally, this pin is an output or an input, but structurally it is an I/O because it either sample configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.
2. During reset, this output signal is actively driven rather than being tri-stated
3. MDIC[0] is grounded through a 162Ω precision 1% resistor and MDIC[1] is connected to $GV1_{DD}$ through a 162Ω precision 1% resistor. For either full or half driver strength calibration of DDR IOs, use the same MDIC resistor value of 162Ω. Memory controller register setting can be used to determine automatic calibration is done to full or half drive strength. These pins are used for automatic calibration of the DDR3L/DDR4 IOs. The MDIC[0:1] pins must be connected to 162Ω precision 1% resistors.
4. This pin is a reset configuration pin. It has a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the processor is in its reset state. This pull-up is designed such that it can be overpowered by an external 4.7 kΩ resistor. However, if the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, a pull-up or active driver is needed.
5. Pin must **NOT** be pulled down during power-on reset. This pin may be pulled up, driven high, or if there are any externally connected devices, left in tristate. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.
6. Recommend that a weak pull-up resistor (2-10 kΩ) be placed on this pin to the respective power supply.

7. This pin is an open-drain signal.
8. Recommend that a weak pull-up resistor (1 kΩ) be placed on this pin to the respective power supply.
9. This pin has a weak (~20 kΩ) internal pull-up P-FET that is always enabled.
10. These are test signals for factory use only and must be pulled up (100Ω to 1-kΩ) to the respective power supply for normal operation.
11. This pin requires a 200Ω pull-up to respective power-supply.
12. Do not connect. These pins should be left floating.
13. These pins must be pulled up to 1.2V through a 180Ω ± 1% resistor for MDC and a 330Ω ± 1% resistor for MDIO.
14. This pin requires an external 1-kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.
15. These pins must be pulled to ground (GND).
16. This pin requires a 698Ω pull-up to respective power-supply.
17. These pins should be tied to ground if the diode is not utilized for temperature monitoring.
18. This pin should be connected to ground through 2-10kΩ resistor when not used.
19. This pin should be connected to ground through 2-10kΩ resistor when SYSCLK input is used as system clock.
20. This pin should be connected to GND through a 10kΩ ± 0.1% resistor with a low temperature coefficient of ≤ 25ppm/°C for bias generation
21. This pin has a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the processor is in its reset state. This pin should have an optional pull down resistor on board. This is required to support DIFF_SYSCLK/DIFF_SYSCLK_B
22. This pin should not be sampled until PORESET_B gets deasserted.
23. This pin must be pulled to O1VDD through a 100-ohm to 1k-ohm resistor for a two core T1024 and tied to ground for a single core T1014 device.
24. External “CLK12” pin is connected internally to both CLK12 and CLK8 pins of QE.
25. The alternate signal in DDR4 configuration is mentioned in T1024 Reference Manual.
26. PORESET_B should be asserted zero during the JTAG Boundry scan operation, and is required to be controllable on board.
27. This pin requires a pull-up to the respective power supply so as to meet the timing requirements in Table 24

Warning
See "Connection recommendations " for additional details on properly connecting these pins for specific applications.

3 ELECTRICAL CHARACTERISTICS

This section provides the AC and DC electrical specifications for the chip. The chip is currently targeted to these specifications, some of which are independent of the I/O cell but are included for a more complete reference. These are not purely I/O buffer design specifications.

3.1 Overall DC electrical characteristics

This section describes the ratings, conditions, and other characteristics.

3.1.1 Absolute maximum ratings

This table provides the absolute maximum ratings for power supply voltage levels.

Table 2: Absolute maximum ratings1

Characteristic		Symbol	Max Value	Unit	Notes
Core and platform supply voltage		V_{DD}	-0.3 to 1.08	V	9, 12
Always ON supply voltage		V_{DDC}	-0.3 to 1.08	V	-
PLL supply voltage (core PLL/eSDHC, platform, DDR)		AV_{DD}_CGA1 AV_{DD}_PLAT AV_{DD}_D1	-0.3 to 1.98	V	11, 12
PLL supply voltage (SerDes, filtered from $X1V_{DD}$)		AVDD_SD1_PLL1 AVDD_SD1_PLL2	-0.3 to 1.48	V	12
SFP Fuse Programming		PROG_SFP	-0.3 to 1.98	V	12
Thermal monitor unit supply		TH_V_{DD}	-0.3 to 1.98	V	12
MPIC, GPIO, system control and power management, clocking, debug, IFC, DDRCLK supply, and JTAG I/O voltage		OV_{DD} $O1V_{DD}$	-0.3 to 1.98	V	12
DUART, I^2C, QE-TDM, QE, MPIC, DIU		DV_{DD}	-0.3 to 2.75 -0.3 to 1.98 -0.3 to 3.63	V	12
eSPI, SDHC_WP, SDHC_CD, SDHC_DAT[4:7]		CV_{DD}	-0.3 to 1.98 -0.3 to 3.63	V	12
eSDHC, DMA		EV_{DD}	-0.3 to 1.98 -0.3 to 3.63	V	12
DDR4 and DDR3L DRAM I/O voltage	DDR4	$G1V_{DD}$	-0.3 to 1.26	V	12
	DDR3L		-0.3 to 1.42		
Main power supply for internal circuitry of SerDes and pad power supply for SerDes receivers		$S1V_{DD}$	-0.3 to 1.08	V	12
Pad power supply for SerDes transmitter		$X1V_{DD}$	-0.3 to 1.45	V	12
Ethernet interface 2, 1588, GPIO		LV_{DD}	-0.3 to 1.98 -0.3 to 2.75	V	12
Ethernet interface 1, Ethernet management interface 1 (EMI1), GPIO		$L1V_{DD}$	-0.3 to 1.98 -0.3 to 2.75	V	12
Ethernet management interface 2 (EMI2) I/O voltage		TV_{DD}	-0.3 to 1.32 -0.3 to 1.98	V	10, 12
USB PHY Transceiver supply voltage		USB_HV_{DD}	-0.3 to 3.63	V	12
		USB_OV_{DD}	-0.3 to 1.98	V	12
USB PHY Analog supply voltage		USB_SV_{DD}	-0.3 to 1.08	V	12
Storage temperature range		T_{STG}	-55 to 150	°C	-

Notes:

Refer to the notes in Table 3.

This table provides the absolute maximum ratings for input signal voltage levels.

Table 3: Absolute maximum ratings for input signal voltage levels (1)

Interface Input signals	Symbol	Max DC V_input range	Max undershoot and overshoot voltage range	Unit	Notes
DDR4 and DDR3L DRAM signals	MV_{IN}	GND to ($G1V_{DD}$ x 1.05)	-0.3 to ($G1V_{DD}$ x 1.1)	V	1, 14
DDR3L DRAM reference	$D1\_MV_{REF}$	GND to ($G1V_{DD}$/2 x 1.05)	-0.3 to ($G1V_{DD}$/2 x 1.1)	V	5
Ethernet signals	LV_{IN} $LV1_{IN}$	GND to (LnV_{DD} x 1.1)	-0.3 to (LnV_{DD} x 1.15)	V	4, 5
MPIC, GPIO, system control and power management, clocking, debug, IFC, DDRCLK supply, and JTAG I/O voltage	OV_{IN} $O1V_{IN}$	GND to (OnV_{DD} x 1.1)	-0.3 to (OnV_{DD} x 1.15)	V	3, 5
eSDHC, DMA signals	EV_{IN}	GND to (EV_{DD} x 1.1)	-0.3 to (EV_{DD} x 1.15)	V	7, 5
eSPI signals	CV_{IN}	GND to (CV_{DD} x 1.1)	-0.3 to (CV_{DD} x 1.15)	V	8, 5
DUART, I^2C, QE-TDM, MPIC, DIU	DV_{IN}	GND to (DV_{DD} x 1.1)	-0.3 to (DV_{DD} x 1.15)	V	5, 6
SerDes signals	$S1V_{IN}$	GND to ($S1V_{DD}$ x 1.05)	-0.3 to ($S1V_{DD}$ x 1.1)	V	5
USB PHY Transceiver signals	$USB\_H\ V_{IN}$	GND to (USB_HV_{DD} x 1.05)	-0.3 to (USB_HV_{DD} x 1.15)	V	5, 13
	$USB\_O\ V_{IN}$	GND to (USB_OV_{DD} x 1.1)	-0.3 to (USB_OV_{DD} x 1.15)	V	5, 13
Ethernet management interface 2 signals	$TVDD_{IN}$	GND to (TV_{DD} x 1.05)	-0.3 to (TV_{DD} x 1.1)	V	5, 13

Notes:

1. Functional operating conditions are given in Table 4. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. Caution: MVIN must not exceed G1VDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. Caution: OVIN must not exceed OVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. Caution: LVIN must not exceed LVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. (S,G,L,O,D,E,C)VIN, USBn_VIN_3P3, USBn_VIN_1P8, TVDD, and D1_MVREF may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 8.
6. Caution: DVIN must not exceed DVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
7. Caution: EVIN must not exceed EVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
8. Caution: CVIN must not exceed CVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
9. Supply voltage specified at the voltage sense pin. Voltage input pins should be regulated to provide specified voltage at the sense pin.
10. TVDD must be connected to 1.2V when Ethernet management interface 2 (EMI2) is used. When EMI2 is not used, TVDD can be connected to 1.2V or 1.8V.
11. AVDD_PLAT, AVDD_CGA1 and AVDD_D1 are measured at the input to the filter (as shown in AN4971) and not at the pin of the device.
12. Exposing device to Absolute Maximum Ratings conditions for long periods of time may affect reliability or cause permanent damage.
13. USB Overshoot or Undershoot signal time should be under 10% of signal rise time or under 2 nSec.
14. Typical DDR interface uses ODT enabled mode. For tests purposes with ODT off mode, simulation should be done first so as to make sure that the overshoot signal level at the input pin does not exceed GVDD by more than 10%. The Overshoot/ Undershoot period should comply with JEDEC standards.

3.1.2 Recommended operating conditions

This table provides the recommended operating conditions for this chip.

NOTE
The values shown are the recommended operating conditions and proper device operation outside these conditions is not guaranteed.

Table 4: Recommended operating conditions

Characteristic		Symbol	Recommended Value	Unit	Status in Deep Sleep[6]	Notes
Core and platform supply voltage		V_{DD}	1.0 ± 30 mV	V	OFF	3, 4, 5
Always ON Core and Platform supply		V_{DDC}	1.0 ± 30 mV	V	ON	3, 4, 5
PLL supply voltage (core PLL/ eSDHC, platform, DDR)		AV_{DD}_CGA1	1.8 V ± 90 mV	V	OFF	-
		AV_{DD}_PLAT			ON	
		AV_{DD}_D1			OFF	
PLL supply voltage (SerDes, filtered from $X1V_{DD}$)		AV_{DD}_SD1_PLL 1 AV_{DD}_SD1_PLL 2	1.35 V ± 67 mV	V	OFF	-
SFP fuse programming		PROG_SFP	1.8 V ± 90 mV	V	ON	2
Thermal monitor unit supply		TH_V_{DD}	1.8 V ± 90 mV	V	OFF	-
IFC, GPIO, Trust, DDRCLK supply, RTC and JTAG I/O voltage		OV_{DD}	1.8 V ± 90 mV	V	OFF	-
MPIC, GPIO, system control, debug and SYSCLK supply		$O1V_{DD}$	1.8 V ± 90 mV	V	ON	-
DUART, I^2C, MPIC, QE-TDM, DIU		DV_{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV 3.3 V ± 165 mV	V	OFF	-
eSPI, SDHC_WP, SDHC_CD, SDHC_DAT[4:7]		CVDD	3.3 V ± 165mV 1.8 V ± 90mV	V	OFF	-
eSDHC, DMA		EVDD	3.3 V ±165 mV 1.8 V ± 90 mV	V	OFF	-
DDR DRAM I/O voltage	DDR4	$G1V_{DD}$	1.2V ± 60 mV	V	OFF	-
	DDR3L		1.35 V ± 67 mV			
Main power supply for internal circuitry of SerDes and pad power supply for SerDes receivers		$S1V_{DD}$	1.0 V + 50 mV 1.0 V - 30 mV	V	OFF	-
Pad power supply for SerDes transmitters		$X1V_{DD}$	1.35 V ± 67 mV	V	OFF	-
Ethernet interface 2, 1588, GPIO		LV_{DD}	1.8 V ± 90 mV 2.5 V ± 125 mV	V	OFF	1
Ethernet interface 1, Ethernet management interface 1 (EMI1), GPIO		$L1V_{DD}$	1.8 V ± 90 mV 2.5 V ± 125 mV	V	ON	1
Ethernet management interface 2 (EMI2) I/O voltage		TV_{DD}	1.2 V ± 60 mV	V	OFF	-
USB PHY Transceiver supply voltage		USB_HV_{DD}	3.3 V ± 165 mV	V	Optionally OFF	-
		USB_OV_{DD}	1.8 V ± 90 mV	V	Optionally OFF	-
USB PHY Analog supply voltage		USB_SV_{DD}	1.0V ± 50 mV	V	Optionally OFF	3
Input voltage	DDR4 and DDR3L DRAM signals	MV_{IN}	GND to $G1V_{DD}$	V	-	-

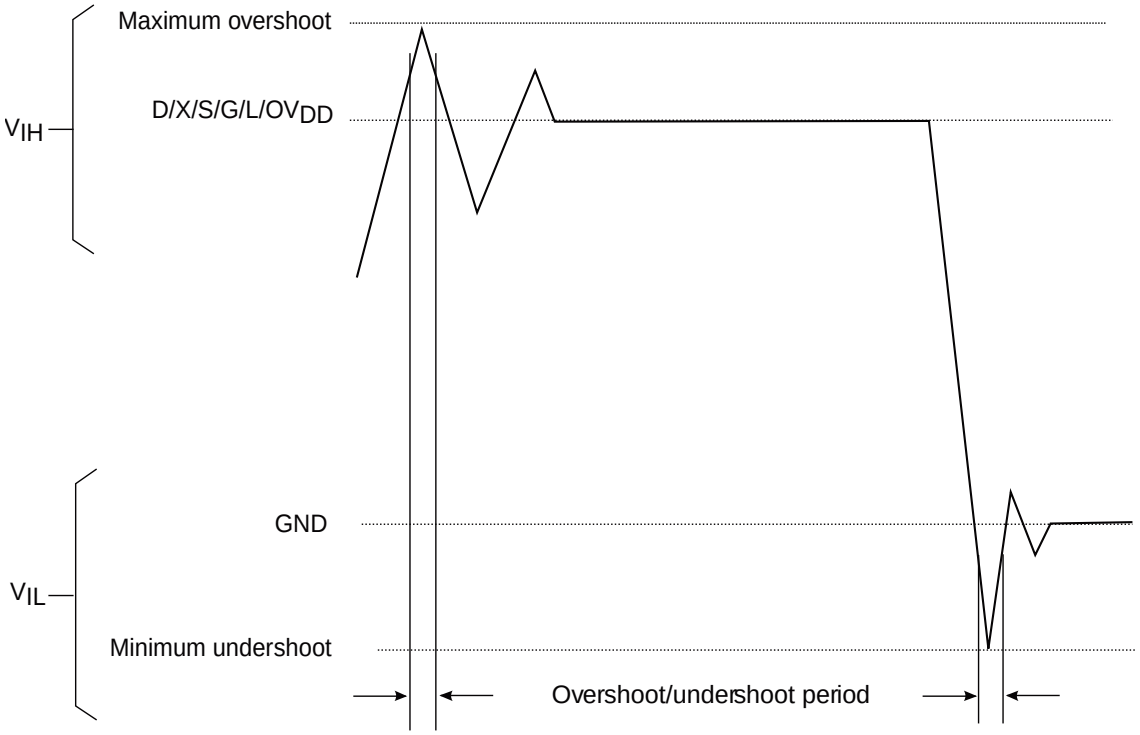
Characteristic		Symbol	Recommended Value	Unit	Status in Deep Sleep[6]	Notes
	DDR3L DRAM reference	D1_MV_{REF}	G1V_{DD}/2 ± 1%	V	-	-
	Ethernet interface, EMI1, 1588, GPIO	LV_{IN} L1V	GND to LV_{DD} GND to L1V	V	-	-
	eSDHC, eSPI, MPIC, GPIO, system control and power management, clocking, debug, IFC, DDRCLK supply, and JTAG I/O voltage	OV_{IN} O1V_{IN}	GND to OnV_{DD}	V	-	-
	DUART, I^2C, QE-TDM, MPIC, DIU	DV_{IN}	GND to DV_{DD}	V	-	-
	SerDes signals	SV_{IN}	GND to S1V_{DD}	V	-	-
	USB PHY Transceiver signals	USB_HVIN	GND to USB_HVDD	V	-	-
		USB_OVIN	GND to USB_OVDD	V	-	-
Operating temperature range	A range	T_C, T_J	T_C = -40 (min) to T = 105 (max)	°C	-	-
	F range	T_C, T_J	T_C = -40 (min) to T = 125 (max)	°C	-	-
	M range	T_C, T_J	T_C = -55 (min) to T = 125 (max)	°C	-	-
	Secure boot fuse programming	T_A, T_J	T_A = 0 (min) to T = 70 (max)	°C	-	2

Notes:

1. Selecting RGMII limits L1V_{DD}, LV_{DD} = 1.8 V or 2.5 V. L1V_{DD}, LV_{DD} should be configured at same voltage.
2. PROG_SFP must be supplied 1.8 V and the chip must operate in the specified fuse programming temperature range only during secure boot fuse programming. For all other operating conditions, PROG_SFP must be tied to GND, subject to the power sequencing constraints shown in Power sequencing.
3. Refer to Core and platform supply voltage filtering for additional information.
4. Supply voltage specified at the voltage sense pin. Voltage input pins should be regulated to provide specified voltage at the sense pin.
5. Operation at 1.1V is allowable for up to 25ms at initial power on.
6. The Power supplies designated as OFF in this column should be switched OFF during Deep Sleep and those designated as ON should not be switched OFF. There are few power supplies which can be optionally switched OFF, for more details refer to QorIQ T1024 Reference Manual.

This figure shows the undershoot and overshoot voltages at the interfaces of the chip.

Figure 8: Overshoot/Undershoot voltage for USB_OV$_{IN}$, USB_HV$_{IN}$, LV$_{IN}$, OV$_{IN}$, MV$_{IN}$, SV$_{IN}$, DV$_{IN}$, SV$_{IN}$, DV$_{IN}$



Notes:

The overshoot/undershoot period should be less than 10% of shortest possible toggling period of the input signal or per input signal specific protocol requirement. For GPIO input signal overshoot/undershoot period, it should be less than 10% of the SYSCLK period.

See Table 4 for actual recommended core voltage. Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 4. The input voltage threshold scales with respect to the associated I/O supply voltage. DV$_{DD}$, OV$_{DD}$ and LV$_{DD}$ based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses differential receivers referenced by the externally supplied D1_MV$_{REF}$ signal (nominally set to G1V$_{DD}$/2) as is appropriate for the SSTL_1.35/SSTL_1.2 electrical signaling standard. The DDR MDQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

3.1.3 Output driver characteristics

This chip provides information on the characteristics of the output driver strengths.

NOTE
These values are preliminary estimates.

Table 5: Output drive capability

Driver type	Output impedance (Ω)			Supply Voltage	Notes
	Minimum[2]	Typical	Maximum[3]		
DDR4 signal	-	18(full-strength mode) 27(half-strength mode)	-	$G1V_{DD}$ = 1.2 V	1
DDR3L signal	-	18(full-strength mode) 27(half-strength mode)	-	$G1V_{DD}$ = 1.35 V	1
Ethernet signals	40	-	90	$L1V_{DD}$ / LV_{DD} = 2.5V	-
	40	-	75	$L1V_{DD}$ / LV_{DD} = 1.8V	-
MDC of Ethernet management interface 2 (EMI 2)	45	-	100	T_{VDD} = 1.2 V	-
MPIC, GPIO, system control and power management, clocking, debug, IFC,DDRCLK supply, and JTAG I/O voltage	23	-	51	OV_{DD}, $O1V_{DD}$ = 1.8 V	-
DUART, DMA, MPIC, QE, TDM, I^2C, DIU	45	-	90	DV_{DD} = 3.3V	-
	40	-	90	DV_{DD} = 2.5V	
	40	-	75	DV_{DD} = 1.8V	
eSPI, SDHC_WP, SDHC_CD	45	-	90	CV_{DD} = 3.3V	-
	40	-	75	CV_{DD} = 1.8V	
eSDHC	45	-	90	EV_{DD} = 3.3V	-
	40	-	75	EV_{DD} = 1.8V	

Notes :

1. The drive strength of the DDR4 or DDR3L interface in half-strength mode is at T_j = 105 °C and at $G1V_{DD}$ (min).
2. Estimated number based on best case processed device.
3. Estimated number based on worst case processed device.

3.1.4 General AC timing specifications

This table provides AC timing specifications for the sections not covered under the specific interface sections.

Table 6: AC Timing specifications

Parameter	Symbol	Min	Max	Unit	Note
Input signal rise and fall times	t_R/t_F	-	5	ns	1

Note:
1. Rise time refers to signal transitions from 10% to 90% of Supply; fall time refers to transitions from 90% to 10% of supply

3.2 Power sequencing

The chip requires that its power rails be applied in a specific sequence in order to ensure proper device operation.

Power up sequence when DDR3L is used

1. $O1V_{DD}$, OV_{DD}, DV_{DD}, CV_{DD}, EV_{DD}, $L1V_{DD}$, LV_{DD}, TH_V_{DD}, USB_HV_{DD}, USB_OV_{DD}, AV_{DD}_CGA1, AV_{DD}_CGA2, AV_{DD}_PLAT, AV_{DD}_D1, TV_{DD}. Drive PROG_SFP = GND
   a. PORESET_B should be driven asserted and held during this step.
2. V_{DDC}, V_{DD}, USB_SV_{DD}, $S1V_{DD}$
   a. When Deep Sleep is not used, it is recommended to source V_{DD} and VDDC from same power supply.
   b. When Deep Sleep is used, VDDC should ramp up before VDD. Alternatively VDD may ramp up together with VDDC provided that the relative timing between VDDC and VDD ramp up conforms to Figure 9
3. $G1V_{DD}$, $X1V_{DD}$, AV_{DD}_SD1_PLL1, AV_{DD}_SD1_PLL2
   a. All supplies in Step 3 may be sourced from same supply

Power up sequence when DDR4 is used

1. $O1V_{DD}$, OV_{DD}, DV_{DD}, CV_{DD}, EV_{DD}, $L1V_{DD}$, LV_{DD}, TH_V_{DD}, USB_HV_{DD}, USB_OV_{DD}, AV_{DD}_CGA1, AV_{DD}_CGA2, AV_{DD}_PLAT, AV_{DD}_D1, $X1V_{DD}$, AV_{DD}_SD1_PLL1, AV_{DD}_SD1_PLL2, TV_{DD}. Drive PROG_SFP = GND
   a. PORESET_B should be driven asserted and held during this step.
2. V_{DDC}, V_{DD}, USB_SV_{DD}, $S1V_{DD}$
   a. When Deep Sleep is not used, it is recommended to source VDD and VDDC from same power supply.
   b. When Deep Sleep is used, VDDC should ramp up before VDD. Alternatively VDD may ramp up together with VDDC provided that the relative timing between VDDC and VDD ramp up conforms to Figure 9: V_{DDC} and V_{DD} ramp up diagram.
3. $G1V_{DD}$

The supplies mentioned as OFF in "Status in Deep Sleep" column of "Recommended Operating conditions Table" are switched ON while exit from Deep sleep power management mode. These supplies should also follow the same power up sequence as mentioned above.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

All supplies must be at their stable values within 75 ms.

Negate PORESET_B input when the required assertion/hold time has been met per Table 24.

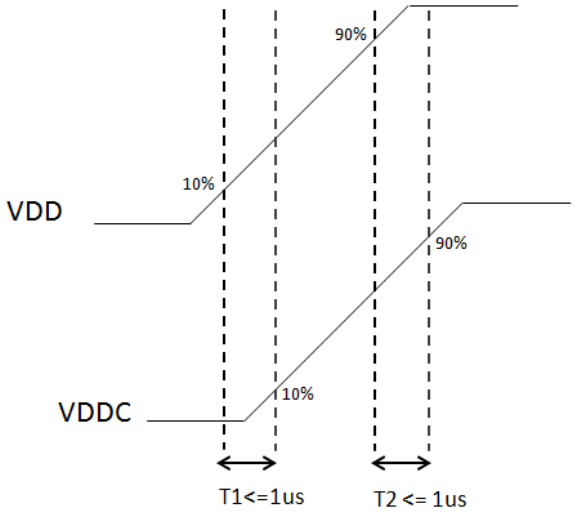
NOTE

- EVT_B2 may be unstable when PORESET_B is asserted. The signal should not be used to enable switchable power supplies during this period.
- Ramp rate requirements should be met per Table 8

Warning
Only 300,000 POR cycles are permitted per lifetime of a device. Note that this value is based on design estimates and is preliminary.

This figure provides the VDDC and VDD ramp up diagram.

Figure 9: V_{DDC} and V_{DD} ramp up diagram



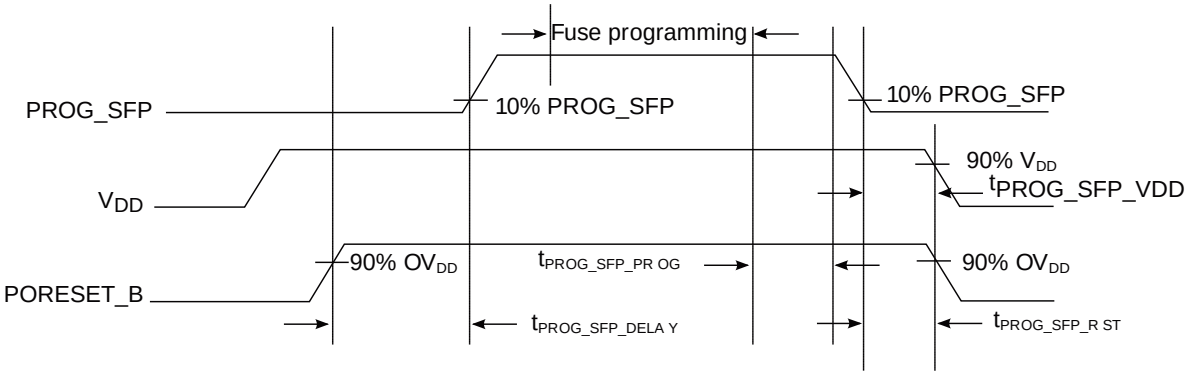
For secure boot fuse programming, use the following steps:

1. After negation of PORESET_B, drive PROG_SFP = 1.8 V after a required minimum delay per Table 7.
2. After fuse programming is completed, it is required to return PROG_SFP = GND before the system is power cycled (PORESET_B assertion) or powered down (V_{DD} ramp down) per the required timing specified in Table 7. See Security fuse processor, for additional details.

Warning
No activity other than that required for secure boot fuse programming is permitted while PROG_SFP is driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while PROG_SFP = GND.

This figure provides the PROG_SFP timing diagram.

Figure 10: PROG_SFP timing diagram



This table provides information on the power-down and power-up sequence parameters for PROG_SFP.

Table 7: PROG_SFP timing(5)

Driver type	Min	Max	Unit	Notes
$t_{PROG\_SFP\_DELAY}$	100	-	SYSCLKs	1
$t_{PROG\_SFP\_PROG}$	0	-	µs	2
$t_{PROG\_SFP\_VDD}$	0	-	µs	3
$t_{PROG\_SFP\_RST}$	0	-	µs	4

Notes:

1. Delay required from the deassertion of PORESET_B to driving PROG_SFP ramp up. Delay measured from PORESET_B deassertion at 90% OVDD to 10% PROG_SFP ramp up.
2. Delay required from fuse programming finished to PROG_SFP ramp down start. Fuse programming must complete while PROG_SFP is stable at 1.8 V. No activity other than that required for secure boot fuse programming is permitted while PROG_SFP driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while PROG_SFP = GND. After fuse programming is completed, it is required to return PROG_SFP = GND.
3. Delay required from PROG_SFP ramp down complete to VDD ramp down start. PROG_SFP must be grounded to minimum 10% PROG_SFP before VDD is at 90% VDD.
4. Delay required from PROG_SFP ramp down complete to PORESET_B assertion. PROG_SFP must be grounded to minimum 10% PROG_SFP before PORESET_B assertion reaches 90% OVDD.
5. Only two secure boot fuse programming events are permitted per lifetime of a device.

3.3 Power-down requirements

The power-down cycle must complete such that power supply values are below 0.4 V before a new power-up cycle can be started.

If performing secure boot fuse programming per Power sequencing, it is required that PROG_SFP = GND before the system is power cycled (PORESET_B assertion) or powered down (VDD ramp down) per the required timing specified in Table 7.

3.4 Power-on ramp rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum power-on ramp rate is required to avoid excess in-rush current.

This table provides the power supply ramp rate specifications.

Table 8: Power supply ramp rate

Parameter	Min	Max	Unit	Notes
Required ramp rate for all voltage supplies (including OV_{DD}/$O1V_{DD}$/DV_{DD}/ $G1V_{DD}$/$S1V_{DD}$/ $X1V_{DD}$/$L1V_{DD}$/LV_{DD}/EV_{DD}/CV_{DD} all core and platform V_{DD} supplies, $D1\_MV_{REF}$ and all AV_{DD} supplies.)	-	25	V/ms	1, 2
Required ramp rate for PROG_SFP	-	25	V/ms	1, 2
Required ramp rate for USB_HV_{DD}	-	26.7	V/ms	1, 2

Notes:
1. Ramp rate is specified as a linear ramp from 10% to 90%. If non-linear (for example, exponential), the maximum rate of change from 200 to 500 mV is the most critical as this range might falsely trigger the ESD circuitry.
2. Over full recommended operating temperature range (see Table 4)

3.5 Power characteristics

This table shows the power dissipations of the V_{DD} and V_{DDC} supply for various operating platform clock frequencies versus the core and DDR clock frequencies.

Table 9: T1024 core power dissipation

Core freq (MHz)	Platform freq (MHz)	DDR data rate (MT/s)	VDD, VDDC (V)	S1 VDD (V)	Junction temp. (ºC)	Power mode	Power (W)			Total Core and platform power (W)1	Notes
							V_{DD}	V_{DDC}	$S1V_{DD}$ [8]		
1000	400	1600	1.0	1.0	65	Typical	1.91	0.46	0.30	2.67	2, 3
					105	Thermal	2.68	0.76	0.33	3.77	4, 7
						Maximum	2.81	0.73	0.33	3.87	5, 6, 7
					125	Thermal	3.08	0.89	0.33	4.3	4, 7
						Maximum	3.21	086	0.33	4.4	5, 6, 7
1200	400	1600	1.0	1.0	65	Typical	2.20	0.46	0.30	2.96	2, 3
					105	Thermal	2.85	0.72	0.33	3.90	4, 7
						Maximum	3.14	0.73	0.33	4.20	5, 6, 7
					125	Thermal	3.25	0.85	0.33	4.43	4, 7
						Maximum	3.54	0.86	0.33	4.73	5, 6, 7
1400	400	1600	1.0	1.0	65	Typical	2.37	0.46	0.30	3.13	2, 3
					105	Thermal	3.77	1.01	0.33	5.11	4, 7
						Maximum	4.12	1.02	0.33	5.47	5, 6, 7
					125	Thermal	4.17	1.14	0.33	5.64	4, 7
						Maximum	4.52	1.15	0.33	6	5, 6, 7

Notes:
1. Combined power of VDDC, VDD and S1VDD with platform at power-on reset default state, DDR controller and all SerDes banks active. Does not include I/O power.
2. Typical power assumes Dhrystone running with activity factor of 80% (on all cores) and executing DMA on the platform with 100% activity factor.
3. Typical power based on nominal, processed device.
4. Thermal power assumes Dhrystone running with activity factor of 80% (on all cores) and executing DMA on the platform at 100% activity factor.
5. Maximum power assumes Dhrystone running with activity factor at 100% (on all cores) and executing DMA on the platform at 115% activity factor.
6. Maximum power is provided for power supply design sizing.
7. Thermal and maximum power are based on worst case processed device.
8. Total S1VDD Power conditions:
   a. SerDes Lane 1, XFI@ 10G

b. SerDes Lane 2 - 4, PCIe@ 5G

Table 10 : T1014 core power dissipation

Core freq (MHz)	Platform freq (MHz)	DDR data rate (MT/s)	V_{DD}, V_{DDC} (V)	S1 V_{DD} (V)	Junction temp. (ºC)	Power mode	Power (W)			Total Core and platform power (W)[1]	Notes
							V_{DD}	V_{DDC}	S1 V_{DD}[8]		
1000	400	1600	1.0	1.0	65	Typical	1.65	0.46	0.30	2.41	2, 3
					105	Thermal	2.31	0.76	0.33	3.40	4, 7
						Maximum	2.37	0.73	0.33	3.43	5, 6, 7
					125	Thermal	2.71	0.89	0.33	3.93	
						Maximum	2.77	0.86	0.33	3.96	
1200	400	1600	1.0	1.0	65	Typical	1.87	0.46	0.30	2.63	2, 3
					105	Thermal	2.41	0.72	0.33	3.46	4, 7
						Maximum	2.61	0.73	0.33	3.67	5, 6, 7
					125	Thermal	2.81	0.85	0.33	3.99	
						Maximum	3.01	0.86	0.33	4.2	
1400	400	1600	1.0	1.0	65	Typical	1.96	0.46	0.30	2.72	2, 3
					105	Thermal	3.14	1.01	0.33	4.48	4, 7
						Maximum	3.37	1.02	0.33	4.72	5, 6, 7
					125	Thermal	3.54	1.14	0.33	5.01	
						Maximum	3.77	1.15	0.33	5.25	

Notes:

1. Combined power of VDDC, VDD and S1VDD with platform at power-on reset default state, DDR controller and all SerDes banks active. Does not include I/O power.
2. Typical power assumes Dhrystone running with activity factor of 90% (on single core) and executing DMA on the platform with 100% activity factor.
3. Typical power based on nominal, processed device.
4. Thermal power assumes Dhrystone running with activity factor of 90% (on single core) and executing DMA on the platform at 100% activity factor.
5. Maximum power assumes Dhrystone running with activity factor at 100% (on single core) and executing DMA on the platform at 115% activity factor.
6. Maximum power is provided for power supply design sizing.
7. Thermal and maximum power are based on worst case processed device.
8. Total S1VDD Power conditions:
   a. SerDes Lane 1, XFI@ 10G
   b. SerDes Lane 2 - 4, PCIe@ 5G

This table shows the power dissipation in deep sleep mode.

Table 11: Deep sleep power dissipation, 1.0V, 35°C

Power (mW)			Total Core and platform power (mW)
V_{DD}	V_{DDC}	$S1V_{DD}$	
-	400	-	400

Note: V_{DD} and $S1V_{DD}$ are switched off during deep sleep mode.

This table provides low power mode saving estimation.

Table 12: Single core, Single cluster low power mode power savings, 1.0V 65°C[0, 2, 3]

Power Mode	Core Frequency			Units	Comment	Notes
	1000 MHz	1200 MHz	1400 MHz			
PH10	0.14	0.19	0.23	Watts	Saving realized moving from PH00 to PH10 state, single core.	4
PH15	0.20	0.23	0.27	Watts	Saving realized moving from PH10 state to PH15 state, single core.	4
LPM20	0.25	0.29	0.33	Watts	Saving realized moving from PH15 to LPM20, single core	4, 5

Notes:

1. LPM20 has all platform clocks disabled.
2. Power for V_{DD} only.
3. Typical power assumes Dhrystone running (PH00 state) with activity factor of 70%.
4. Typical power based on nominal process distribution for this device.
5. PH10, PH15, LPM20 power savings with 1 core. Maximum savings would be N times, where N is the number of used cores.

3.5.1 I/O DC power supply recommendation

This table provides the estimated I/O power numbers for each block: DDR, PCI Express, IFC, Ethernet controller, SGMII, eSDHC, USB, eSPI, DUART, IIC, DIU, SATA and GPIO. Note that these numbers are based on design estimates only.

Table 13: I/O power supply estimated values

Interface	Parameter	Symbol	Typical	Maximum	Deep Sleep	Unit	Note
DDR3L	1600MT/s data rate	G1VDD(1.35 V)	860	1760	-	mW	1,2,6
DDR4	1600MT/s data rate	G1VDD(1.2 V)	660	1000	-	mW	1, 8, 9
PCI Express	x1, 2.5 GT/s	X1VDD(1.35 V)	50	62	-	mW	1, 4, 7
	x2, 2.5 GT/s		81	94			
	x4, 2.5 GT/s		145	158			
	x1, 5 GT/s		50	70			
	x2, 5 GT/s		90	100			
SGMII	x1, 1.25 G-baud	X1VDD(1.35 V)	50	60	-	mW	1, 4, 7
	x1, 5 G-baud		50	70			
XFI	x1, 10 G-baud	X1VDD(1.35 V)	60	70	-	mW	1, 4, 7
SATA	x1, 3.0 G-Baud	X1VDD(1.35 V)	50	60	-	mW	1, 4, 7
IFC	16-bit, 100MHz	OVDD(1.8 V)	35	61	-	mW	1, 3, 7
EC1	RGMII	L1VDD(2.5 V)	155	220	13	mW	1, 3, 7
	RGMII	L1VDD(1.8 V)	115	180	11		
EC2	RGMII	LVDD(2.5 V)	155	220	-	mW	1, 3, 7
	RGMII	LVDD(1.8 V)	115	180			
eSDHC		EVDD(3.3 V)	11	17	-	mW	1, 3, 7
		EVDD(1.8 V)	7	10			
USB1, USB2		USB_HVDD(3.3 V)	40	60	-	mW	1, 3, 7
		USB_OVDD(1.8 V)	100	110			
eSPI		CVDD(3.3 V)	14	22	-	mW	1, 3, 7
		CVDD(1.8 V)	11	16			
DIU		DVDD(3.3 V)	70	90	-	mW	1, 3, 7
QE		DVDD(3.3 V)	15	21	-	mW	1, 3, 7
		DVDD(2.5 V)	11	17			
I2C		DVDD(3.3 V)	14	22	-	mW	1, 3, 7
		DVDD(2.5 V)	10	16			
		DVDD(1.8 V)	8	13			
DUART		DVDD(3.3 V)	14	22	-	mW	1, 3, 7
		DVDD(2.5 V)	10	15			
		DVDD(1.8 V)	8	12			
IEEE1588		LVDD(2.5 V)	16	21	-	mW	1, 3, 7
GPIO	x8	3.3 V	5	8	-	mW	1, 3, 5, 7
		2.5 V	4	7			
		1.8 V	3	5			
System Control		O1VDD(1.8 V)	45	70	8	mW	1, 3, 7
PLL core and system		AVDD_CGA1(1.8 V)	20	20	-	mW	1, 3, 7
		AVDD_PLAT(1.8 V)			2		
PLL DDR		AVDD_D1(1.8 V)	30	40	-	mW	1, 3, 7
PLL Serdes		AVDD_SD1_PLL1, AVDD_SD1_PLL2(1.35 V)	50	50	-	mW	1, 3, 7
PROG_SFP		PROG_SFP (1.8V)	173	-	-	mW	1, 10

Interface	Parameter	Symbol	Typical	Maximum	Deep Sleep	Unit	Note
TH_VDD		TH_VDD (1.8V)	18	-	-	mW	1
Ethernet management interface 2		TVDD	2	2		mW	1, 3, 7

Notes:
1. The typical values are estimates and based on simulations at nominal recommended voltage for the I/O power supply and assuming at 65° C junction temperature.
2. Typical DDR power numbers are based on 1 Rank DIMM with 40% utilization.
3. Assuming 15 pF total capacitance load per pin.
4. The total power numbers of X1VDD is dependent on customer application use case. This table lists all the SerDes configurations possible for the device. To get the X1VDD power numbers, the user should add the combined lanes to match to the total SerDes Lanes used, not simply multiply the power numbers by the number of lanes.
5. GPIO are supported on OVDD, O1VDD, L1VDD, LVDD, DVDD, CVDD and EVDD power rails.
6. Maximum DDR power numbers are based on 2 Ranks DIMM with 100% utilization.
7. The maximum values are dependent on actual use case such as what application, external components used, environmental conditions such as temperature voltage and frequency. This is not intended to be the maximum guaranteed power. Expect different results depending on the use case. The maximum values are estimated and they are based on simulations at 105ºC junction temperature.
8. Typical DDR4 power numbers are based on single Rank DIMM with 40% utilization.
9. Maximum DDR4 power numbers are based on single Rank DIMM with 100% utilization.
10. The max power requirement is during programming. No active power beyond leakage levels should be drawn and the supply must be grounded when not programming.

3.6 Input clocks

3.6.1 System clock (SYSCLK) timing specifications

This section provides the system clock DC and AC timing specifications.

3.6.1.1 System clock DC timing specifications

This table provides the system clock (SYSCLK) DC specifications.

Table 14: SYSCLK DC electrical characteristics [2]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	1.2	-	-	V	1
Input low voltage	V_{IL}	-	-	0.6	V	1
Input capacitance	C_{IN}	-	7	12	pF	-
Input current ($O1V_{IN}$= 0 V or $O1V_{IN}$= $O1V_{DD}$)	I_{IN}	-	-	± 50	µA	-

Notes:
1. The min VIL and max VIH values are based on the respective min and max O1VIN values found in Table 4.
2. At recommended operating conditions with $O1V_{DD}$ = 1.8 V, see Table 4.

3.6.1.2 System clock AC timing specifications

This table provides the system clock (SYSCLK) AC timing specifications.

Table 15: SYSCLK AC timing specifications[5]

Parameter/condition	Symbol	Min	Typ	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	64.0	-	133.3	MHz	0, 2
SYSCLK cycle time	t_{SYSCLK}	7.5	-	15.6	ns	0, 2
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	-	60	%	2
SYSCLK slew rate	-	1	-	4	V/ns	3
SYSCLK peak period jitter	-	-	-	± 150	ps	-
SYSCLK jitter phase noise at -56 dBc	-	-	-	500	KHz	4
AC Input Swing Limits at 1.8 V $O1V_{DD}$	ΔV_{AC}	1.08	-	1.8	V	-

Notes:
1. At recommended operating conditions with O1VDD= 1.8V, see Table 4.
2. **Caution:** The relevant clock ratio settings must be chosen such that the resulting SYSCLK frequency does not exceed their respective maximum or minimum operating frequencies.
3. Measured at the rising edge and/or the falling edge at O1VDD/2.
4. Slew rate as measured from 0.35 x O1VDD to 0.65 x O1VDD.
5. Phase noise is calculated as FFT of TIE jitter.

3.6.2 Spread-spectrum sources

Spread-spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter to diffuse the EMI spectral content. The jitter specification given in this table considers short-term (cycle-to-cycle) jitter only. The clock generator's cycle-to-cycle output jitter should meet the chip's input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns; the chip is compatible with spread-spectrum sources if the recommendations listed in this table are observed.

Table 16: Spread-spectrum clock source recommendations[3]

Parameter	Min	Max	Unit	Notes
Frequency modulation	-	60	kHz	-
Frequency spread	-	1.0	%	1, 2

Notes:
1. At recommended operating conditions with $O1V_{DD}$ = 1.8 V, see Table 4.
2. SYSCLK frequencies that result from frequency spreading and the resulting core frequency must meet the minimum and maximum specifications given in Table 15.
3. Maximum spread-spectrum frequency may not result in exceeding any maximum operating frequency of the device.

CAUTION
The processor's minimum and maximum SYSCLK and core/ platform/DDR frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated core/platform/DDR frequency should avoid violating the stated limits by using down-spreading only.

3.6.3 Real-time clock timing

The real-time clock timing (RTC) input is sampled by the platform clock. The output of the sampling latch is then used as an input to the counters of the MPIC and the time base unit of the core; there is no need for jitter specification. The minimum period of the RTC signal should be greater than or equal to 16x the period of the platform clock with a 50% duty cycle. There is no minimum RTC frequency; RTC may be grounded if not needed.

3.6.4 Gigabit Ethernet reference clock timing

This table provides the Ethernet gigabit reference clock DC specifications.

Table 17: EC*n*_GTX_CLK125 DC electrical characteristics ($L1V_{DD}/LV_{DD}$=1.8V)

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 * LVDD	-	-	V	2
Input low voltage	V_{IL}	-	-	0.2 * LVDD	V	2
Input capacitance	C_{IN}	-	-	6	pF	-
Input current (V_{IN} = 0 V or V_{IN} = $L1V_{DD}$)/ LV_{DD})	I_{IN}	-	-	± 50	µA	3

Notes:
1. At recommended operating conditions with $L1V_{DD}$ /LV_{DD} = 1.8 V
2. The min V_{IL} and max V_{IH} values are based on the respective min and max V_{IN} values found in Table 4.
3. The symbol V_{IN}, in this case, represents the $L1V_{IN}$/LV_{IN} symbol referenced in Recommended operating conditions

This table provides the Ethernet gigabit reference clock DC specifications.

Table 18: EC*n*_GTX_CLK125 DC electrical characteristics (($L1V_{DD}/LV_{DD}$=2.5V)

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 * LVDD	-	-	V	2
Input low voltage	V_{IL}	-	-	0.2 * LVDD	V	2
Input capacitance	C_{IN}	-	-	6	pF	-
Input current (V_{IN} = 0 V or V_{IN} = $L1V_{DD}$)/ LV_{DD})	I_{IN}	-	-	± 50	µA	3

Notes:
1. At recommended operating conditions with $L1V_{DD}$ /LV_{DD} = 2.5 V
2. The min V_{IL} and max V_{IH} values are based on the respective min and max V_{IN} values found in Table 4.
3. The symbol V_{IN}, in this case, represents the $L1V_{IN}$/LV_{IN} symbol referenced in Recommended operating conditions.

This table provides the Ethernet gigabit reference clocks AC timing specifications.

Table 19: EC*n*_GTX_CLK125 AC timing specifications [1]

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC*n*_GTX_CLK125 frequency	f_{G125}	125 - 100 ppm	125	125 + 100 ppm	MHz	-
EC*n*_GTX_CLK125 cycle time	t_{G125}	-	8	-	ns	-
EC*n*_GTX_CLK125 rise and fall time $L1/LV_{DD}$ = 1.8 V $L1/LV_{DD}$ = 2.5 V	t_{G125R}/t_{G125F}	-	-	 0.54 0.75	ns	2
EC*n*_GTX_CLK125 duty cycle 1000Base-T for RGMII	t_{G125H}/t_{G125}	40	-	60	%	3
EC*n*_GTX_CLK125 jitter	-	-	-	± 150	ps	3

Notes:
1. At recommended operating conditions with L1VDD/LVDD = 1.8 V ± 90mV / 2.5 V ± 125 mV.
2. Rise and fall times for ECn_GTX_CLK125 are measured from 0.5 and 2.0 V for L1VDD/LVDD = 2.5 V.
3. ECn_GTX_CLK125 is used to generate the GTX clock for the Ethernet transmitter. See RGMII AC timing specifications for duty cycle for 10Base-T and 100Base-T reference clock.

3.6.5 DDR clock timing

This section provides the DDR clock DC and AC timing specifications.

3.6.5.1 DDR clock DC timing specifications

This table provides the DDR clock (DDRCLK) DC specifications.

Table 20: DDRCLK DC electrical characteristics[3]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	-	-	V	1
Input low voltage	V_{IL}	-	-	0.6	V	1
Input capacitance	C_{IN}	-	7	12	pF	-
Input current (OV_{IN}= 0 V or OV_{IN} = OV_{DD})	I_{IN}	-	-	± 50	μA	2

Notes:
1. The min VIL and max VIH values are based on the respective min and max OV_{IN} values found in Table 4.
2. The symbol OV_{IN}, in this case, represents the OV_{IN} symbol referenced in Recommended operating conditions.
3. At recommended operating conditions with OV_{DD} = 1.8 V, see Table 4.

3.6.5.2 DDR clock AC timing specifications

This table provides the DDR clock (DDRCLK) AC timing specifications.

Table 21: DDRCLK AC timing specifications[5]

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
DDRCLK frequency	f_{DDRCLK}	64.0	-	133.3	MHz	1, 2
DDRCLK cycle time	t_{DDRCLK}	7.5	-	15.6	ns	1, 2
DDRCLK duty cycle	t_{KHK}/t_{DDRCLK}	40	-	60	%	2
DDRCLK slew rate	-	1	-	4	V/ns	3
DDRCLK peak period jitter	-	-	-	± 150	ps	-
DDRCLK jitter phase noise at -56 dBc	-	-	-	500	KHz	4
AC Input Swing Limits at 1.8 V OV_{DD}	ΔV_{AC}	1.08	-	1.8	V	-

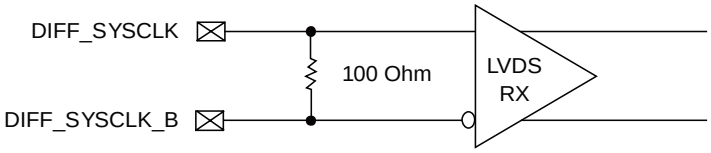
Notes:
1. At recommended operating conditions with OV_{DD} = 1.8V, see Table 4.
2. **Caution:** The relevant clock ratio settings must be chosen such that the resulting DDRCLK frequency does not exceed their respective maximum or minimum operating frequencies.
3. Measured at the rising edge and/or the falling edge at OV_{DD}/2.
4. Slew rate as measured from 0.35 x OV_{DD} to 0.65 x OV_{DD}.
5. Phase noise is calculated as FFT of TIE jitter.

3.6.6 Differential system clock (DIFF_SYSCLK/DIFF_SYSCLK_B) timing specifications

Single Source clocking mode requires single onboard oscillator to provide reference clock input to Differential System clock pair (DIFF_SYSCLK/DIFF_SYSCLK_B).

This Differential clock pair input provides clock to Core, Platform, DDR and USB PLL's. This figure shows a receiver reference diagram of the Differential System clock.

Figure 11: LVDS receiver



This section provides the differential system clock DC and AC timing specifications.

3.6.6.1 Differential system clock DC timing specifications

The Differential System clock receivers core power supply voltage requirements ($O1V_{DD}$) are as specified in Recommended operating conditions.

The Differential system clock can also be single-ended. For this, DIFF_SYSCLK_B should be connected to $O1V_{DD}/2$.

This table provides the differential system clock (DIFF_SYSCLK/DIFF_SYSCLK_B) DC specifications.

Table 22: Differential system clock DC electrical characteristics[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input differential voltage swing	V_{id}	100	-	600	mV	-
Input common mode voltage	V_{icm}	50	-	1570	mV	-
Power supply current	I_{cc}	-	-	5	mA	-
Input capacitance	C_{in}	1.45	1.5	1.55	pF	-

Note:
1. At recommended operating conditions with O1VDD = 1.8 V, see Table 4.

3.6.6.2 Differential system clock AC timing specifications

Spread Spectrum clocking is not supported on Differential System clock pair input. This table provides the differential system clock (DIFF_SYSCLK/DIFF_SYSCLK_B) AC specifications.

Table 23: Differential system clock AC electrical characteristics[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
DIFF_SYSCLK/DIFF_SYSCLK_B frequency range	t_{DIFF_SYSCLK}	-	100	-	MHz	-
DIFF_SYSCLK/DIFF_SYSCLK_B frequency tolerance	t_{DIFF_TOL}	-300	-	-300	ppm	-
Duty cycle	t_{DIFF_DUTY}	40	50	60	%	-
Clock period jitter (peak to peak)	t_{DIFF_TJ}	-	-	100	ps	1
Slew rate	t_{DIFF_slew}	0.5	-	4	V/ns	-

Notes:
1. At recommended operating conditions with O1VDD = 1.8 V, see Table 4.
2. This is evaluated with supply noise profile at +/- 5% sine wave.

3.6.7 Other input clocks

A description of the overall clocking of this device is available in the chip reference manual in the form of a clock subsystem block diagram. For information about the input clock requirements of functional sourced external of the chip, such as SerDes, Ethernet management, eSDHC, IFC, see the specific interface section.

3.7 RESET initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements. This table describes the AC electrical specifications for the RESET initialization timing.

Table 24: RESET Initialization timing specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of PORESET_B	1	-	ms	1
Required input assertion time of HRESET_B	32	-	SYSCLKs	2, 3
Maximum rise/fall time of HRESET_B	-	10	SYSCLK	4
Maximum rise/fall time of PORESET_B	-	1	SYSCLK	4
PLL input setup time with stable SYSCLK before HRESET_B negation	100	-	µs	-
Input setup time for POR configs with respect to negation of PORESET_B	4	-	SYSCLKs	2
Input hold time for all POR configs with respect to negation of PORESET_B	2	-	SYSCLKs	2
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of PORESET_B	-	5	SYSCLKs	2

Notes:

1. PORESET_B must be driven asserted before the core and platform power supplies are powered up.
2. SYSCLK is the primary clock input for the chip.
3. The device asserts HRESET_B as an output when PORESET_B is asserted to initiate the power-on reset process. The device releases HRESET_B sometime after PORESET_B is deasserted. The exact sequencing of HRESET_B deassertion is documented in section "Power-On Reset Sequence" in the chip reference manual.
4. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

This table provides the PLL lock times.

Table 25: PLL lock times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times (Core, platform, DDR only)	-	100	µs	-

3.8 DDR4 and DDR3L SDRAM controller

This section describes the DC and AC electrical specifications for the DDR4 and DDR3L SDRAM controller interface. Note that the required $G1V_{DD}$(typ) voltage is 1.2V when interfacing to DDR4 SDRAM and the $G1V_{DD}$(typ) voltage is 1.35V when interfacing to DDR3L SDRAM.

3.8.1 DDR4 and DDR3L SDRAM interface DC electrical characteristics

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3L SDRAM.

Table 26: DDR3L SDRAM interface DC electrical characteristics ($G1V_{DD}$ = 1.35 V)[1, 9]

Parameter	Symbol	Min	Max	Unit	Note
I/O reference voltage	$D1\_MV_{REF}$	0.49 x $G1V_{DD}$	0.51 x $G1V_{DD}$	V	2, 3, 4
Input high voltage	V_{IH}	$D1\_MV_{REF}$ + 0.090	$G1V_{DD}$	V	5
Input low voltage	V_{IL}	GND	$D1\_MV_{REF}$ - 0.090	V	5
Output high current (V_{OUT} = 0.641V)	I_{OH}	-	-23.3	mA	7, 8
Output low current (V_{OUT} =0.641 V)	I_{OL}	23.3	-	mA	7, 8
I/O leakage current	I_{OZ}	-100	100	µA	6

Notes:
1. G1VDD is expected to be within 50 mV of the DRAM's voltage supply at all times. The voltage supply of DRAM and memory controller may or may not be from the same source.
2. $D1\_MV_{REF}$ is expected to be equal to 0.5 x $G1V_{DD}$ and to track $G1V_{DD}$ DC variations as measured at the receiver. Peak to-peak noise on $D1\_MV_{REF}$ may not exceed the $D1\_MV_{REF}$ DC level by more than ±1% of $G1V_{DD}$ (that is ±13.5mV).
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to $D1\_MV_{REF}$ with a min value of $D1\_MV_{REF}$ - 0.04 and a max value of $D1\_MV_{REF}$ + 0.04. V_{TT} should track variations in the DC level of $D1\_MV_{REF}$.
4. The voltage regulator for $D1\_MV_{REF}$ must meet the specifications stated in Table 28.
5. Input capacitance load for DQ, DQS, and DQS_B are available in the IBIS models.
6. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ $G1V_{DD}$.
7. See the IBIS model for the complete output IV curve characteristics.
8. I_{OH} and I_{OL} are measured at $G1V_{DD}$ = 1.282 V.
9. For recommended operating conditions, see Table 4.

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR4 SDRAM.

Table 27: DDR4 SDRAM interface DC electrical characteristics ($G1V_{DD}$ = 1.2 V)[1]

Parameter	Symbol	Min	Max	Unit	Note
Input low	V_{IL}	-	0.7 x $G1V_{DD}$ - 0.175	V	1, 3, 7
Input high	V_{IH}	0.7 x $G1V_{DD}$ + 0.175	-	V	1, 3, 7
Output high current (V_{OUT} = 0.57V)	I_{OH}	-	-20.7	mA	4, 5
Output low current (V_{OUT} =0.57V)	I_{OL}	20.7	-	mA	4, 5
I/O leakage current	I_{OZ}	-100	100	µA	6

Notes:
1. For recommended operating conditions, see Table 4.
2. G1VDD is expected to be within 60 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
3. VTT and VREFCA are applied directly to the DRAM device. Both VTT and VREFCA voltages must track G1VDD/2.
4. Input capacitance load for MDQ, MDQS, and MDQS_B are available in the IBIS models.
5. IOH and IOL are measured at G1VDD = 1.14 V.
6. Refer to the IBIS model for the complete output IV curve characteristics.

7. Output leakage is measured with all outputs disabled, 0 V ≤ VOUT ≤ G1VDD.
8. Internal Vref for data must be set to 0.7 x G1VDD.

This table provides the current draw characteristics for $D1\_MV_{REF}$.

Table 28: Current draw characteristics for $D1\_MV_{REF}$

Parameter	Symbol	Min	Max	Unit	Notes
Current draw for DDR3L SDRAM for D1_MVREF	I_{D1_MVREF}	-	500	µA	-

Note:
1. For recommended operating conditions, see Table 4.

3.8.2 DDR4 and DDR3L SDRAM interface AC timing specifications

This section provides the AC timing specifications for the DDR SDRAM controller interface. The DDR controller supports DDR4 and DDR3L memories. Note that the required $G1V_{DD}$(typ) voltage is 1.2 V when interfacing to DDR4 SDRAM. The required $G1V_{DD}$(typ) voltage is 1.35 V when interfacing to DDR3L SDRAM.

3.8.2.1 DDR4 and DDR3L SDRAM interface input AC timing specifications

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3L SDRAM.

Table 29: DDR3L SDRAM interface input AC timing specifications[1]

Parameter		Symbol	Min	Max	Unit	Notes
AC input low voltage	> 1200 MT/s data rate	V_{ILAC}	-	D1_MVREF- 0.135	V	-
	≤ 1200 MT/s data rate			D1_MVREF- 0.160		
AC input high voltage	> 1200 MT/s data rate	V_{IHAC}	D1_MVREF+ 0.135	-	V	-
	≤ 1200 MT/s data rate		D1_MVREF+ 0.160			

Note:
1. For recommended operating conditions, see Table 4.

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR4 SDRAM.

Table 30: DDR4 SDRAM interface input AC timing specifications[1]

Parameter		Symbol	Min	Max	Unit	Notes
AC input low voltage	≤ 1600 MT/s data rate	V_{ILAC}	-	0.7 x G1VDD - 0.175	V	-
AC input high voltage	≤ 1600 MT/s data rate	V_{IHAC}	0.7 x G1VDD + 0.175	-	V	-

Note:
1. For recommended operating conditions, see Table 4.

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3L and DDR4 SDRAM.

Table 31: DDR4 and DDR3L SDRAM interface input AC timing specifications[3]

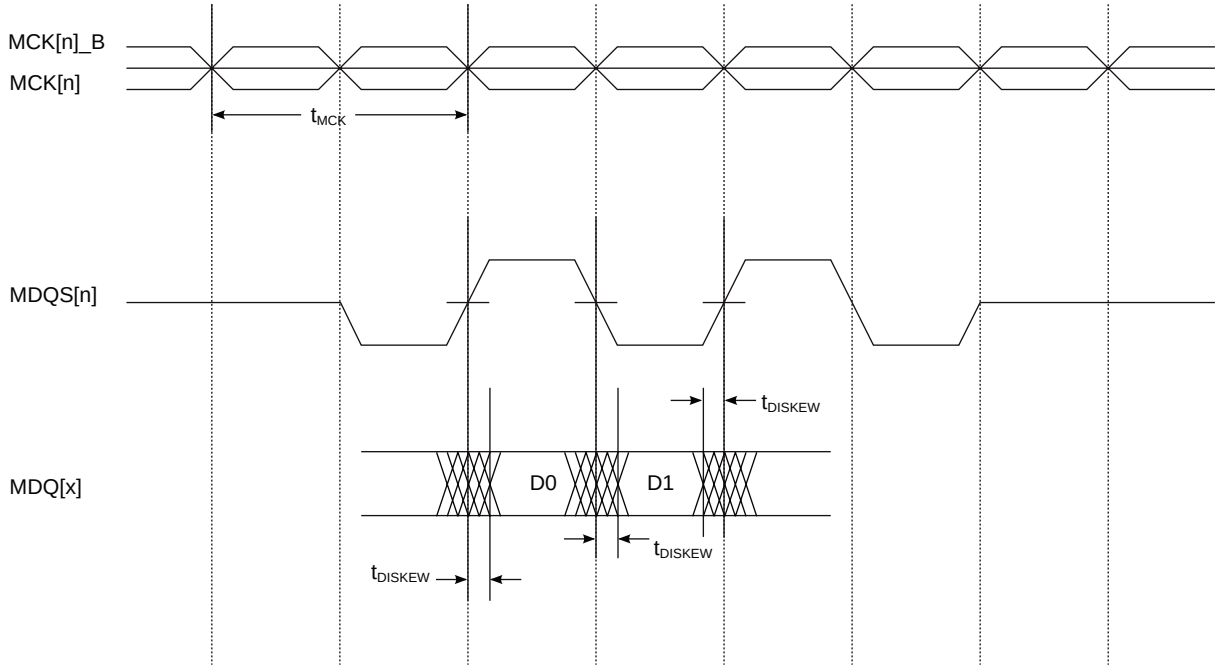
Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS-MDQ/MECC	t_{CISKEW}			ps	
1600 MT/s data rate		-112	112		1
1300 MT/s data rate		-125	125		1
1200 MT/s data rate		-142	142		1, 4
1000 MT/s data rate		-170	170		1, 4
Tolerated Skew for MDQS-MDQ/MECC	t_{DISKEW}			ps	
1600 MT/s data rate		-200	200		2
1300 MT/s data rate		-250	250		2
1200 MT/s data rate		-275	275		2, 2
1000 MT/s data rate		-330	330		2, 2

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This must be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}.This can be determined by the following equation: $t_{DISKEW} = \pm(T \div 4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.
3. For recommended operating conditions, see Table 4.
4. DDR3L only.

This figure shows the DDR4 and DDR3L SDRAM interface input timing diagram.

Figure 12: DDR4 and DDR3L SDRAM Interface Input Timing Diagram



3.8.2.2 DDR4 and DDR3L SDRAM interface output AC timing specifications

This table provides the output AC timing targets for the DDR4 and DDR3L SDRAM interface.

Table 32: DDR4 and DDR3L SDRAM interface output AC timing specifications[8]

Parameter		Symbol[1]	Min	Max	Unit	Notes
MCK[n] cycle time		t_{MCK}	1250	2000	ps	2
ADDR/CMD/CNTL output setup with respect to MCK	1600 MT/s data rate	t_{DDKHAS}	495	–	ps	3
	1300 MT/s data rate		606	–		
	1200 MT/s data rate		675	–		3, 6
	1000 MT/s data rate		744	–		3, 6
ADDR/CMD/CNTL output hold with respect to MCK	1600 MT/s data rate	t_{DDKHAX}	495	–	ps	3
	1300 MT/s data rate		606	–		
	1200 MT/s data rate		675	–		3, 6
	1000 MT/s data rate		744	–		3, 6
MCK to MDQS Skew ≥ 1000 MT/s data rate, ≤ 1600 MT/s data rate		t_{DDKHMH}	(-)245	245	ps	4, 7
MDQ/MECC/MDM output Data eye	1600 MT/s data rate	$t_{DDKXDEYE}$,	400	–	ps	5
	1300 MT/s data rate		500	–		
	1200 MT/s data rate		550	–		5, 6
	1000 MT/s data rate		600	–		5, 6
MDQS preamble		t_{DDKHMP}	900 x t_{MCK}	–	ps	–
MDQS postamble		t_{DDKHME}	400 x t_{MCK}	600 x t_{MCK}	ps	–

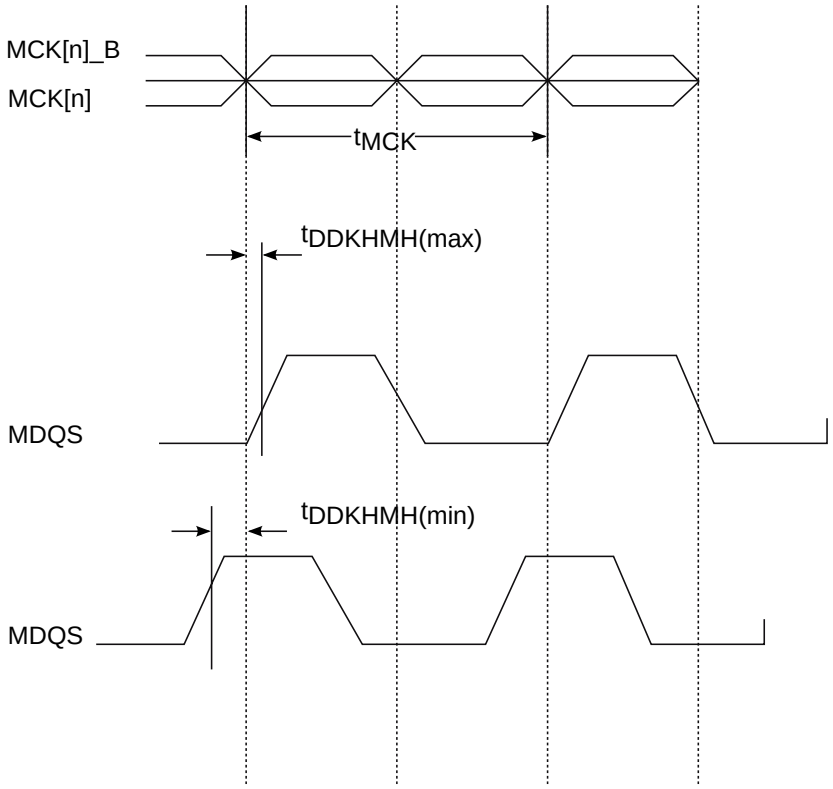
Notes:

1. The symbols used for timing specifications follow these patterns: $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time.
2. All MCK/MCK_B and MDQS/MDQS_B referenced measurements are made from the crossing of the two signals.
3. ADDR/CMD/CNTL includes all DDR SDRAM output signals except MCK/MCK_B, MCS_B, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This is typically set to the same delay as in DDR_SDRAM_CLK_CNTL[CLK_ADJUST]. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the chip reference manual for a description and explanation of the timing modifications enabled by the use of these bits.
5. Available eye for data (MDQ), ECC (MECC), and data mask (MDM) outputs at the pin of the processor. Memory controller will center the strobe (MDQS) in the available data eye at the DRAM (end point) during the initialization.
6. DDR3L only.
7. Note that it is required to program the start value of the MDQS adjust for write leveling.
8. For recommended operating conditions, see Table 4.

NOTE
For the ADDR/CMD/CNTL setup and hold specifications in Table 32, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.

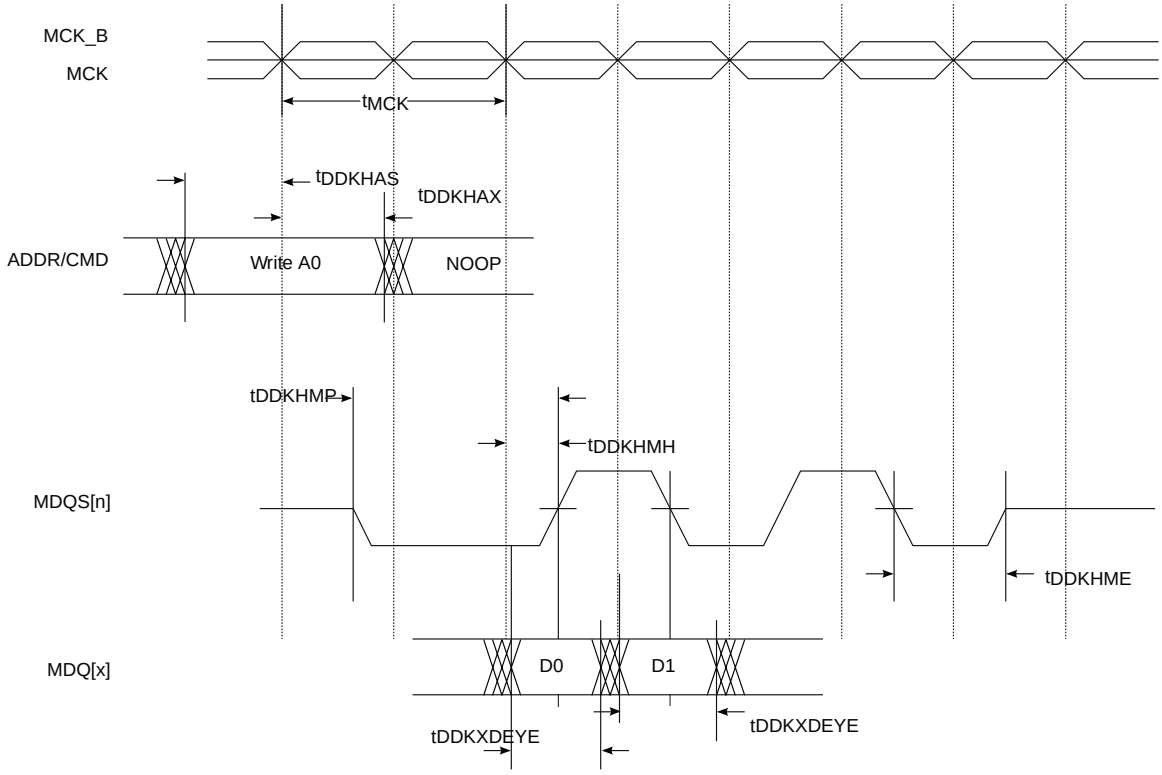
This figure shows the DDR4 and DDR3L SDRAM interface output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

Figure 13: t_{DDKHMH} timing diagram



This figure shows the DDR4 and DDR3L SDRAM output timing diagram.

Figure 14: DDR4 and DDR3L output timing diagram



3.9 eSPI interface

This section describes the DC and AC electrical specifications for the eSPI interface.

3.9.1 eSPI DC electrical characteristics

This table provides the DC electrical characteristics for the eSPI interface operating at CV_{DD} = 1.8 V.

Table 33: eSPI DC electrical characteristics (1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x CV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.2 x CV_{DD}	V	2
Input current (V_{IN} = 0 V or V_{IN} = CV_{DD})	I_{IN}	-	±50	µA	3
Output high voltage	V_{OH}	1.35	-	V	-
(CV_{DD} = min, I_{OH} = -0.5 mA)					
Output low voltage (CV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

Notes:
1. For recommended operating conditions, see Table 4.
2. The min V_{IL} and max VIH values are based on the respective min and max CVIN values found in Table 4.
3. The symbol V_{IN}, in this case, represents the CVIN symbol referenced in Recommended operating conditions.

This table provides the DC electrical characteristics for the eSPI interface operating at CVDD = 3.3 V.

Table 34: eSPI DC electrical characteristics (3.3 V)

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x CV_{DD}	-	V	2
Input low voltage	V_{IL}	-	0.2 x CV_{DD}	V	2
Input current (V_{IN} = 0 V or V_{IN} = CV_{DD})	I_{IN}	-	±50	µA	-
Output high voltage (I_{OH} = -2.0 mA)	V_{OH}	2.4	-	V	-
Output low voltage (I_{OL} = 2.0 mA)	V_{OL}	-	0.4	V	-

Notes:
1. For recommended operating conditions, see Table 4.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max CVIN values found in Table 4.

3.9.2 eSPI AC timing specifications

This table provides the eSPI input and output AC timing specifications.

Table 35: eSPI AC timing specifications[3]

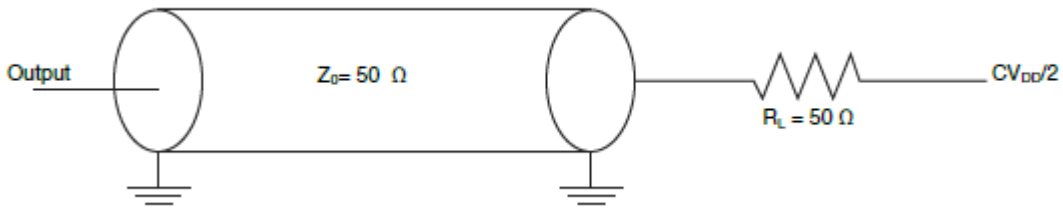
Parameter/Condition	Symbol [2]	Min	Max	Unit	Notes
SPI_MOSI output-Master data (internal clock) hold time	t_{NIKHOX}	(-1.5) + ($t_{PLATFORM\_CLK/2}$ * SPMODE[HO_ADJ])	-	ns	1, 2
SPI_MOSI output-Master data (internal clock) delay	t_{NIKHOV}	-	1.5 + ($t_{PLATFORM\_CLK/2}$ * SPMODE[HO_ADJ])	ns	1, 2
SPI_CS outputs-Master data (internal clock) hold time	$t_{NIKHOX2}$	-100	-	ns	1
SPI_CS outputs-Master data (internal clock) delay	$t_{NIKHOV2}$	-	6.0	ns	1
SPI inputs-Master data (internal clock) input setup time	t_{NIIVKH}	6.09	-	ns	-
SPI inputs-Master data (internal clock) input hold time	t_{NIIXKH}	0	-	ns	-
Clock-high time	t_{NIKCKH}	4	-	ns	
Clock-low time	t_{NIKCKL}	4	-	ns	-

Notes:

1. See the chip reference manual for details about the SPMODE register.
2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
3. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).
4. Refer AN4375 to calculate maximum achievable eSPI interface frequency on a system.

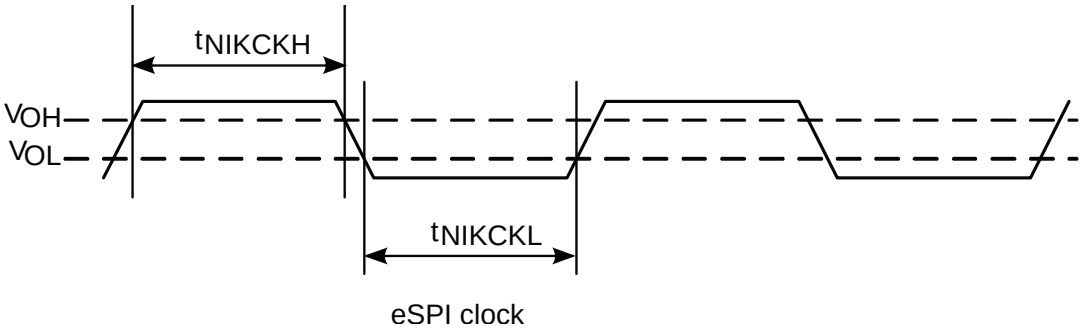
This figure provides the AC test load for the eSPI

Figure 15: eSPI AC test load



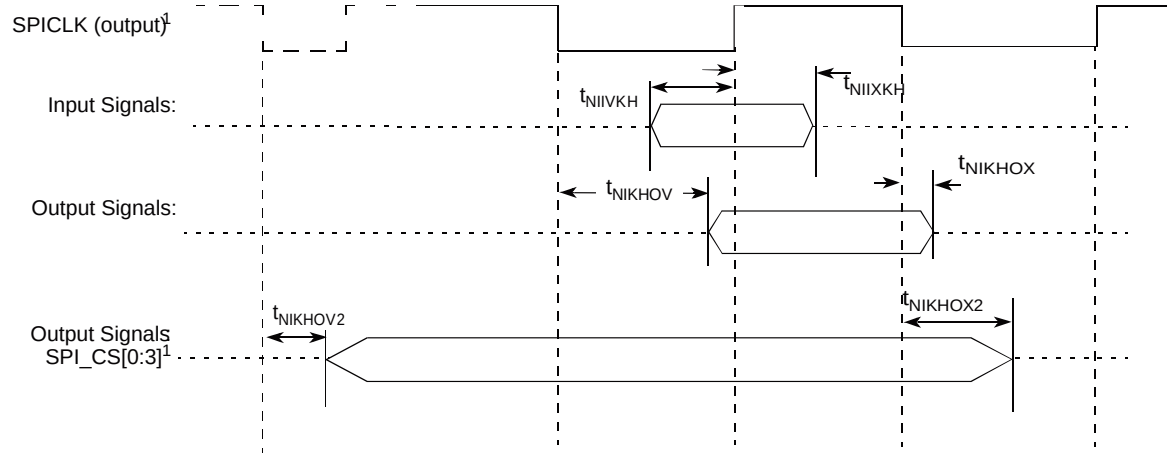
This figure provides the eSPI clock output timing diagram.

Figure 16: eSPI clock output timing diagram



This figure represents the AC timing from Table 35 in master mode (internal clock). Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge. Also, note that the clock edge is selectable on eSPI.

Figure 17: eSPI AC timing in master mode (internal clock) diagram



Note 1: SPICLK appears on the interface only after CS assertion.

3.10 DUART interface

This section describes the DC and AC electrical specifications for the DUART interface.

3.10.1 DUART DC electrical characteristics

This table provides the DC electrical characteristics for the DUART interface at DV_{DD} = 3.3 V.

Table 36: DUART DC electrical characteristics (3.3 V)

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	-	V	2
Input low voltage	VIL	–	0.2 x DV_{DD}	V	2
Input current (VIN = 0 V or VIN = DVDD)	IIN	–	±50	µA	1
Output high voltage	VOH	2.4	–	V	–
(IOH = -2.0 mA)					
Output low voltage	VOL	–	0.4	V	–
(IOL = 2.0 mA)					

Notes:
1. For recommended operating conditions, see Table 4.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max DVIN values found in Table 4.

This table provides the DC electrical characteristics for the DUART interface at DV_{DD} = 2.5 V.

Table 37: DUART DC electrical characteristics(2.5 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	–	V	1
Input low voltage	V_{IL}	–	0.2 x DV_{DD}	V	1
Input current (DV_{IN} = 0 V or DV_{IN} = DV_{DD})	I_{IN}	–	±50	µA	2
Output high voltage (DV_{DD} = min, I_{OH} = -1 mA)	V_{OH}	2.0	–	V	–
Output low voltage (DV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	–	0.4	V	–

Notes:
1. The min VIL and max VIH values are based on the min and max DVIN respective values found in Table 4.
2. The symbol DVIN represents the input voltage of the supply. It is referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 4.

This table provides the DC electrical characteristics for the DUART interface at DV_{DD} = 1.8 V.

Table 38: DUART DC electrical characteristics(1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	–	V	1
Input low voltage	V_{IL}	–	0.2 x DV_{DD}	V	1
Input current (DV_{IN} = 0 V or DV_{IN} = DV_{DD})	I_{IN}	–	±50	µA	2
Output high voltage (DV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	–	V	–
Output low voltage (DV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	–	0.4	V	–

Notes:
1. The min VIL and max VIH values are based on the min and max DVIN respective values found in Table 4.
2. The symbol DVIN represents the input voltage of the supply. It is referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 4.

3.10.1.1 DUART AC electrical specifications

This table provides the AC timing parameters for the DUART interface.

Table 39: DUART AC timing specifications

Parameter	Value	Unit	Notes
Minimum baud rate	f_{PLAT}/(2 x 1,048,576)	baud	1, 3
Maximum baud rate	f_{PLAT}/(2 x 16)	baud	1, 2

Notes:
1. f_{PLAT} refers to the internal platform clock.
2. The actual attainable baud rate is limited by the latency of interrupt processing.
3. The middle of a start bit is detected as the eighth sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

3.11 Ethernet interface, Ethernet management interface, IEEE Std 1588™

This section provides the AC and DC electrical characteristics for the Ethernet controller and the Ethernet management interface.

3.11.1 SGMII interface

Each SGMII port features a 4-wire AC-coupled serial link from the SerDes interface of the chip, as shown in Figure 18, where C_{TX} is the external (on board) AC-coupled capacitor. Each SerDes transmitter differential pair features 100-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to XGND*n*. The reference circuit of the SerDes transmitter and receiver is shown in Figure 68.

3.11.1.1 SGMII clocking requirements for SD1_REF_CLK*n*_P and SD1_REF_CLK*n*_N

When operating in SGMII mode, the EC*n*_GTX_CLK125 clock is not required for this port. Instead, a SerDes reference clock is required on SD1_REF_CLK[1:2]_P and SD1_REF_CLK[1:2]_N pins. SerDes lanes may be used for SerDes SGMII configurations based on the RCW Configuration field SRDS_PRTCL.

For more information on these specifications, see SerDes reference clocks.

3.11.1.2 SGMII DC electrical characteristics

This section discusses the electrical characteristics for the SGMII interface.

3.11.1.2.1 SGMII and SGMII 2.5G transmit DC specifications

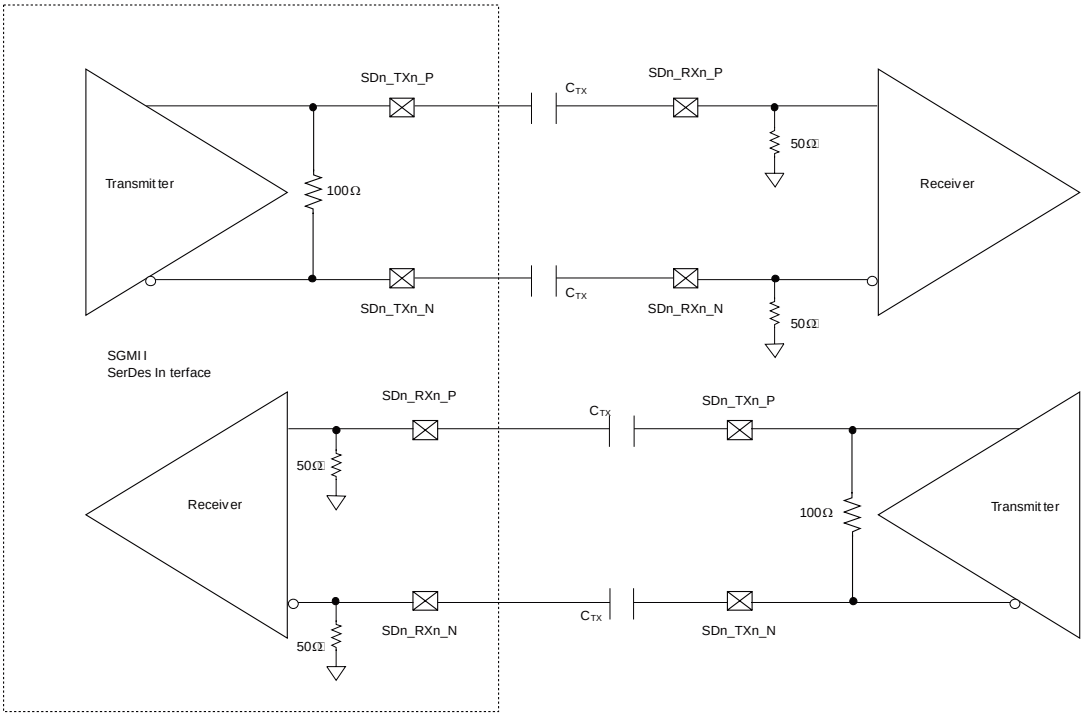
This table describes the SGMII SerDes transmitter AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD1_TX*n*_P and SD1_TX*n*_N)as shown in Figure 19.

Table 40: SGMII DC transmitter electrical characteristics ($X1V_{DD}$ = 1.35 V)[4]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output high voltage	V_{OH}	-	-	1.5 x $\lvert V_{OD}\rvert_{-max}$	mV	1
Output low voltage	V_{OL}	$\lvert V_{OD}\rvert_{-min}/2$	-	-	mV	1
Output differential voltage[2, 3, 5] (XV_{DD-Typ} at 1.35 V)	$\lvert V_{OD}\rvert$	320	500.0	725.0	mV	TECR0[AMP_R ED]=0b000000
		293.8	459.0	665.6		TECR0[AMP_R ED]=0b000001
		266.9	417.0	604.7		TECR0[AMP_R ED]=0b000011
		240.6	376.0	545.2		TECR0[AMP_R ED]=0b000010
		213.1	333.0	482.9		TECR0[AMP_R ED]=0b000110
		186.9	292.0	423.4		TECR0[AMP_R ED]=0b000111
		160.0	250.0	362.5		TECR0[AMP_R ED]=0b010000
Output impedance (differential)	R_O	80	100	120	Ω	-

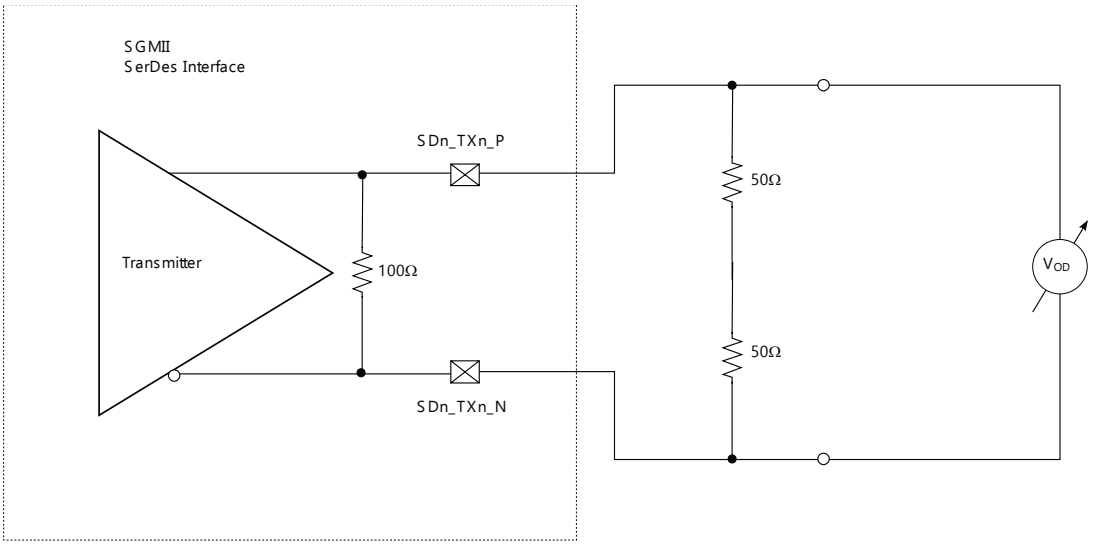
Notes:
1. This does not align to DC-coupled SGMII.
2. $\lvert VOD\rvert$ = $\lvert VSD\_TXn\_P - VSD\_TXn\_N\rvert$. $\lvert VOD\rvert$ is also referred to as output differential peak voltage. $V_{TX-DIFFp-p} = 2 \times \lvert VOD\rvert$.
3. The $\lvert VOD\rvert$ value shown in the Typ column is based on the condition of XVDD_SRDSn-Typ = 1.35 V, no common mode offset variation. SerDes transmitter is terminated with 100-Ω differential load between SDn _TXn_P and SDn_TXn_N.
4. For recommended operating conditions, see Table 4.
5. Example amplitude reduction setting for SGMII on SerDes1 lane E: SRDS1LN4TECR0[AMP_RED] = 0b000001 for an output differential voltage of 459 mV typical.

Figure 18: 4-wire AC-coupled SGMII serial link connection example



This figure shows the SGMII transmitter DC measurement circuit.

Figure 19: SGMII transmitter DC measurement circuit



This table defines the SGMII 2.5G transmitter DC electrical characteristics for 3.125 GBaud.

Table 41: SGMII 2.5G transmitter DC electrical characteristics (X1VDD = 1.35 V)1

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Output differential voltage	$\lvert V_{OD} \rvert$	400	-	600	mV	
Output impedance (differential)	R_O	80	100	120	Ω	-

Note:
1. For recommended operating conditions, see Table 4.

3.11.1.2.2 SGMII and SGMII 2.5G DC receiver electrical characteristics

This table lists the SGMII DC receiver electrical characteristics. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 42: SGMII DC receiver electrical characteristics (S1VDD = 1.0V)4

Parameter		Symbol	Min	Typ	Max	Unit	Notes
DC input voltage range		-	N/A			-	1
Input differential voltage	REIDL_TH = 001	$V_{RX\_DIFFp-p}$	100	-	1200	mV	2, 5
	REIDL_TH = 100		175	-			
Loss of signal threshold	REIDL_TH = 001	V_{LOS}	30	-	100	mV	3, 5
	REIDL_TH = 100		65	-	175		
Receiver differential input impedance		Z_{RX_DIFF}	80	-	120	Ω	-

This table defines the SGMII 2.5G receiver DC electrical characteristics for 3.125 GBaud.

Table 43: SGMII 2.5G receiver DC timing specifications (S1VDD = 1.0V)1

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input differential voltage	V_{RX_DIFFp-}	200	-	1200	mV	-
Loss of signal threshold	V_{LOS}	75	-	200	mV	-
Receiver differential input impedance	Z_{RX_DIFF}	80	-	120	Ω	-

Notes:
1. For recommended operating conditions, see Table 4.
2. Input must be externally AC coupled
3. VRX_DIFFp-p is also referred to as peak-to-peak input differential voltage.
4. The concept of this parameter is equivalent to the electrical idle detect threshold parameter in PCI Express. See PCI Express DC physical layer receiver specifications, and PCI Express AC physical layer receiver specifications, for further explanation.
5. For recommended operating conditions, see Table 4.
6. The REIDL_TH shown in the table refers to the chip's SRDSxLNmGCR1[REIDL_TH] bit field.

3.11.1.3 SGMII AC timing specifications

This section discusses the AC timing specifications for the SGMII interface.

3.11.1.3.1 SGMII and SGMII 2.5G transmit AC timing specifications

This table provides the SGMII and SGMII 2.5G transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include RefClk jitter.

Table 44: SGMII transmit AC timing specifications4

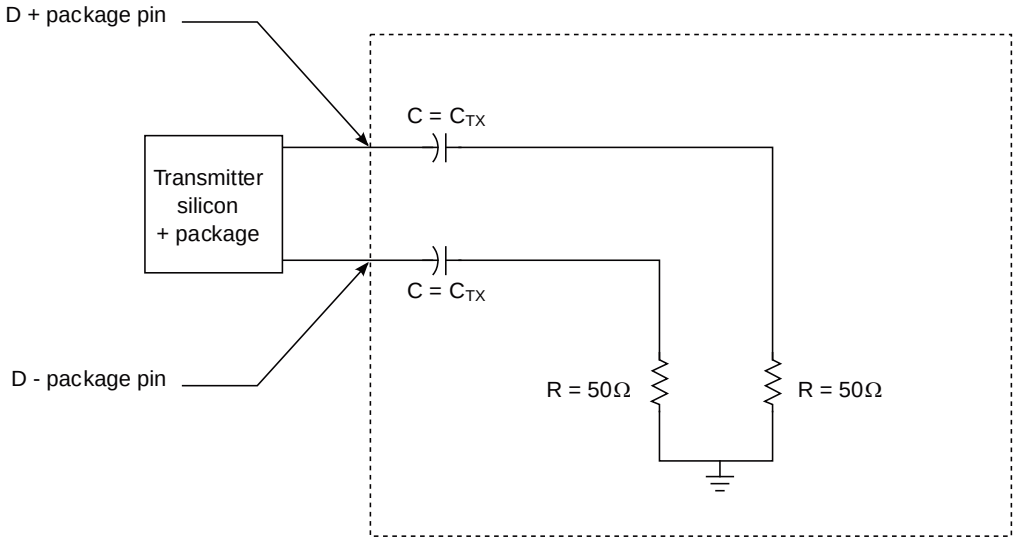
Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter	JD	-	-	0.17	UI p-p	-
Total jitter	JT	-	-	0.35	UI p-p	2
Unit Interval: 1.25 GBaud (SGMII)	UI	800 - 100 ppm	800	800 + 100 ppm	ps	1
Unit Interval: 3.125 GBaud (2.5G SGMII])	UI	320 - 100 ppm	320	320 + 100 ppm	ps	1
AC coupling capacitor	C_{TX}	10	-	200	nF	3

Notes:
1. Each UI is 800 ps ± 100 ppm or 320 ps ± 100 ppm.
2. See Figure 21 for single frequency sinusoidal jitter measurements.
3. The external AC coupling capacitor is required. It is recommended that it be placed near the device transmitter output.
4. For recommended operating conditions, see Table 4.

3.11.1.3.2 SGMII AC measurement details

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SD1_TX*n*_P and SD1_TX*n*_N) or at the receiver inputs (SD1_RX*n*_P and SD1_RX*n*_N) respectively, as depicted in this figure.

Figure 20: SGMII AC test/measurement load



3.11.1.3.3 SGMII and SGMII 2.5G receiver AC timing Specification

This table provides the SGMII and SGMII 2.5G receiver AC timing specifications. The AC timing specifications do not include RefClk jitter. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 45: SGMII Receive AC timing specifications[3]

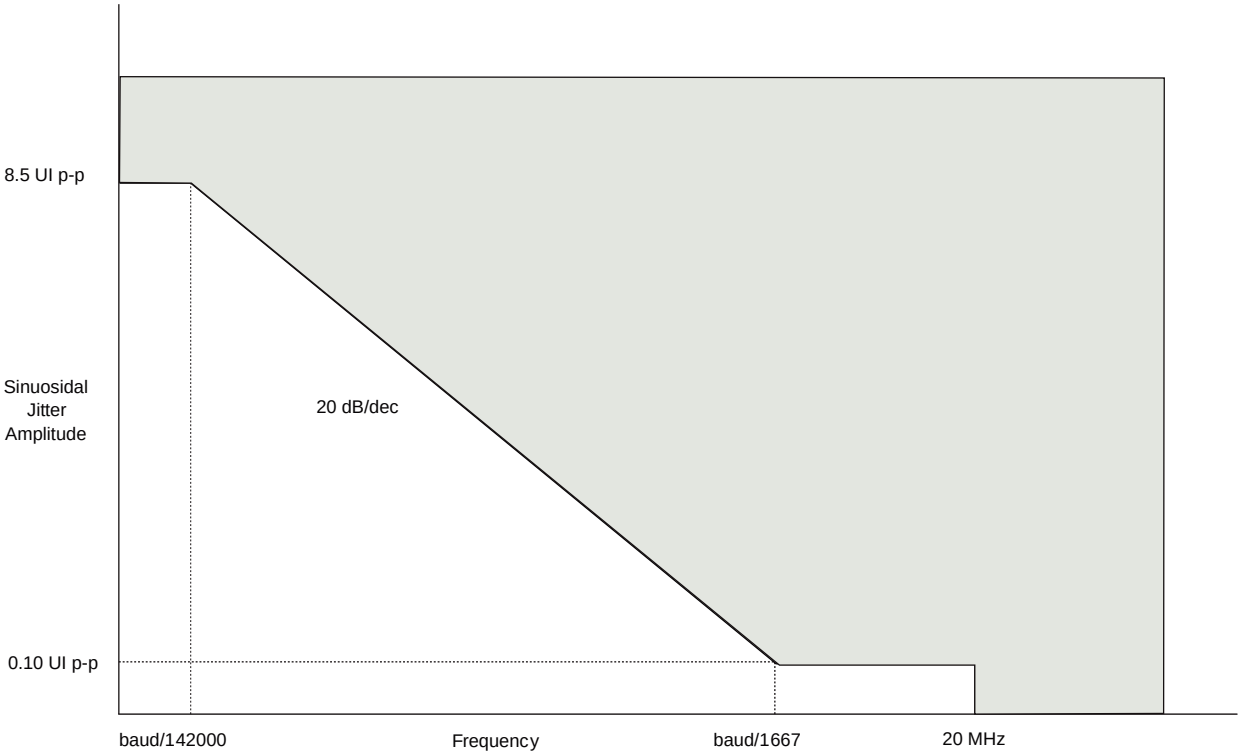
Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter tolerance	J_D	-	-	0.37	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	-	-	0.55	UI p-p	1
Total jitter tolerance	J_T	-	-	0.65	UI p-p	1, 2
Bit error ratio	BER	-	-	10^{-12}	-	-
Unit Interval: 1.25 GBaud (SGMII)	UI	800 - 100 ppm	800	800 + 100 ppm	ps	1
Unit Interval: 3.125 GBaud (2.5G SGMII])	UI	320 - 100 ppm	320	320 + 100 ppm	ps	1

Notes:

1. Measured at receiver
2. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 21. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.
3. For recommended operating conditions, see Table 4.

The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of this figure.

Figure 21: Single-frequency sinusoidal jitter limits



3.11.2 QSGMII interface

This section describes the QSGMII clocking and its DC and AC electrical characteristics.

3.11.2.1 QSGMII clocking requirements for SD*n*_REF_CLK*n* and SD*n*_REF_CLK*n*_B

For more information on these specifications, see SerDes reference clocks.

3.11.2.2 QSGMII DC electrical characteristics

This section discusses the electrical characteristics for the SGMII interface.

3.11.2.2.1 QSGMII transmitter DC specifications

This table describes the QSGMII SerDes transmitter AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD*n*_TX*n* and SD*n*_TX*n*_B).

Table 46: QSGMII DC transmitter electrical characteristics ($X1V_{DD}$ = 1.35V)[1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output differential voltage	V_{DIFF}	400	-	900	mV	-
Differential resistance	T_{RD}	80	100	120	Ω	-

Note:
1. For recommended operating conditions, see Table 4.

3.11.2.2.2 QSGMII DC receiver electrical characteristics

This table defines the QSGMII receiver DC electrical characteristics.

Table 47: QSGMII receiver DC timing specifications (SV_{DD} = 1.0V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input differential voltage	V_{DIFF}	100	-	900	mV	-
Differential resistance	R_{RDIN}	80	100	120	Ω	-

Note:
1. For recommended operating conditions, see Table 4.

3.11.2.3 QSGMII AC timing specifications

This section discusses the AC timing specifications for the QSGMII interface.

3.11.2.3.1 QSGMII transmit AC timing specifications

This table provides the QSGMII transmitter AC timing specifications.

Table 48: QSGMII transmit AC timing specifications[1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Transmitter baud rate	T_{BAUD}	5.000 - 100 ppm	5.000	5.000 + 100 ppm	Gb/s	-
Uncorrelated high probability jitter	T_{UHPJ}	-	-	0.15	UI p-p	-
Total jitter tolerance	J_T	-	-	0.30	UI p-p	-

Note:
1. For recommended operating conditions, see Table 4.

3.11.2.3.2 QSGMII receiver AC timing Specification

This table provides the QSGMII receiver AC timing specifications.

Table 49: QSGMII receive AC timing specifications[2]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Receiver baud rate	R_{BAUD}	5.000 - 100 ppm	5.000	5.000 + 100 ppm	Gb/s	-
Uncorrelated bounded high probability jitter	R_{DJ}	-	-	0.15	UI p-p	-
Correlated bounded high probability jitter	R_{CBHPJ}	-	-	0.30	UI p-p	1
Bounded high probability jitter	R_{BHPJ}	-	-	0.45	UI p-p	-
Sinusoidal jitter, maximum	R_{SJ-max}	-	-	5.00	UI p-p	-
Sinusoidal jitter, high frequency	R_{SJ-hf}	-	-	0.05	UI p-p	-
Total jitter (does not include sinusoidal jitter)	R_{Tj}	-	-	0.60	UI p-p	-

Notes:
1. The jitter (RCBHPJ) and amplitude have to be correlated, for example, by a PCB trace.
2. For recommended operating conditions, see Table 4.

The sinusoidal jitter may have any amplitude and frequency in the unshaded region of this figure.

Figure 22: QSGMII single-frequency sinusoidal jitter limits

3.11.3 1000Base-KX interface

This section discusses the electrical characteristics for the 1000Base-KX. Only AC- coupled operation is supported.

3.11.3.1 1000Base-KX DC electrical characteristics

3.11.3.1.1 1000Base-KX Transmitter DC Specifications

This table describes the 1000Base-KX SerDes transmitter DC specification at TP1 per IEEE Std 802.3ap-2007. Transmitter DC characteristics are measured at the transmitter outputs (SD1_TXn_P and SD1_TXn_N).

Table 50: 1000Base-KX Transmitter DC Specifications

Parameter	Symbols	Min	Typ	Max	Units	Notes
Output differential voltage	$V_{TX-DIFFp-p}$	800	-	1600	mV	1
Differential resistance	T_{RD}	80	100	120	ohm	-

Notes:
1. SRDSxLNmTECR0[AMP_RED]=00_0000.
2. For recommended operating conditions, see Table 4.

3.11.3.1.2 1000Base-KX Receiver DC Specifications

Table below provides the 1000Base-KX receiver DC timing specifications.

Table 51: 1000Base-KX Receiver DC Specifications

Parameter	Symbols	Min	Typical	Max	Units	Notes
Input differential voltage	$V_{RX-DIFFp-p}$	-	-	1600	mV	1
Differential resistance	T_{RDIN}	80	-	120	ohm	-

Notes:
1. For recommended operating conditions, see Table 4.

3.11.3.2 1000Base-KX AC electrical characteristics

3.11.3.2.1 1000Base-KX Transmitter AC Specifications

Table below provides the 1000Base-KX transmitter AC specification.

Table 52: 1000Base-KX Transmitter AC Specifications

Parameter	Symbols	Min	Typical	Max	Units	Notes
Baud Rate	T_{BAUD}	1.25-100ppm	1.25	1.25+100ppm	Gb/s	-
Uncorrelated High Probability Jitter/ Random Jitter	$T_{UHPJ}T_{RJ}$	-	-	0.15	UI p-p	-
Deterministic Jitter	T_{DJ}	-	-	0.10	UI p-p	-
Total Jitter	T_{TJ}	-	-	0.25	UI p-p	1

Notes:
1. Total jitter is specified at a BER of 10-12.
2. For recommended operating conditions, Table 4.

3.11.3.2.2 1000Base-KX Receiver AC Specifications

Table below provides the 1000Base-KX receiver AC specification with parameters guided by IEEE Std 802.3ap-2007.

Table 53: 1000Base-KX Receiver AC Specifications

Parameter	Symbols	Min	Typical	Max	Units	Notes
Receiver Baud Rate	T_{BAUD}	1.25-100ppm	1.25	1.25+100ppm	Gb/s	-
Random Jitter	R_{RJ}	-	-	0.15	UI p-p	1
Sinusoidal Jitter, maximum	R_{SJ-max}	-	-	0.10	UI p-p	2
Total Jitter	R_{TJ}	-	-	See Note 3	UI p-p	2

Notes:
1. Random jitter is specified at a BER of 10-12.
2. The receiver interference tolerance level of this parameter shall be measured as described in Annex 69A of the IEEE Std 802.3ap-2007.
3. Per IEEE 802.3ap-clause 70.
4. The AC specifications do not include Refclk jitter.
5. For recommended operating conditions, Table 4.

3.11.4 RGMII electrical specifications

This section discusses the electrical characteristics for the RGMII interface.

3.11.4.1 RGMII DC electrical characteristics

This table shows the DC electrical characteristics for the RGMII interface.

Table 54: RGMII DC electrical characteristics(LV_{DD}, $L1V_{DD}$ = 2.5 V)[4]

Parameters	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x LV_{DD}	-	V	1
Input low voltage	V_{IL}	-	0.2 x LV_{DD}	V	1
Input current (LV_{IN}=0 V or LV_{IN}= LV_{DD})	I_{IH}	-	±50	µA	2, 3
Output high voltage (LV_{DD} = min,I_{OH} = -1.0 mA)	V_{OH}	2.00	-	V	3
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	-	0.4	V	3

Notes:
1. The min VIL and max VIH values are based on the respective min and max LVIN values found in Table 4.
2. The symbol LVIN, in this case, represents the LVIN and L1VIN symbol referenced in Recommended operating conditions.
3. The symbol LVDD, in this case, represents the LVDD and L1VDD symbol referenced in Recommended operating conditions.
4. For recommended operating conditions, see Table 4.

This table provides the DC electrical characteristics for the RGMII interface at $L1V_{DD}/LV_{DD}$ = 1.8 V.

Table 55: RGMII DC electrical characteristics(1.8 V)[4]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x LV_{DD}	-	V	1
Input low voltage	V_{IL}	-	0.2 x LV_{DD}	V	1
Input current (LV_{IN} = 0 V or LV_{IN}= LV_{DD})	I_{IN}	-	±50	µA	2, 3
Output high voltage (LV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	3
Output low voltage (LV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	3

Notes:
1. The min VIL and max VIH values are based on the min and max LVIN values found in Table 4.
2. The symbol LVIN, in this case, represents the LVIN and L1VIN symbol referenced in Recommended operating conditions.
3. The symbol LVDD, in this case, represents the LVDD and L1VDD symbol referenced in Recommended operating conditions.
4. For recommended operating conditions, see Table 4.

3.11.4.2 RGMII AC timing specifications

This table presents the RGMII AC timing specifications.

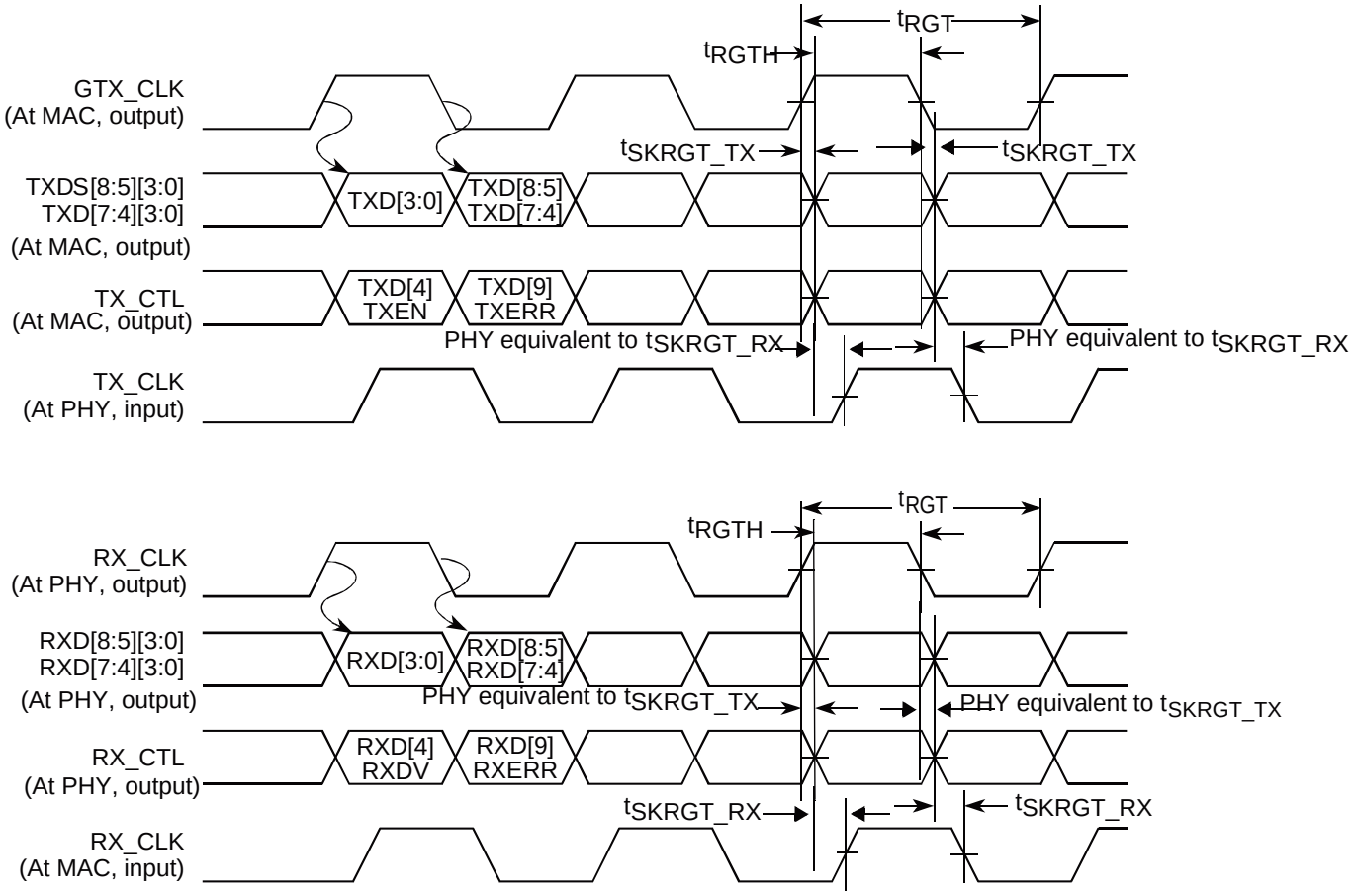
Table 56: RGMII AC timing specifications (LV_{DD} = 2.5 /1.8 V)[8]

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
Data to clock output skew (at transmitter)	t_{SKRGT_TX}	-620	0	520	ps	7
Data to clock input skew (at receiver)	t_{SKRGT_RX}	1.6	-	2.6	ns	2
Clock period duration	t_{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40	50	60	%	3, 4
Duty cycle for Gigabit	t_{RGTH}/t_{RGT}	45	50	55	%	-
Rise time (20%-80%) $L1/LV_{DD}$ = 2.5V $L1/LV_{DD}$ = 1.8V	t_{RGTR}	-	-	- 0.75 0.54	ns	5, 6
Fall time (20%-80%) $L1/LV_{DD}$ = 2.5V $L1/LV_{DD}$ = 1.8V	t_{RGTF}	-	-	- 0.75 0.54	ns	5, 6

Notes:
1. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII timing. Note that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 2.1 ns is added to the associated clock signal. Many PHY vendors already incorporate the necessary delay inside their device. If so, additional PCB delay is probably not needed.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Applies to inputs and outputs.
6. System/board must be designed to ensure this input requirement to the chip is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.
7. The frequency of ECn_RX_CLK (input) should not exceed the frequency of ECn_GTX_CLK (output) by more than 300 ppm.
8. For recommended operating conditions, see Table 4.

This figure shows the RGMII AC timing and multiplexing diagrams.

Figure 23: RGMII AC timing and multiplexing diagrams



3.11.4.2.1 Warning

Teledyne e2v guarantees timings generated from the MAC. Board designers must ensure delays needed at the PHY or the MAC.

3.11.5 XFI interface

This section describes the XFI clocking requirements and its DC and AC electrical characteristics.

3.11.5.1 XFI clocking requirements for SD*n*_REF_CLK*n*_P and SD*n*_REF_CLK*n*_N

SerDes 1 (SD1_REF_CLK[1:2]_P and SD1_REF_CLK[1:2]_N) may be used for SerDes XFI configurations based on the RCW Configuration field SRDS_PRTCL.

For more information on these specifications, see SerDes reference clocks.

3.11.5.2 XFI DC electrical characteristics

This section describes the DC electrical characteristics for XFI.

3.11.5.2.1 XFI transmitter DC electrical characteristics

This table defines the XFI transmitter DC electrical characteristics.

Table 57: XFI transmitter DC electrical characteristics (XV_{DD} = 1.35V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Output differential voltage	$V_{TX-DIFF}$	360	-	770	mV	-
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-1.14dB}$	0.6	1.1	1.6	dB	-
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-3.5dB}$	3	3.5	4	dB	-
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-4.66dB}$	4.1	4.6	5.1	dB	-
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	-
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-9.5dB}$	9	9.5	10	dB	-
Differential resistance	T_{RD}	80	100	120	Ω	-

Note:
1. For recommended operating conditions, see Table 4.

3.11.5.2.2 XFI receiver DC electrical characteristics

This table defines the XFI receiver DC electrical characteristics.

Table 58: XFI receiver DC electrical characteristics (SV_{DD} = 1.0V)[2]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input differential voltage	$V_{RX-DIFF}$	110	-	1050	mV	1
Differential resistance	R_{RD}	80	100	120	Ω	-

Notes:
1. Measured at receiver
2. For recommended operating conditions, see Table 4.

3.11.5.3 XFI AC timing specifications

This section describes the AC timing specifications for XFI.

3.11.5.3.1 XFI transmitter AC timing specifications

This table defines the XFI transmitter AC timing specifications. RefClk jitter is not included.

Table 59: XFI transmitter AC timing specifications1

Parameter	Symbol	Min	Typical	Max	Unit
Transmitter baud rate	T_{BAUD}	10.3125 - 100ppm	10.3125	10.3125 + 100ppm	Gb/s
Unit Interval	UI	-	96.96	-	ps
Deterministic jitter	D_J	-	-	0.15	UI p-p
Total jitter	T_J	-	-	0.30	UI p-p

Notes:
1. For recommended operating conditions, see Table 4.

3.11.5.3.2 XFI receiver AC timing specifications

This table defines the XFI receiver AC timing specifications. RefClk jitter is not included.

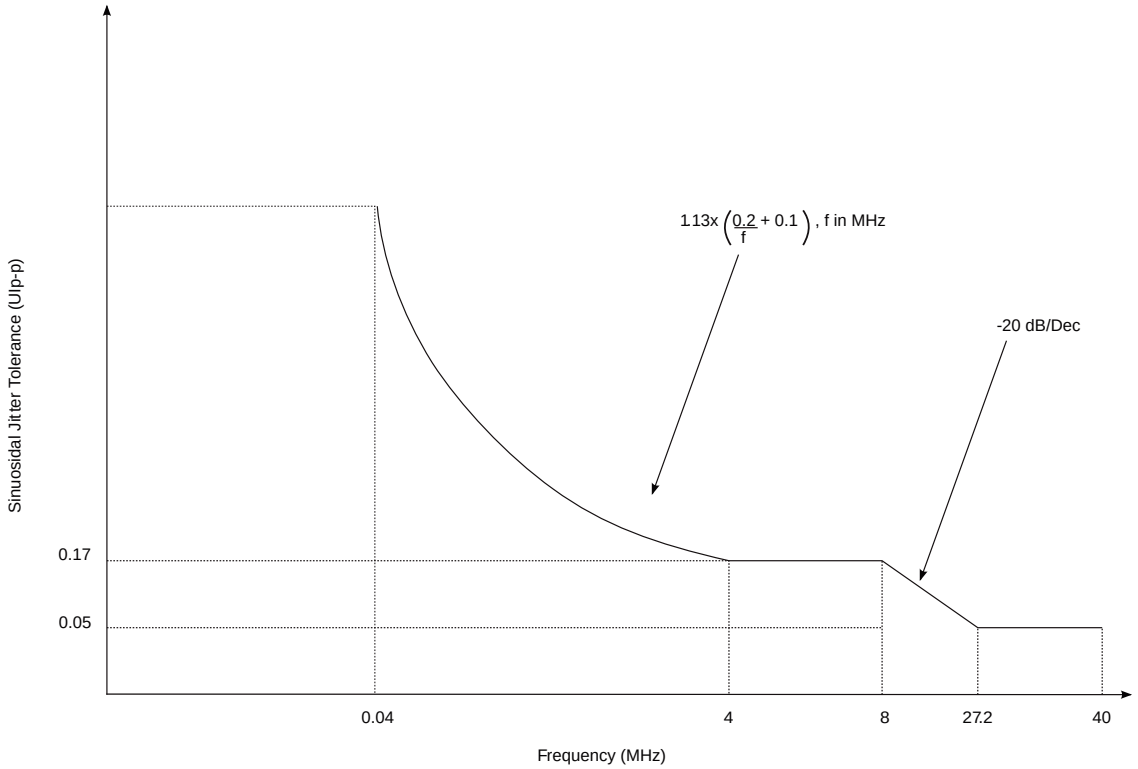
Table 60: XFI receiver AC timing specifications[3]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Receiver baud rate	R_{BAUD}	10.3125 - 100ppm	10.3125	10.3125 +100ppm	Gb/s	-
Unit Interval	UI	-	96.96	-	ps	-
Total non-EQJ jitter	$T_{NON-EQJ}$	-	-	0.45	UI p-p	1
Total jitter tolerance	T_J	-	-	0.65	UI p-p	1, 2

Notes:
1. The total jitter (TJ) consists of Random Jitter (RJ), Duty Cycle Distortion (DCD), Periodic Jitter (PJ), and Inter symbol Interference (ISI). Non-EQJ jitter can include duty cycle distortion (DCD), random jitter (RJ), and periodic jitter (PJ). Non-EQJ jitter is uncorrelated to the primary data stream with exception of the DCD and so cannot be equalized by the receiver under test. It can exhibit a wide spectrum. Non - EQJ = TJ - ISI = RJ + DCD + PJ
2. The XFI channel has a loss budget of 9.6 dB @5.5GHz. The channel loss including connector @ 5.5GHz is 6dB. The channel crosstalk and reflection margin is 3.6dB. Manual tuning of TX Equalization and amplitude will be required for performance optimization.
3. For recommended operating conditions, see Table 4.

This figure shows the sinusoidal jitter tolerance of XFI receiver.

Figure 24: XFI host receiver input sinusoidal jitter tolerance



3.11.6 10GBase-KR interface

This section describes the 10GBase-KR clocking requirements and its DC and AC electrical characteristics.

3.11.6.1 10GBase-KR clocking requirements for SD*n*_REF_CLK*n*_P and SD*n*_REF_CLK*n*_N

Only SerDes 1 (SD1_REF_CLK1_P and SD1_REF_CLK1_N) may be used for SerDes 10GBase-KR configurations based on the RCW Configuration field SRDS_PRTCL.

For more information on these specifications, see SerDes reference clocks .

3.11.6.2 10GBase-KR DC electrical characteristics

This section describes the DC electrical characteristics for 10GBase-KR.

3.11.6.2.1 10GBase-KR transmitter DC electrical characteristics

This table defines the 10GBase-KR transmitter DC electrical characteristics.

Table 61: 10GBaseKR transmitter DC electrical characteristics (XV_{DD} = 1.35V or 1.5V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Output differential voltage	$V_{TX-DIFF}$	800	-	1200	mV	-
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-1.14dB}$	0.6	1.1	1.6	dB	-
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-3.5dB}$	3	3.5	4	dB	-
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-4.66dB}$	4.1	4.6	5.1	dB	-
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	-
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-9.5dB}$	9	9.5	10	dB	-
Differential resistance	T_{RD}	80	100	120	Ω	-

Note:
1. For recommended operating conditions, see Table 4.

3.11.6.2.2 10GBase-KR receiver DC electrical characteristics

This table defines the 10GBase-KR receiver DC electrical characteristics.

Table 62: 10GBase-KR receiver DC electrical characteristics (XV_{DD} = 1.35V or 1.5V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input differential voltage	$V_{RX-DIFF}$	-	-	1200	mV	-
Differential resistance	R_{RD}	80	-	120	Ω	-

Note:
1. For recommended operating conditions, see Table 4.

3.11.6.3 10GBase-KR AC timing specifications

This section describes the AC timing specifications for 10GBase-KR.

3.11.6.3.1 10GBase-KR transmitter AC timing specifications

This table defines the 10GBase-KR transmitter AC timing specifications. RefClk jitter is not included.

Table 63: 10GBase-KR transmitter AC timing specifications[1]

Parameter	Symbol	Min	Typical	Max	Unit
Transmitter baud rate	T_{BAUD}	10.3125 - 100 ppm	10.3125	10.3125 + 100 ppm	Gb/s
Uncorrelated high probability jitter/Random jitter	U_{HPJ}/R_J	-	-	0.15	UI p-p
Deterministic jitter	D_J	-	-	0.15	UI p-p
Total jitter	T_J	-	-	0.30	UI p-p

Note:
1. For recommended operating conditions, see Table 4.

3.11.6.3.2 10GBase-KR receiver AC timing specifications

This table defines the 10GBase-KR receiver AC timing specifications. RefClk jitter is not included.

Table 64: 10GBase-KR receiver AC timing specifications[2]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Receiver baud rate	R_{BAUD}	10.3125 – 100 ppm	10.3125	10.3125 + 100 ppm	Gb/s	-
Random jitter	R_J	-	-	0.130	UI p-p	-
Sinusodial jitter, maximum	S_{J-max}	-	-	0.115	UI p-p	-
Duty cycle distortion	D_{CD}	-	-	0.035	UI p-p	-
Total jitter	T_J	-	-	See Note 1	UI p-p	1

Notes:
1. The total jitter (TJ) is per Interference tolerance test IEEE Standard 802.3ap-2007 specified in Annex 69A.
2. For recommended operating conditions, see Table 4.

3.11.7 Ethernet management interface (EMI)

This section discusses the electrical characteristics for the EMI1 interface. The EMI1 interface timing is compatible with IEEE Std 802.3™ clause 22.

3.11.7.1 Ethernet management interface 1 DC electrical characteristics

The DC electrical characteristics for EMI1_MDIO and EMI1_MDC are provided in this section. The pins are available on LV_{DD} and $L1V_{DD}$. Refer to Table 4 for operating voltages.

Table 65: Ethernet management interface 1 DC electrical characteristics ($L1V_{DD}$= 2.5 V)[3, 4]

Parameters	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x $L1V_{DD}$	-	V	1
Input low voltage	V_{IL}	-	0.2 x $L1V_{DD}$	V	1
Input high current (VIN = L1VDD)	I_{IH}	-	50	µA	2, 4
Input low current (VIN = GND)	I_{IL}	-50	-	µA	-
Output high voltage (L1VDD = min, IOH = -1.0 mA)	V_{OH}	2.00	-	V	-
Output low voltage (L1VDD = min, IOL = 1.0 mA)	V_{OL}	-	0.40	V	-

Notes:
1. The min VIL and max VIH values are based on min and max of L1VIN values found in Table 4.
2. The symbol VIN, in this case, represents the L1VIN symbols referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 4.

Table 66: Ethernet management interface 1 DC electrical characteristics($L1V_{DD}$=1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x $L1V_{DD}$	-	V	1
Input low voltage	V_{IL}	-	0.2 x $L1V_{DD}$	V	1
Input current (LVIN = 0 V or LVIN = L1VDD)	I_{IN}	-	±50	µA	2, 4
Output high voltage (L1VDD = min, IOH = -0.5 mA)	V_{OH}	1.35	-	V	4
Output low voltage (L1VDD = min, IOL = 0.5 mA)	V_{OL}	-	0.4	V	4

Notes:
1. The min V_{IL} and max VIH values are based on min and max L1VIN respective values found in Table 4.
2. The symbol LV_{IN} represents the L1VIN symbols referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 4.

3.11.7.2 Ethernet management interface 2 DC electrical characteristics

Ethernet management interface 2 pins function as open drain I/Os. The interface conforms to 1.2 V nominal voltage levels. The DC electrical characteristics for EMI2_MDIO and EMI2_MDC are provided in this section.

Table 67: Ethernet management interface 2 DC electrical characteristics (TV_{DD} = 1.2 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x TV_{DD}	-	V	-
Input low voltage	V_{IL}	-	0.2 x TV_{DD}	V	-
Output high voltage (IOH= -100 µA)	V_{OH}	1.0	-	V	-
Output low voltage (IOL = 100 µA)	V_{OL}	-	0.2	V	-
Output low current (VOL = 0.2 V)	I_{OL}	4	-	mA	-
Input capacitance	C_{IN}	-	10	pF	-

Notes:
1. For recommended operating conditions, see Table 4.

3.11.7.3 Ethernet management interface 1 AC electrical specifications

This table provides the Ethernet management interface 1 AC timing specifications.

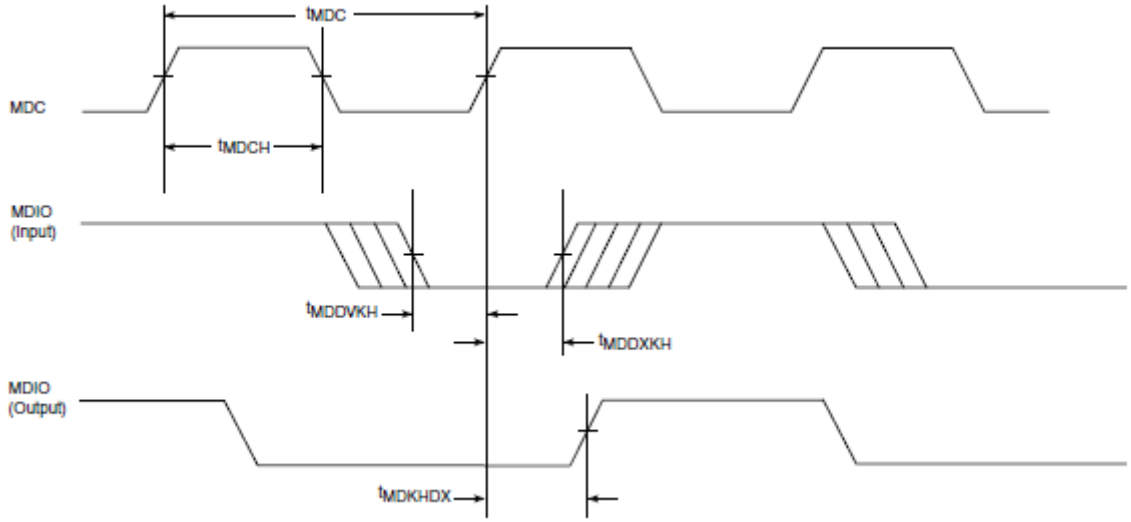
Table 68: Ethernet management interface 1 AC timing specifications[5]

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	-	-	2.5	MHz	2
MDC clock pulse width high	t_{MDCH}	160	-	-	ns	-
MDC to MDIO delay	t_{MDKHDX}	(5 x t_{enet_clk}) - 3	-	(5 x t_{enet_clk}) + 3	ns	3, 4
MDIO to MDC setup time	t_{MDDVKH}	8	-	-	ns	-
MDIO to MDC hold time	t_{MDDXKH}	0	-	-	ns	-

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, tMDDVKH symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time.
2. This parameter is dependent on the Ethernet clock frequency (MDIO_CFG [MDIO_CLK_DIV] field determines the clock frequency of the MgmtClk Clock EC_MDC).
3. This parameter is dependent on the Ethernet clock frequency. The delay is equal to 5 Ethernet clock periods ± 3 ns. For example, with an Ethernet clock of 400 MHz, the min/max delay is 12.5 ns ± 3 ns.
4. tenet_clk is the Ethernet clock period (Frame Manager clock period x 2).
5. For recommended operating conditions, see Table 4.

This figure shows the Ethernet management interface 1 timing diagram

Figure 25: Ethernet management interface 1 timing diagram



3.11.7.4 Ethernet management interface 2 AC electrical characteristics

This table provides the Ethernet management interface 2 AC timing specifications.

Table 69: Ethernet management interface 2 AC timing specifications[5]

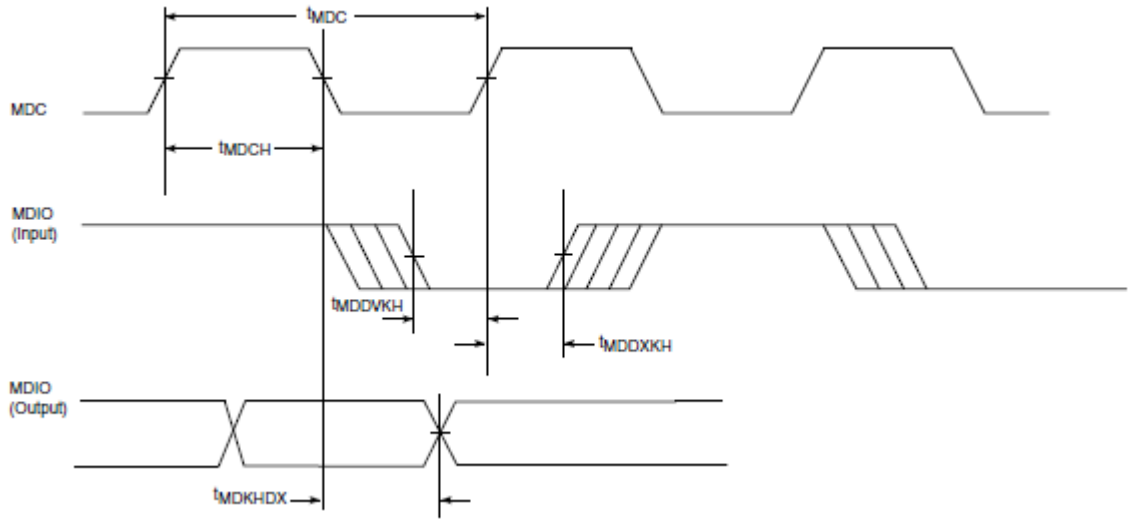
Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	-	-	2.5	MHz	2
MDC clock pulse width high	t_{MDCH}	160	-	-	ns	-
MDC to MDIO delay	t_{MDKHDX}	((Y + 5) x t_{enet_clk}) - 15	-	((Y + 5) x t_{enet_clk}) + 65	ns	3, 4, 5, 6
MDIO to MDC setup time	t_{MDDVKH}	80	-	-	ns	7
MDIO to MDC hold time	t_{MDDXKH}	0	-	-	ns	7

Notes:

1. The symbols used for timing specifications follow the pattern of t(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, tMDKHDX symbolizes management data timing (MD) for the time tMDC from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, tMDDVKH symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the tMDC clock reference (K) going to the high (H) state or setup time.
2. This parameter is dependent on the Ethernet clock frequency (MDIO_CFG [MDIO_CLK_DIV] field determines the clock frequency of the MgmtClk Clock EC_MDC).
3. tenet_clk is the Ethernet clock period (Frame Manager clock period x 2).
4. Ethernet clock period is equal to Frame Manager Clock period if Frame Manager Clock frequency is less than or equal to 600MHz. Ethernet clock period is equal to Frame Manager Clock period x 2 if Frame Manager Clock period is greater than 600MHz.
5. Y is the value programmed to adjust hold time by MDIO_CFG[EHOLD].
6. The timings are defined with respect to falling edge of MDC.
7. The timings are defined with respect to rising edge of MDC.
8. For recommended operating conditions, see Table 4.

This figure shows the Ethernet management interface 2 timing diagram

Figure 26: Ethernet management interface 2 timing diagram



3.11.8 IEEE 1588 electrical specifications

3.11.8.1 IEEE 1588 DC electrical characteristics

This table shows IEEE 1588 DC electrical characteristics when operating at LV_{DD} = 2.5 V supply.

Table 70: IEEE 1588 DC electrical characteristics(LV_{DD} = 2.5 V)[3]

Parameters	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x LV_{DD}	-	V	1
Input low voltage	V_{IL}	-	0.2 x LV_{DD}	V	1
Input current (LVIN= 0 V or LVIN= LVDD)	I_{IH}	-	±50	µA	2
Output high voltage (LVDD = min, IOH = -1.0 mA)	V_{OH}	2.00	-	V	-
Output low voltage (LVDD = min, IOL = 1.0 mA)	V_{OL}	-	0.40	V	-

Notes:
1. The min VIL and max VIH values are based on the respective min and max LVIN values found in Table 2.
2. The symbol LVIN, in this case, represents the LVIN symbol referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 4.

This table shows IEEE 1588 DC electrical characteristics when operating at LV_{DD} = 1.8 V supply.

Table 71: IEEE 1588 DC electrical characteristics(LV_{DD} = 1.8 V)[3]

Parameters	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x LV_{DD}	-	V	1
Input low voltage	V_{IL}	-	0.2 x LV_{DD}	V	1
Input current (LVIN= 0 V or LVIN= LVDD)	I_{IH}	-	±50	µA	2
Output high voltage (LVDD = min, IOH = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (LVDD = min, IOL = 0.5 mA)	V_{OL}	-	0.40	V	-

Notes:
1. The min VIL and max VIH values are based on the respective min and max LVIN values found in Table 4.
2. The symbol LVIN, in this case, represents the LVIN symbol referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 4.

3.11.8.2 IEEE 1588 AC specifications

This table provides the IEEE 1588 AC timing specifications.

Table 72: IEEE 1588 AC timing specifications5

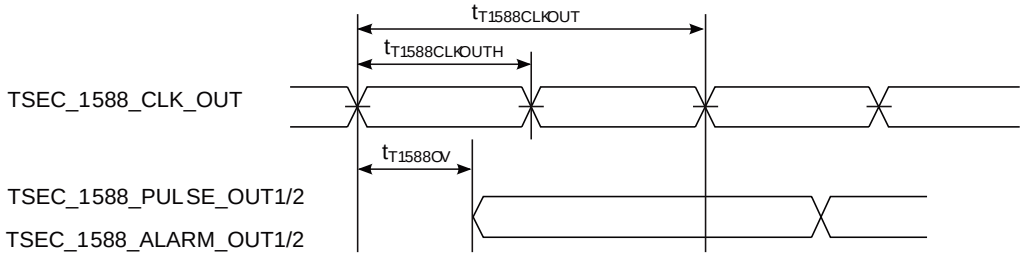
Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
TSEC_1588_CLK_IN clock period	$t_{T1588CLK}$	FM_CLK/2	-	T_{RX_CLK} x	ns	1, 3
TSEC_1588_CLK_IN duty cycle	$t_{T1588CLKH}$/ $t_{T1588CLK}$	40	50	60	%	2
TSEC_1588_CLK_IN peak-to-peak jitter	$t_{T1588CLKINJ}$	-	-	250	ps	-
Rise time TSEC_1588_CLK_IN (20%-80%)	$t_{T1588CLKINR}$	1.0	-	2.0	ns	-
Fall time TSEC_1588_CLK_IN (80%-20%)	$t_{T1588CLKINF}$	1.0	-	2.0	ns	-
TSEC_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	5.0	-	-	ns	4
TSEC_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}$/ $t_{T1588CLKOUT}$	30	50	70	%	-
TSEC_1588_PULSE_OUT1/2, TSEC_1588_ALARM_OUT1/2	$t_{T1588OV}$	0.5	-	3.0	ns	-
TSEC_1588_TRIG_IN1/2 pulse width	$t_{T1588TRIGH}$	2 x $t_{T1588CLK\_MAX}$	-	-	ns	3

Notes:

1. TRX_CLK is the maximum clock period of Ethernet receiving clock selected by TMR_CTRL[CKSEL]. See the chip reference manual for a description of TMR_CTRL registers.
2. It needs to be at least two times the clock period of the clock selected by TMR_CTRL[CKSEL]. See the chip reference manual for a description of TMR_CTRL registers.
3. The maximum value of tT1588CLK is not only defined by the value of TRX_CLK, but also defined by the recovered clock. For example, for 10/100/1000 Mbps modes, the maximum value of tT1588CLK will be 2800, 280, and 56 ns, respectively.
4. There are 3 input clock sources for 1588 that is, TSEC_1588_CLK_IN, RTC and MAC clock / 2. When using TSEC_1588_CLK_IN, the minimum clock period is 2 x tT1588CLK.
5. For recommended operating conditions, see Table 4.

This figure shows the data and command output AC timing diagram.

Figure 27: IEEE 1588 output AC timing

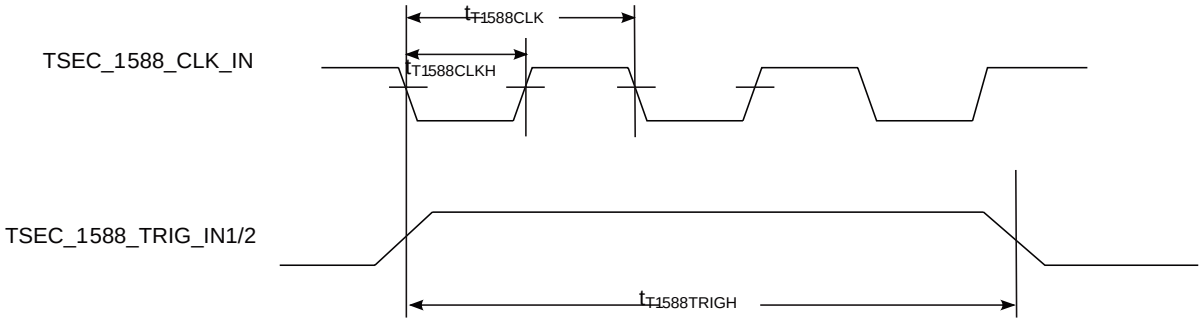


Note: The output delay is counted starting at the rising edge if $t_{T1588CLKOUT}$ is non-inverting. Otherwise, it is counted starting at the falling edge.

Note: The output delay is counted starting at the rising edge if tT1588CLKOUT is non-inverting. Otherwise, it is counted starting at the falling edge.

This figure shows the data and command input AC timing diagram.

Figure 28: IEEE 1588 input AC timing



3.12 QUICC Engine Specifications

3.12.1 HDLC, Transparent, and Synchronous UART interfaces

This section describes the DC and AC electrical specifications for the high level data link control HDLC, transparent and synchronous UART.

3.12.1.1 HDLC, Transparent and Synchronous UART DC electrical characteristics

This table provides the DC electrical characteristics for the HDLC, Transparent and Synchronous UART protocols.

Table 73: HDLC, Transparent and Synchronous UART DC electrical characteristics (DVDD = 3.3V)

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	-	V	1
Input low voltage	V_{IL}	-	0.2 x DV_{DD}	V	1
Input current (VIN = 0 V or VIN = DVDD)	I_{IN}	-	±50	µA	2
Output high voltage (DVDD = min, IOH = -2 mA)	V_{OH}	2.4	-	V	-
Output low voltage (DVDD = min, IOH = 2 mA)	V_{OL}	-	0.4	V	-

Notes:
1. The min VIL and max VIH values are based on the respective min and max BV_{IN} values found in Table 4.
2. The symbol V_{IN}, in this case, represents the input voltage of the supply. It is referenced in Recommended operating Table 4: “.
3. For recommended operating conditions, see Table 4.

This table provides the DC electrical characteristics for the HDLC, Transparent and Synchronous UART protocols.

Table 74: HDLC, Transparent and Synchronous UART DC electrical characteristics (DVDD = 2.5V)

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	-	V	1
Input low voltage	V_{IL}	-	0.2 x DV_{DD}	V	1
Input current (V_{IN} = 0 V or V_{IN} = DV_{DD})	I_{IN}	-	±50	µA	2
Output high voltage (DV_{DD} = min, I_{OH} = -1 mA)	V_{OH}	2.0	-	V	-
Output low voltage (DV_{DD} = min, I_{OH} = 1 mA)	V_{OL}	-	0.4	V	-

Notes:
1. The min VIL and max VIH values are based on the respective min and max BVIN values found in Table 4.
2. The symbol VIN, in this case, represents the input voltage of the supply. It is referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 4.

3.12.1.2 HDLC, Transparent and Synchronous UART AC timing specifications

This table provides the input and output AC timing specifications for HDLC, and Transparent and Synchronous UART protocols.

Table 75: HDLC, Transparent AC timing specifications

Parameter	Symbol	Min	Max	Unit	Notes
Outputs-Internal clock delay	t_{HIKHOV}	0	5.5	ns	1
Outputs-External clock delay	t_{HEKHOV}	1	9	ns	1
Outputs-Internal clock High Impedance	t_{HIKHOX}	0	5.5	ns	1
Outputs-External clock High Impedance	t_{HEKHOX}	1	8	ns	1
Inputs-Internal clock input setup time	t_{HIIVKH}	8	-	ns	-
Inputs-External clock input setup time	t_{HEIVKH}	4	-	ns	-
Inputs-Internal clock input Hold time	t_{HIIXKH}	0	-	ns	-
Inputs-External clock input hold time	t_{HEIXKH}	1.27	-	ns	-

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. For recommended operating conditions, see Table 4.

This table provides the input and output AC timing specifications for the synchronous UART protocols.

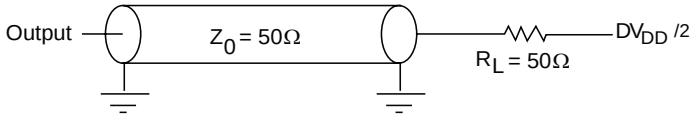
Table 76: Synchronous UART AC timing specifications

Parameter	Symbol	Min	Max	Unit	Notes
Outputs-Internal clock delay	t_{HIKHOV}	0	11	ns	1
Outputs-External clock delay	t_{HEKHOV}	1	14	ns	1
Outputs-Internal clock High Impedance	t_{HIKHOX}	0	11	ns	1
Outputs-External clock High Impedance	t_{HEKHOX}	1	14	ns	1
Inputs-Internal clock input setup time	t_{HIIVKH}	10	-	ns	-
Inputs-External clock input setup time	t_{HEIVKH}	8	-	ns	-
Inputs-Internal clock input Hold time	t_{HIIXKH}	0	-	ns	-
Inputs-External clock input hold time	t_{HEIXKH}	1	-	ns	-

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. For recommended operating conditions, see Table 4.

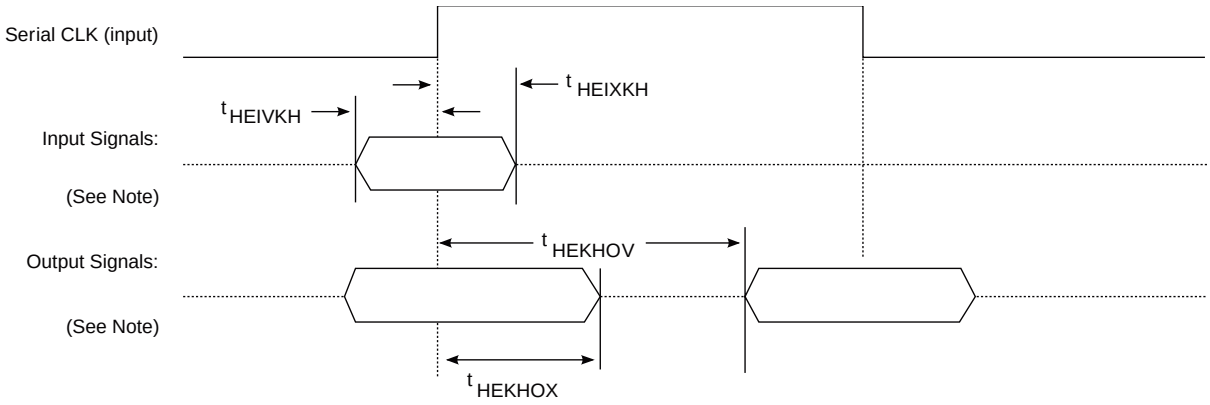
This figure provides the AC test load.

Figure 29: AC test load



These figures represent the AC timing from Table 75 and Table 76. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge. This figure shows the timing with external clock.

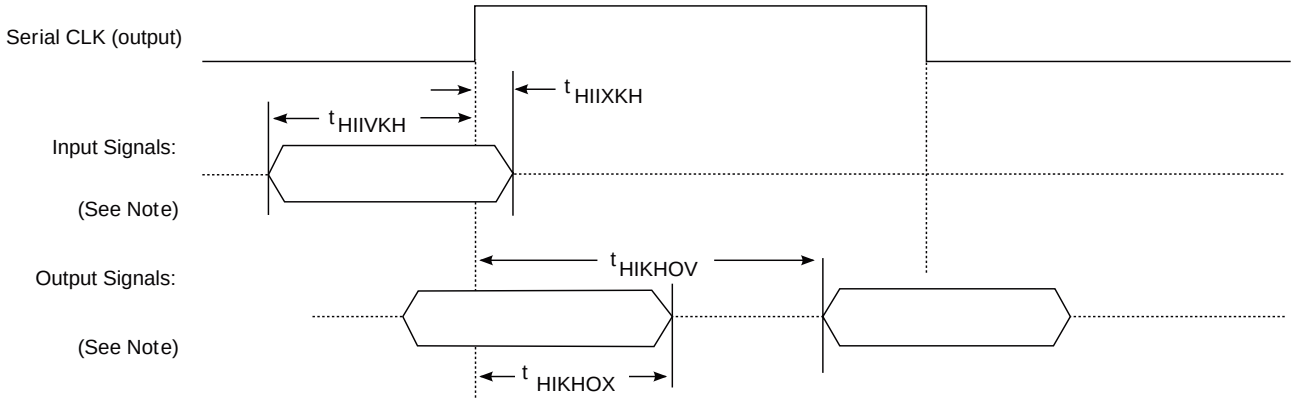
Figure 30: AC timing (external clock) diagram



Note: The clock edge is selectable

This figure shows the timing with internal clock.

Figure 31: AC timing (internal clock) diagram



Note: The clock edge is selectable

3.12.2 TDM/SI

This section describes the DC and AC electrical specifications for the time-division- multiplexed and serial interface (TDM/SI).

3.12.2.1 TDM/SI DC electrical characteristics

This table provides the TDM/SI DC electrical characteristics.

Table 77: TDM/SI DC electrical characteristics (DVDD=3.3V)

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	-	V	1
Input low voltage	V_{IL}	-	0.2 x DV_{DD}	V	1
Input current (VIN = 0 V or VIN = DVDD)	I_{IN}	-	±50	µA	2
Output high voltage (DVDD = min, IOH = -2 mA)	V_{OH}	2.4	-	V	-
Output low voltage (DVDD = min, IOH = 2 mA)	V_{OL}	-	0.4	V	-

Notes:

1. The min VIL and max VIH values are based on the respective min and max BVIN values found in Table 4.
2. The symbol VIN, in this case, represents the input voltage of the supply. It is referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 4.

Table 78: TDM/SI DC electrical characteristics (DVDD=2.5V)

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	-	V	1
Input low voltage	V_{IL}	-	0.2 x DV_{DD}	V	1
Input current (V_{IN} = 0 V or V_{IN} = DV_{DD})	I_{IN}	-	±50	µA	2
Output high voltage (DV_{DD} = min, I_{OH} = -1 mA)	V_{OH}	2.0	-	V	-
Output low voltage (DV_{DD} = min, I_{OH} = 1 mA)	V_{OL}	-	0.4	V	-

Notes:
1. The min VIL and max VIH values are based on the respective min and max BVIN values found in Table 4.
2. The symbol VIN, in this case, represents the input voltage of the supply. It is referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 4.

TDM/SI AC timing specifications

This table provides the TDM/SI input and output AC timing specifications.

Table 79: TDM/SI AC timing specifications [1]

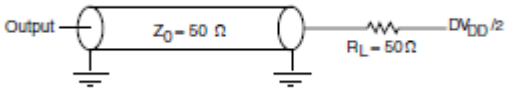
Parameter	Symbol [1]	Min	Max	Unit
TDM/SI outputs-External clock delay	t_{SEKHOV}	2	11	ns
TDM/SI outputs-External clock High Impedance	t_{SEKHOX}	2	10	ns
TDM/SI inputs-External clock input setup time	t_{SEIVKH}	5	-	ns
TDM/SI inputs-External clock input hold time	t_{SEIXKH}	2	-	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. For recommended operating conditions, see Table 4.

Note:
The rise/fall time on QUICC Engine block input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of DV_{DD}; fall time refers to transitions from 90% to 10% of DV_{DD}

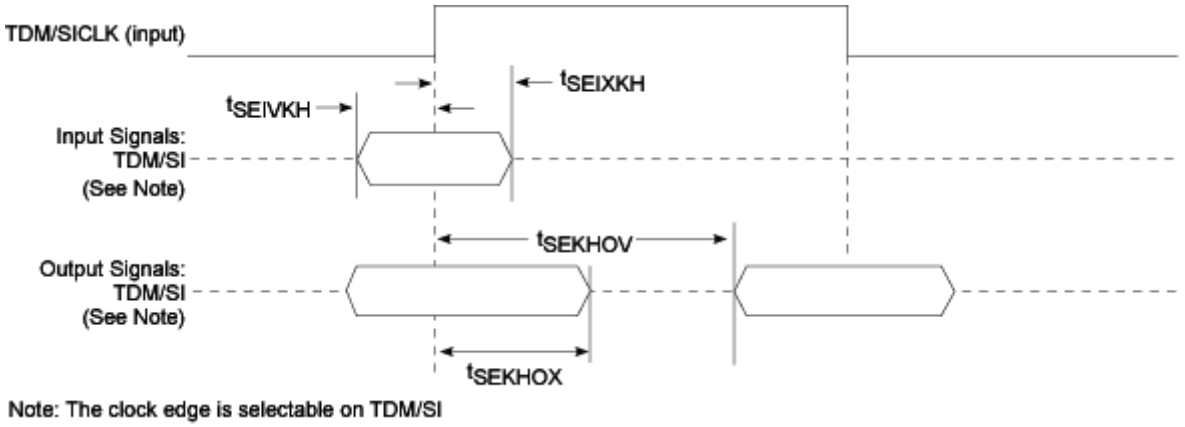
This figure provides the AC test load for the TDM/SI.

Figure 32: TDM/SI AC test load



This figure represents the AC timing from Table 79. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge. This figure shows the TDM/SI timing with external clock.

Figure 33: TDM/SI AC timing (external clock) diagram



3.13 USB interface

This section provides the AC and DC electrical specifications for the USB interface.

3.13.1 USB DC electrical characteristics

This table provides the DC electrical characteristics for the USB interface at USB_HV_{DD} = 3.3 V.

Table 80: USB DC electrical characteristics (USB_HV_{DD} = 3.3 V) [3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	-	V	1
Input low voltage	V_{IL}	-	0.8	V	1
Input current (USB_HV_{IN} = 0 V or USB_HV_{IN}= USB_HV_{DD})	I_{IN}	-	±50	µA	2
Output high voltage (USB_HV_{DD} = min, I_{OH} = -2 mA)	V_{OH}	2.8	-	V	-
Output low voltage (USB_HV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	-	0.3	V	-

Notes:
1. The min VIL and max VIH values are based on the respective min and max USB_HVIN values found in Table 4.
2. The symbol USB_HVIN, in this case, represents the USB_HVIN symbol referenced in Recommended operating conditions
3. For recommended operating conditions, see Table 4.

This table provides the DC electrical characteristics for the USBCLK at $O1V_{DD}$ = 1.8 V.

Table 81: USBCLK DC electrical characteristics (1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	-	V	1
Input low voltage	V_{IL}	-	0.6	V	1
Input current (V_{IN} = 0 V or V_{IN} = $O1V_{DD}$)	I_{IN}	-	±50	µA	2

Notes:
1. The min VIL and max VIH values are based on the respective min and max O1VIN values found in Table 4.
2. The symbol VIN, in this case, represents the O1VIN symbol referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 4.

3.13.2 USB AC timing specifications

This section describes the AC timing specifications for the on-chip USB PHY. See Chapter 7 in the *Universal Serial Bus Revision 2.0 Specification* for more information.

This table provides the USB clock input (USBCLK) AC timing specifications.

Table 82: USBCLK AC timing specifications[1]

Parameter	Condition	Symbol	Min	Typ	Max	Unit	Notes
Frequency range	-	$f_{USB\_CLK\_IN}$	-	24	-	MHz	-
Rise/Fall time	Measured between 10% and 90%	t_{USRF}	-	-	6	ns	2
Clock frequency tolerance	-	t_{CLK_TOL}	-0.005	0	0.005	%	-
Reference clock duty cycle	Measured at rising edge and/or failing edge at $O1V_{DD}/2$	t_{CLK_DUTY}	40	50	60	%	-
Total input jitter/time interval error	RMS value measured with a second-order, band-pass filter of 500 kHz to 4 MHz bandwidth at 10^{-12} BER	t_{CLK_PJ}	-	-	5	ps	-

Notes:
1. For recommended operating conditions, see Table 4.
2. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

3.14 Integrated flash controller

This section describes the DC and AC electrical specifications for the integrated flash controller.

3.14.1 Integrated flash controller DC electrical characteristics

This table provides the DC electrical characteristics for the integrated flash controller when operating at OV_{DD}= 1.8 V.

Table 83: Integrated flash controller DC electrical characteristics (1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.25	-	V	1
Input low voltage	V_{IL}	-	0.6	V	1
Input current (V_{IN} = 0 V or V_{IN} = OV_{DD})	I_{IN}	-	±50	µA	2
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.6	-	V	-
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.32	V	-

Notes:
1. The min VIL and max VIH values are based on the respective min and max OVIN values found in Table 4.
2. The symbol VIN, in this case, represents the OVIN symbol referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 4.

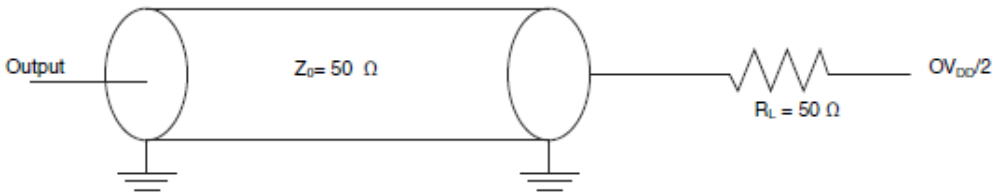
3.14.2 Integrated flash controller AC timing

This section describes the AC timing specifications for the integrated flash controller.

3.14.2.1 Test condition

This figure provides the AC test load for the integrated flash controller.

Figure 34: Integrated flash controller AC test load



3.14.2.2 Integrated flash controller Input AC timing specifications

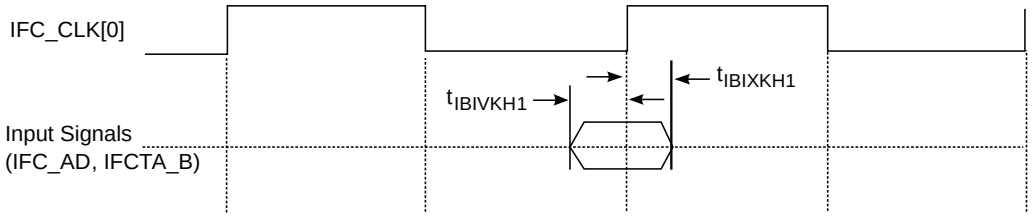
This table describes the input AC timing specifications of the IFC-GPCM and IFC- GASIC interface.

Table 84: Integrated Flash Controller input timing specifications for GPCM and GASIC mode (OVDD = 1.8 V)

Parameter	Symbol	Min	Max	Unit	Notes
Input setup	$t_{IBIVKH1}$	4	-	ns	-
Input hold	$t_{IBIXKH1}$	1	-	ns	-

This figure shows the input AC timing diagram for IFC-GPCM, IFC-GASIC interface.

Figure 35: IFC-GPCM, IFC-GASIC input AC timings



This table describes the input timing specifications of the IFC-NOR interface.

Table 85: Integrated Flash Controller Input timing specifications for NOR mode (OV_{DD} = 1.8 V)

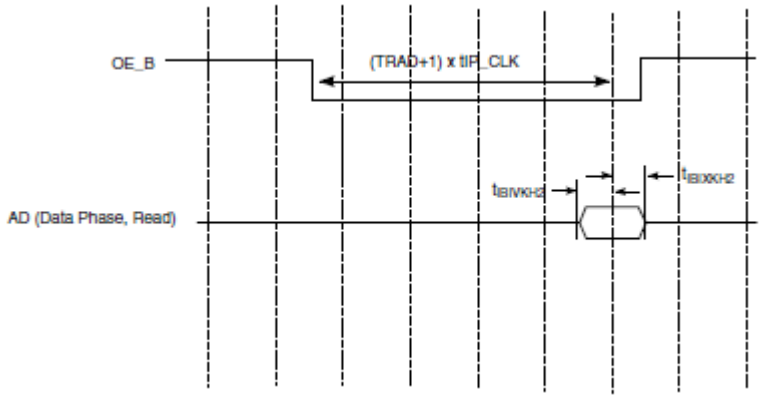
Parameter	Symbol	Min	Max	Unit	Notes
Input setup	$t_{IBIVKH2}$	(2 x t_{IP_CLK}) + 2	-	ns	1
Input hold	$t_{IBIXKH2}$	1 x t_{IP_CLK}	-	ns	1

Note:

1. t_{IP_CLK} is the period of ip clock (not the IFC_CLK) on which IFC is running.
2. For recommended operating conditions, see Table 4.

This figure shows the AC input timing diagram for input signals of IFC-NOR interface. Here TRAD is a programmable delay parameter, refer to IFC section of T1024 QorIQ Integrated Processor Reference Manual for more information.

Figure 36: IFC-NOR Interface input AC timings



IP_CLK is the internal clock on which IFC is running. It is not available on interface pins.

This table describes the input timing specifications of the IFC-NAND interface.

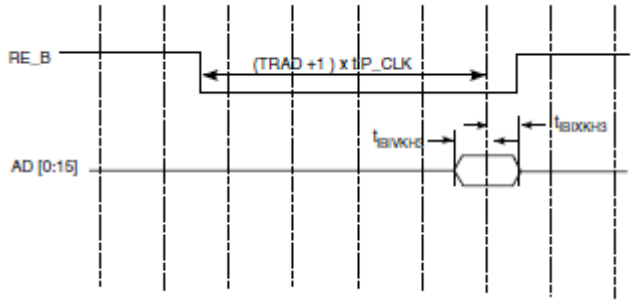
Table 86: Integrated Flash Controller input timing specifications for NAND mode (OV_{DD} = 1.8 V)

Parameter	Symbol	Min	Max	Unit	Notes
Input setup	$t_{IBIVKH3}$	(2 x t_{IP_CLK}) +2	-	ns	1
Input hold	$t_{IBIXKH3}$	(1 x t_{IP_CLK})	-	ns	1
IFC_RB_B pulse width	t_{IBCH}	2	-	t_{IP_CLK}	1

Notes:
1. t_{IP_CLK} is the period of ip clock on which IFC is running.
2. For recommended operating conditions, see Table 4.

This figure shows the AC input timing diagram for input signals of IFC-NAND interface. Here TRAD is a programmable delay parameter, refer to IFC section of T1024 QorIQ Integrated Processor Reference Manual for more information.

Figure 37: IFC-NAND Interface input AC timings



t_{IP_CLK} is the period of ip clock (not the IFC_CLK) on which IFC is running.

3.14.2.3 Integrated flash controller output AC timing specifications

This table describes the output AC timing specifications of IFC-GPCM and IFC-GASIC interface .

Table 87: Integrated Flash Controller IFC-GPCM and IFC-GASIC interface output timing specifications (OVDD = 1.8 V)

Parameter	Symbol	Min	Max	Unit	Notes
IFC_CLK cycle time	t_{IBK}	10	-	ns	-
IFC_CLK duty cycle	t_{IBKH}/ t_{IBK}	45	55	%	-
Output delay	$t_{IBKLOV1}$	-	1.5	ns	-
Output hold	t_{IBKLOX}	-	-2	ns	1
IFC_CLK[0] to IFC_CLK[m] skew	$t_{IBKSKEW}$	0	±75	ps	-

Notes:
1. Output hold is negative. This means that output transition happens earlier than the falling edge of IFC_CLK.
2. For recommended operating conditions, see Table 4.

This figure shows the output AC timing diagram for IFC-GPCM, IFC-GASIC interface.

Figure 38: IFC-GPCM, IFC-GASIC Signals

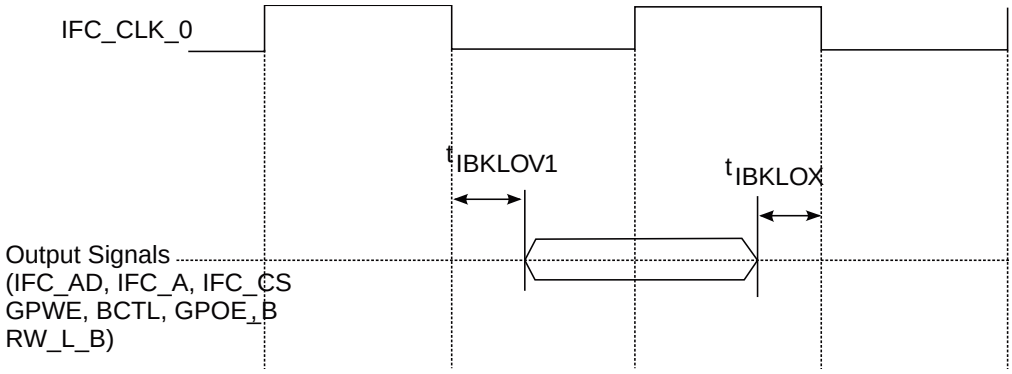


Table 88: Integrated Flash Controller IFC-NOR Interface output timing specifications (OV_{DD} = 1.8 V)

Parameter	Symbol	Min	Max	Unit	Notes
Output delay	$t_{IBKLOV2}$	-	±1.5	ns	1

Notes:
1. This effectively means that a signal change may appear anywhere within ±tIBKLOV2 (max) duration, from the point where it's expected to change.
2. For recommended operating conditions, see Table 4.

This figure shows the AC timing diagram for output signals of IFC-NOR interface. The timing specs have been illustrated here by taking timings between two signals, CS_B and OE_B as an example. OE_B is suppose to change TACO (a programmable delay, refer to IFC section of T1024 QorIQ Integrated Processor Reference Manual for more information) time after CS_B. Because of skew between the signals, OE_B may change anywhere within time window $t_{IBKLOV2}$ (min) and $t_{IBKLOV2}$ (max). This concept applies to other output signals of IFC-NOR interface as well.

Figure 39: IFC-NOR Interface Output AC Timings

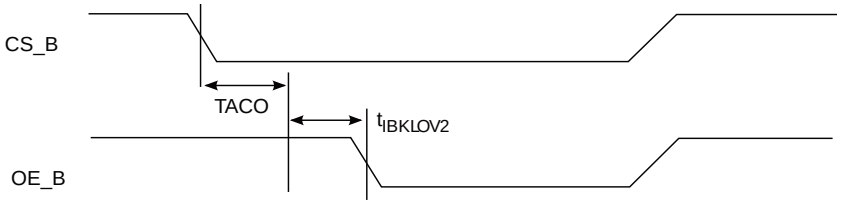


Table 89: Integrated Flash Controller IFC-NAND Interface output timing specifications (OV_{DD} = 1.8 V)

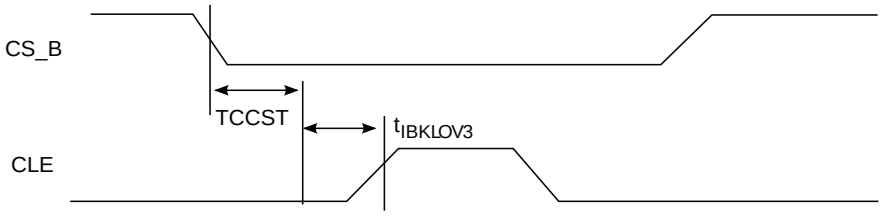
Parameter	Symbol	Min	Max	Unit	Notes
Output delay	$t_{IBKLOV3}$	-	±1.5	ns	1

Notes:

1. This effectively means that a signal change may appear anywhere within tIBKLOV3 (min) to tIBKLOV3 (max) duration, from the point where it's expected to change.
2. For recommended operating conditions, see Table 4.

This figure shows the AC timing diagram for output signals of IFC-NAND interface. The timing specs have been illustrated here by taking timings between two signals, CS_B and CLE as an example. CLE is suppose to change TCCST (a programmable delay, refer to IFC section of T1024 QorIQ Integrated Processor Reference Manual for more information) time after CS_B. Because of skew between the signals CLE may change anywhere within time window $t_{IBKLOV3}$ (min) and $t_{IBKLOV3}$ (max). This concept applies to other output signals of IFC-NAND interface as well.

Figure 40: IFC-NAND Interface Output AC Timings



3.14.2.4 Integrated flash controller NAND Source Synchronous Interface AC timing specifications

This table describes the AC timing specifications of IFC-NAND Source Synchronous interface.

Table 90: Integrated Flash Controller IFC-NAND Source Synchronous Interface AC Timing Specifications (OV_{DD} = 1.8V)

Parameter	Symbol	I/O	Min	Max	Unit	Notes
Command/address DQ hold time	t_{CAH}	O	2.5	-	ns	-
CLE and ALE hold time	t_{CALH}	O	2.5	-	ns	-
CLE and ALE setup time	t_{CALS}	O	2.5	-	ns	-
Command/address DQ setup time	t_{CAS}	O	2.5	-	ns	-
CE# hold time	t_{CH}	O	2.5	-	ns	-
Data DQ setup time	t_{DS}	O	1	-	ns	-
Data DQ hold time	t_{DH}	O	1	-	ns	-
Average clock cycle time	t_{CK}(avg) or t_{CK}	O	10	-	ns	1
Absolute clock period	t_{CK}(abs)	O	9.5	10.5	ns	-
Clock cycle high	t_{CKH}(abs)	O	0.44	0.56	t_{CK}	2
Clock cycle low	t_{CKL}(abs)	O	0.44	0.56	t_{CK}	-
DQS output high pulse width	t_{DQSH}	O	0.43	0.57	t_{CK}	3
DQS output low pulse width	t_{DQSL}	O	0.43	0.57	t_{CK}	3
DQS-DQ skew, DQS to last DQ valid, per access	t_{DQSQ}	I	-	1	ns	-
Data output to first DQS latching transition	t_{DQSS}	O	0.75 + 100 (ps)	1.25 - 150 (ps)	t_{CK}	-
DQS cycle time	t_{DSC}	O	10	-	ns	-
DQS falling edge to CLK rising – hold time	t_{DSH}	O	0.2 + 150 (ps)	-	t_{CK}	-
DQS falling edge to CLK rising – setup time	t_{DSS}	O	0.2 + 150 (ps)	-	t_{CK}	-
Input data valid window	t_{DVW}	I	2.1	-	ns	-
Half-clock period	t_{HP}	O	4.4	-	ns	-
The deviation of a given t_{CK}(abs) from t_{CK}(avg)	t_{JIT}(per)	O	-0.5	0.5	ns	-
DQ-DQS hold, DQS to first DQ to go non-valid, per access	t_{QH}	I	3.1	-	ns	-

Notes:

1. $t_{CK(avg)}$ is the average clock period over any consecutive 200 cycle window.
2. $t_{CKH(abs)}$ and $t_{CKL(abs)}$ include static off set and duty cycle jitter.
3. t_{DQSL} and t_{DQSH} are relative to t_{CK} when CLK is running . If CLK is stopped during data input, then t_{DQSL} and t_{DQSH} are relative to t_{DSC}.
4. For recommended operating conditions, see Table 4.

These figures show the AC timing diagram for IFC-NAND source synchronous interface.

Figure 41: Command Cycle

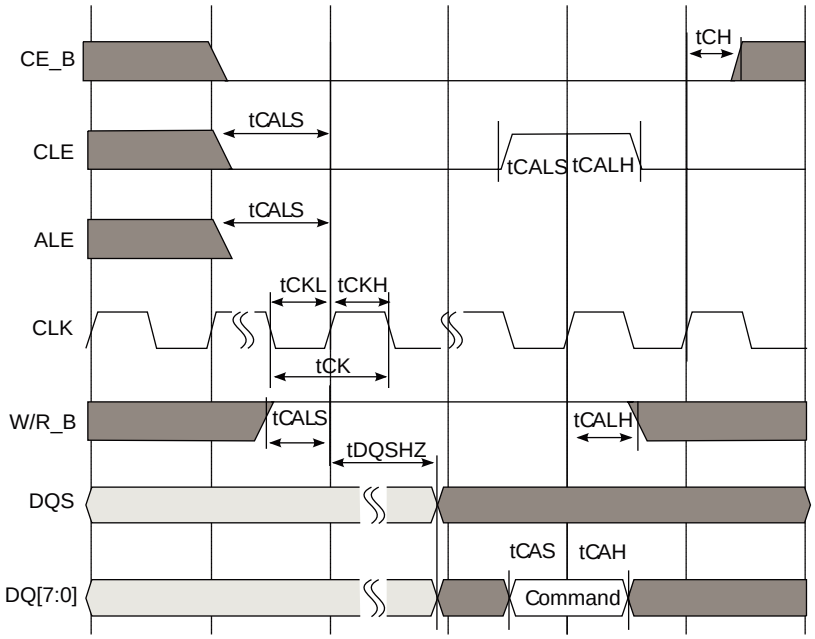


Figure 42: Address Cycle

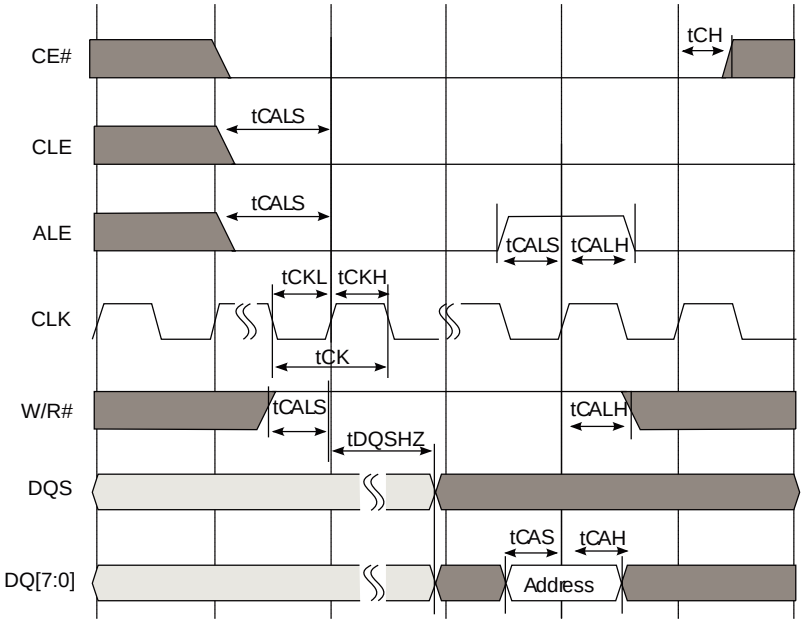


Figure 43: Write Cycle

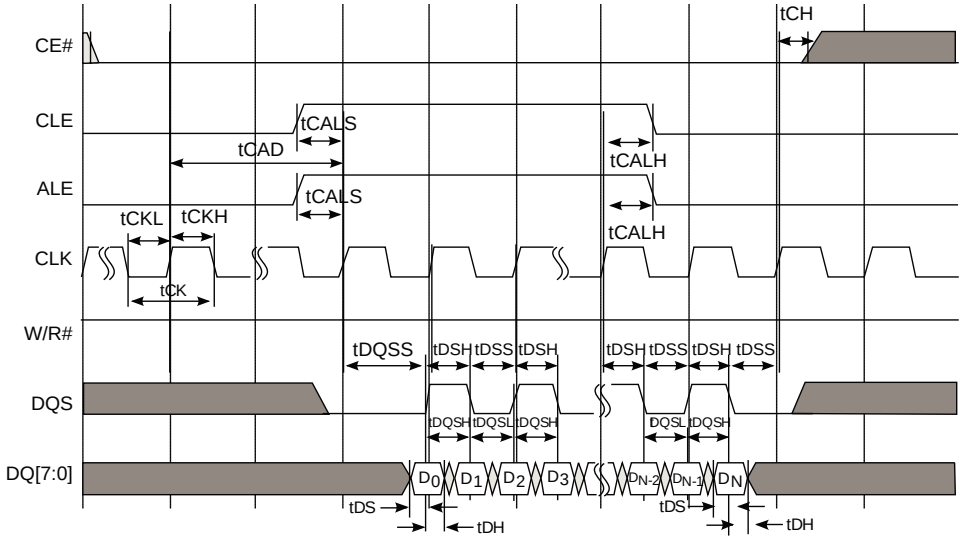
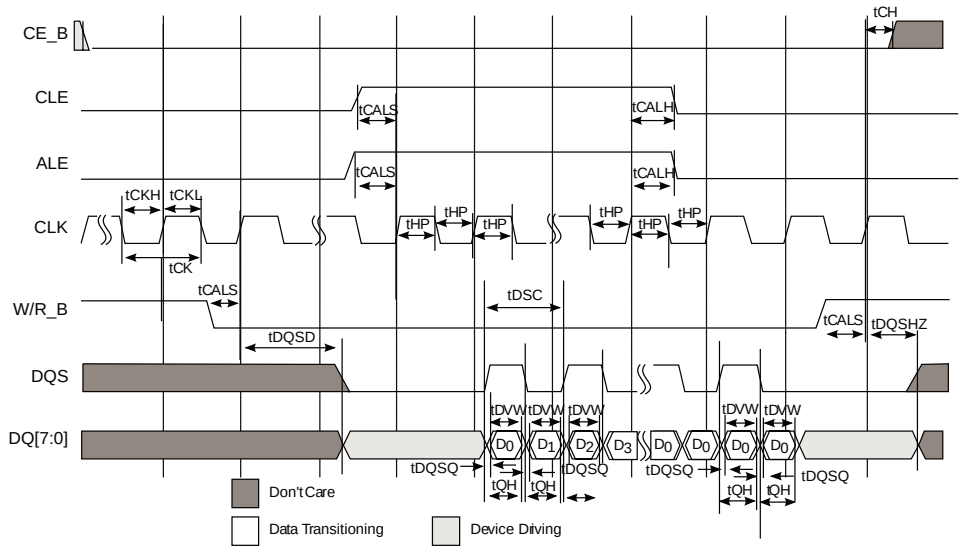


Figure 44: Read Cycle



3.15 Enhanced secure digital host controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC interface.

3.15.1 eSDHC DC electrical characteristics

This table provides the DC electrical characteristics for the eSDHC interface.

Table 91: eSDHC interface DC electrical characteristics (dual-voltage cards)[3]

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Input high voltage	V_{IH}	-	0.7 x V_{DD}	-	V	1
Input low voltage	V_{IL}	-	-	0.2 x V_{DD}	V	1
Input/Output leakage current	I_{IN}/I_{OZ}	-	-50	50	µA	-
Output high voltage	V_{OH}	I_{OH} = -100 µA at V_{DD} min	V_{DD} - 0.2 V	-	V	-
Output low voltage	V_{OL}	I_{OL}= 100 µA at V_{DD} min	-	0.2	V	-
Output high voltage	V_{OH}	I_{OH} = -100 µA	V_{DD} - 0.2	-	V	2
Output low voltage	V_{OL}	I_{OL} = 2 mA	-	0.3	V	2

Notes:
1. The min VIL and VIH values are based on the respective min and max VIN values found in Table 4.
2. Open-drain mode is for MMC cards only.
3. For recommended operating conditions, see Table 4.

SDHC interface is powered by EV_{DD} and CV_{DD}. The V_{DD} and V_{IN} in the table above should be replaced by the respective IO power supply.

3.15.2 eSDHC AC timing specifications

This table provides the eSDHC AC timing specifications as defined in Figure 45 and Figure 46 (EV_{DD}/CV_{DD} = 1.8V or 3.3V).

Table 92: eSDHC AC timing specifications (High Speed/Full Speed)[6]

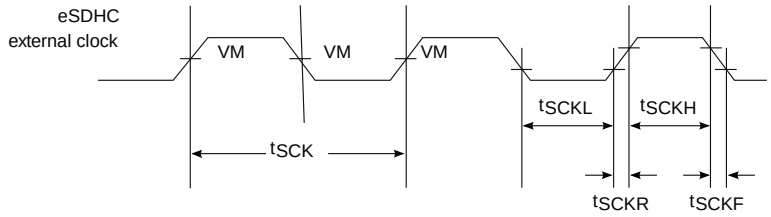
Parameter		Symbol1	Min	Max	Unit	Notes
SDHC_CLK clock frequency	SD/SDIO (full-speed/high-speed mode)	f_{SCK}	0	25/50	MHz	2, 4
	MMC full-speed/high-speed mode			20/52		
SDHC_CLK clock low time (full-speed/high-speed mode)		t_{SCKL}	10/7	–	ns	4
SDHC_CLK clock high time (full-speed/high-speed mode)		t_{SCKH}	10/7	–	ns	4
SDHC_CLK clock rise and fall times		t_{SCKR}/ t_{SCKF}	–	3	ns	4
Input setup times: SDHC_CMD, SDHC_DATx, SDHC_CD to SDHC_CLK		t_{NIIVKH}	2.5	–	ns	3, 4, 5
Input hold times: SDHC_CMD, SDHC_DATx, SDHC_CD to SDHC_CLK		t_{NIIXKH}	2.5	–	ns	4, 5
Output hold time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid		t_{NIKHOX}	-3	–	ns	4, 5
Output delay time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid		t_{NIKHOV}	–	3	ns	4, 5

Notes:
1. The symbols used for timing specifications herein follow the pattern of t(first three letters of functional block)(signal)(state) (reference)(state) for inputs and (first three letters of functional block)(reference)(state)(signal)(state) for outputs. For example, tFHSKHOV symbolizes eSDHC high-speed mode device timing (SHS) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2. In full-speed mode, the clock frequency value can be 0-25 MHz for an SD/SDIO card and 0-20 MHz for an MMC card. In high-speed mode, the clock frequency value can be 0-50 MHz for an SD/SDIO card and 0-52 MHz for an MMC card.
3. To satisfy setup timing, one-way board-routing delay between Host and Card, on SDHC_CLK, SDHC_CMD, and SDHC_DATx should not exceed 1 ns for any high speed MMC card. For any high speed or default speed mode SD card, the one way board routing delay between Host and Card, on SDHC_CLK, SDHC_CMD, and SDHC_DATx should not exceed 1.5ns.
4. CCARD ≤ 10 pF, (1 card), and CL = CBUS + CHOST + CCARD ≤ 40 pF.
5. The parameter values apply to both full-speed and high-speed modes.
6. For recommended operating conditions, see Table 4.

This figure provides the eSDHC clock input timing diagram.

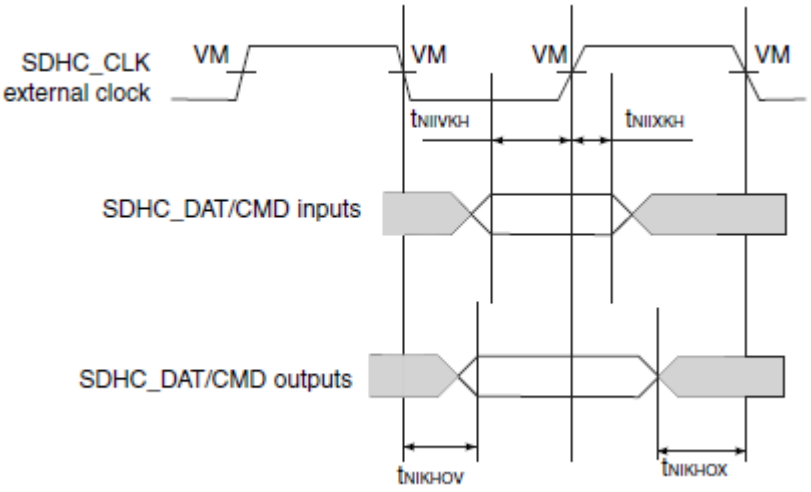
Figure 45: eSDHC clock input timing diagram



VM = Midpoint voltage ($OV_{DD}/2$)

This figure provides the data and command input/output timing diagram.

Figure 46: eSDHC data and command input/output timing diagram referenced to clock



VM = Midpoint voltage ($OV_{DD}/2$)

This table provides the eSDHC AC timing specifications for SDR50 mode (EV_{DD}/CV_{DD} = 1.8V).

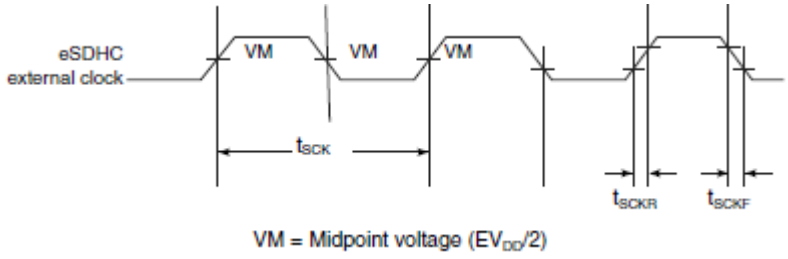
Table 93: eSDHC AC timing (SDR50)[2]

Parameter	Symbol	Min	Max	Unit	Notes
SDHC_CLK clock frequency:	f_{SCK}		90	MHz	
SDHC_CLK duty cycle		40	60	%	
SDHC_CLK clock rise and fall times	t_{SCKR}/ t_{SCKF}	-	1	ns	1
Skew between SDHC_CLK_SYNC_OUT and SDHC_CLK	–	-0.1	0.1	ns	–
Input setup times: SDHC_CMD, SDHC_DATx, SDHC_CD to SDHC_CLK_SYNC_IN	t_{NIIVKH}	1.71	-	ns	
Input hold times: SDHC_CMD, SDHC_DATx, SDHC_CD to SDHC_CLK_SYNC_IN	t_{NIIXKH}	1	-	ns	
Output hold time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid, SDHC_DATx_DIR, SDHC_CMD_DIR	t_{NIKHOX}	2.1	-	ns	
Output delay time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid, SDHC_DATx_DIR, SDHC_CMD_DIR	t_{NIKHOV}	-	7.41	ns	

Note:
1. $C_{CARD} \leq 10$ pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 30$ pF.
2. For recommended operating conditions, see Table 4.

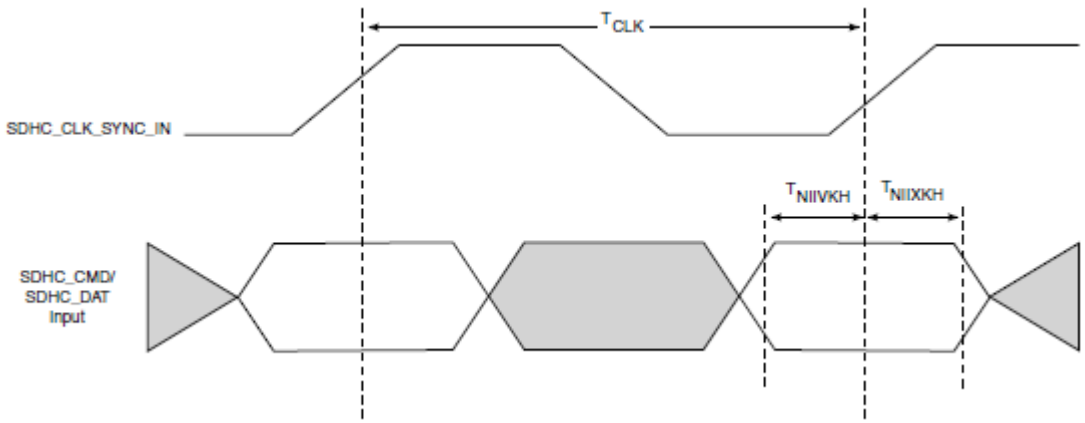
This figure provides the eSDHC clock input timing diagram for SDR50 mode.

Figure 47: eSDHC SDR50 mode clock input timing diagram



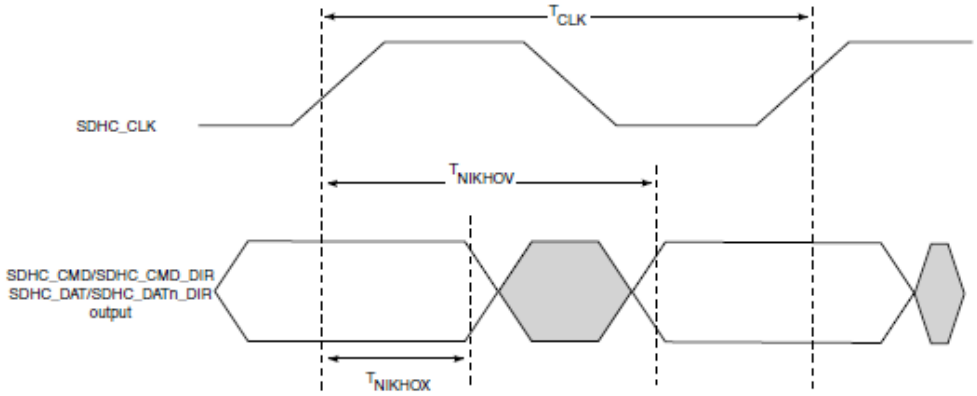
This figure shows the eSDHC input AC timing diagram for SDR50 mode.

Figure 48: eSDHC SDR50 mode input AC timing diagram



This figure shows the eSDHC output AC timing diagram for SDR50 mode.

Figure 49: eSDHC SDR50 mode output AC timing diagram



This table provides the eSDHC AC timing specifications for DDR50/eMMC DDR mode (EV_{DD}/CV_{DD} = 1.8V for DDR50, EV_{DD}/CV_{DD} = 1.8V for eMMC DDR mode).

Table 94: eSDHC AC timing (DDR50/eMMC DDR)[3]

Parameter		Symbol	Min	Max	Units	Notes
SDHC_CLK clock frequency	SD/SDIO DDR50 mode	f_{SCK}	–	42	MHz	–
	eMMC DDR mode			45		
SDHC_CLK duty cycle		–	47	53	%	–
Skew between SDHC_CLK_SYNC_OUT and SDHC_CLK		–	-0.1	0.1	ns	–
SDHC_CLK clock rise and fall times	SD/SDIO DDR50 mode	t_{SCKR}/ t_{SCKF}	–	4	ns	1
	eMMC DDR mode			2		2
Input setup times: SDHC_DATx to SDHC_CLK_SYNC_IN	SD/SDIO DDR50 mode	t_{NDIVKH}	2.5	–	ns	–
	eMMC DDR mode		1.81			
Input hold times: SDHC_DATx to SDHC_CLK_SYNC_IN	SD/SDIO DDR50 mode	t_{NDIXKH}	1.18	–	ns	–
	eMMC DDR mode		1.18			
Output hold time: SDHC_CLK to SDHC_DATx valid, SDHC_DATx_DIR	SD/SDIO DDR50 mode	t_{NDKHOX}	2.1	–	ns	–
	eMMC DDR mode		3.82			
Output delay time: SDHC_CLK to SDHC_DATx valid, SDHC_DATx_DIR	SD/SDIO DDR50 mode	t_{NDKHOV}	–	7.7	ns	–
	eMMC DDR mode			7.51		
Input setup times: SDHC_CMD, SDHC_CD to SDHC_CLK_SYNC_IN	SD/SDIO DDR50 mode	t_{NIIVKH}	7.21	–	ns	–
	eMMC DDR mode		5.77			
Input hold times: SDHC_CMD, SDHC_CD to SDHC_CLK_SYNC_IN	SD/SDIO DDR50 mode	t_{NIIXKH}	1.18	–	ns	–
	eMMC DDR mode		1.18			
Output hold time: SDHC_CLK to SDHC_CMD valid, SDHC_CMD_DIR	SD/SDIO DDR50 mode	t_{NIKHOX}	2.1	–	ns	–
	eMMC DDR mode		4.32			
Output delay time: SDHC_CLK to SDHC_CMD valid, SDHC_CMD_DIR	SD/SDIO DDR50 mode	t_{NIKHOV}	–	16.1	ns	–
	eMMC DDR mode			17.67		

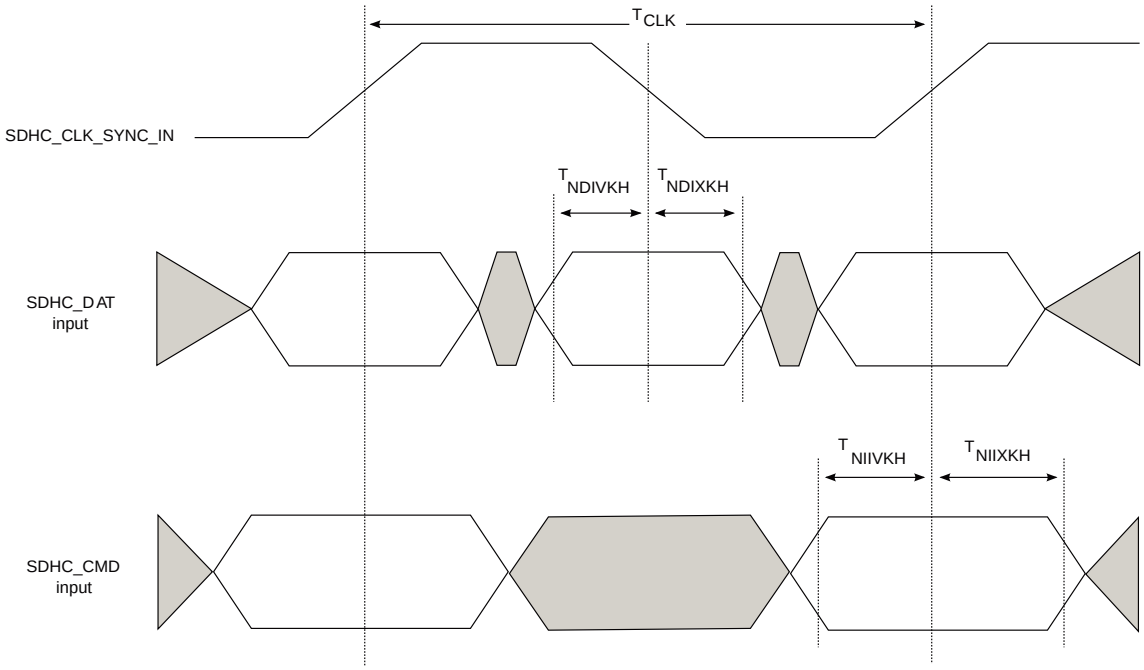
Notes:

1. $C_{CARD} \leq 10$ pF, (1 card).
2. $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 20$ pF for MMC. 40pF for SD.

3. For recommended operating conditions, see Table 4.

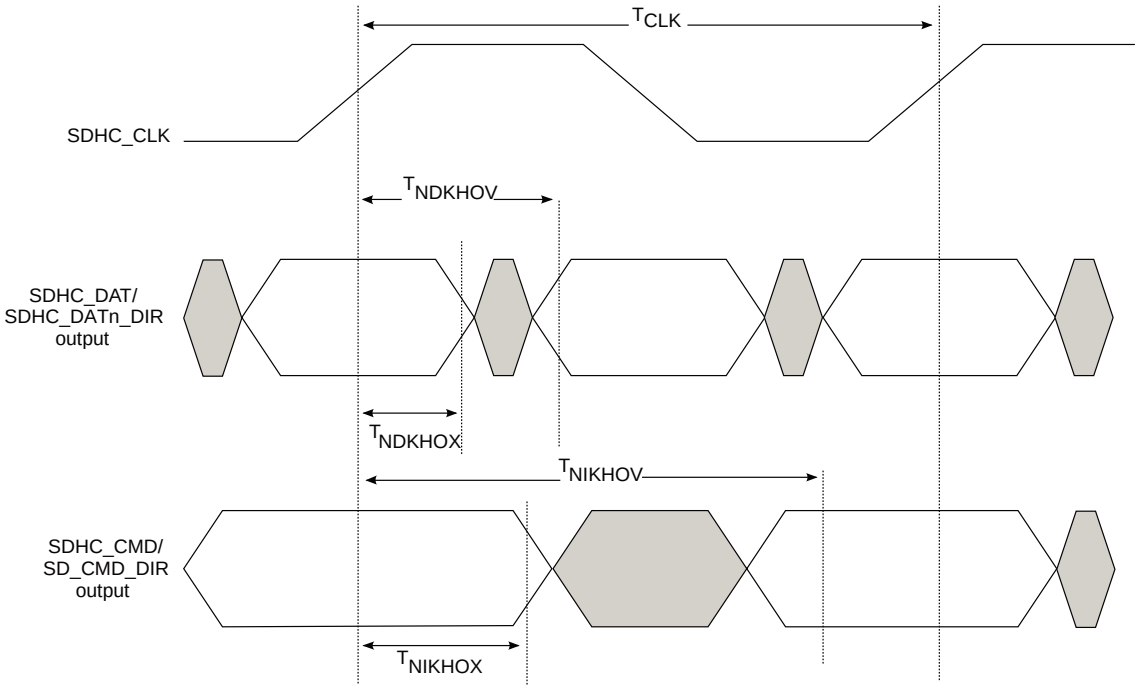
This figure shows the eSDHC DDR50/eMMC DDR mode input AC timing diagram (EV_{DD}/CV_{DD} = 1.8V).

Figure 50: eSDHC DDR50/eMMC DDR mode input AC timing diagram



This figure shows the DDR50/eMMC DDR mode output AC timing diagram.

Figure 51: eSDHC DDR50/eMMC DDR mode output AC timing diagram



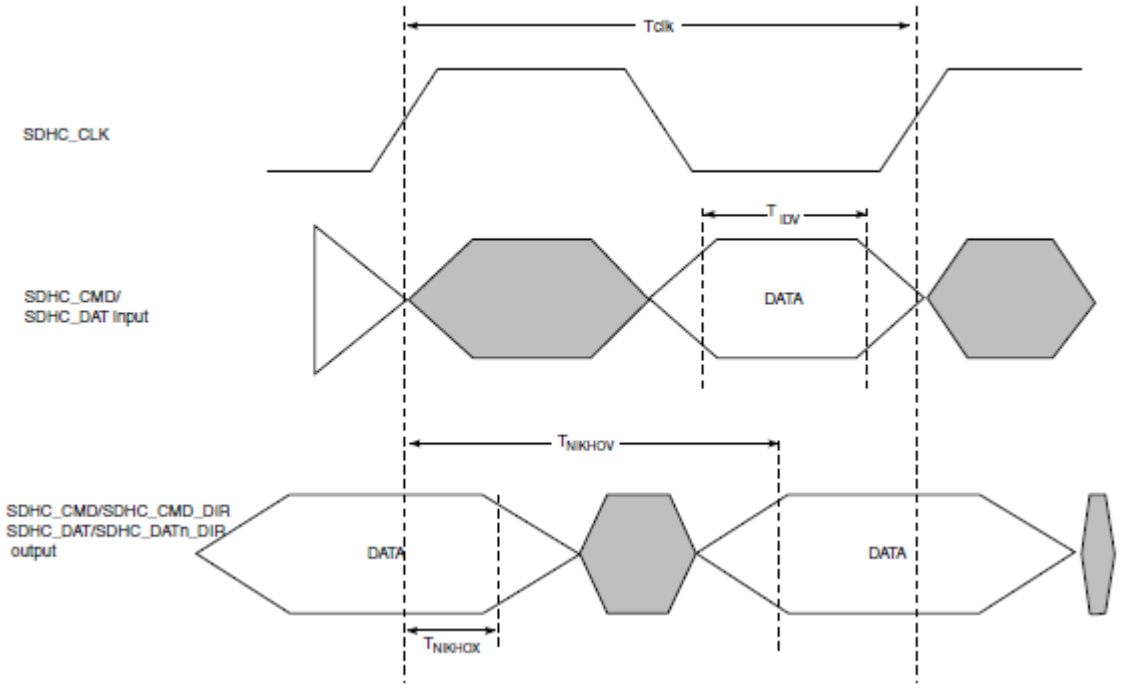
This table provides the eSDHC AC timing specifications for SDR104/eMMC HS200 mode as defined in Figure 52.

Table 95: eSDHC AC timing (SDR104/eMMC HS200)

Parameter		Symbol	Min	Max	Units	Notes
SDHC_CLK clock frequency	SD/SDIO SDR104 mode	f_{SCK}	-	140	MHz	-
	eMMC HS200 mode			140		
SDHC_CLK duty cycle		-	43	57	%	-
SDHC_CLK clock rise and fall times		t_{SCKR}/ t_{SCKF}	-	1	ns	1
Output hold time: SDHC_CLK to SDHC_CMD, SDHC DATx valid, SDHC_CMD_DIR, SDHC_DATx_DIR	SD/SDIO SDR104 mode	T_{NIKHOX}	1.6	-	ns	-
	eMMC HS200 mode		1.6			
Output delay time: SDHC_CLK to SDHC_CMD, SDHC DATx valid, SDHC_CMD_DIR, SDHC_DATx_DIR	SD/SDIO SDR104	T_{NIKHOV}	-	5.04	ns	-
	eMMC HS200 mode			5.04		
Input data window (UI)	SD/SDIO SDR104 mode	t_{IDV}	0.5	-	Unit interval	-
	eMMC HS200 mode		0.475			

Notes:
1. CL = CBUS + CHOST + CCARD ≤ 10 pF.
2. For recommended operating conditions, see Table 4.
3. This figure provides the SDR104/HS200 mode timing diagram.

Figure 52: SDR104/eMMC HS200 mode timing diagram



3.16 Multicore programmable interrupt controller (MPIC)

This section describes the DC and AC electrical specifications for the multicore programmable interrupt controller.

3.16.1 MPIC DC specifications

These tables provides the DC electrical characteristics for the MPIC interface.

Table 96: MPIC DC electrical characteristics ($O1V_{DD}$ = 1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.2	-	V	1
Input low voltage	V_{IL}	-	0.6	V	1
Input current ($O1V_{IN}$ = 0 V or $O1V_{IN}$ = $O1V_{DD}$)	I_{IN}	-	±50	µA	2
Output high voltage ($O1V_{DD}$ = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage ($O1V_{DD}$ = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

Notes:
1. The min VIL and max VIH values are based on the min and max O1VIN respective values found in Table 4.
2. The symbol $O1V_{IN}$, in this case, represents the $O1V_{IN}$ symbol referenced in Table 4.
3. For recommended operating conditions, see Table 4.

Table 97: MPIC DC electrical characteristics (DV_{DD} = 1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	-	V	1
Input low voltage	V_{IL}	-	0.2 x DV_{DD}	V	1
Input current (DV_{IN} = 0 V or DV_{IN} = DV_{DD})	I_{IN}	-	±50	µA	2
Output high voltage (DV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (DV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

Notes:
1. The min V_{IL} and max V_{IH} values are based on the min and max DVIN respective values found in Table 4.
2. The symbol DVIN, in this case, represents the DVIN symbol referenced in Table 4.
3. For recommended operating conditions, see Table 4.

Table 98: MPIC DC electrical characteristics (DV_{DD} = 2.5 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	-	V	1
Input low voltage	V_{IL}	-	0.2 x DV_{DD}	V	1
Input current (DV_{IN} = 0 V or DV_{IN} = DV_{DD})	I_{IN}	-	±50	μA	2
Output high voltage (DV_{DD} = min, I_{OH} = -1 mA)	V_{OH}	2.0	-	V	-
Output low voltage (DV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	-	0.4	V	-

Notes:
1. The min VIL and max VIH values are based on the min and max DVIN respective values found in Table 4.
2. The symbol DV_{IN}, in this case, represents the DV_{IN} symbol referenced in Table 4.
3. For recommended operating conditions, see Table 4.

Table 99: MPIC DC electrical characteristics (DV_{DD} = 3.3 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	-	V	1
Input low voltage	V_{IL}	-	0.2 x DV_{DD}	V	1
Input current (DV_{IN} = 0 V or DV_{IN} = DV_{DD})	I_{IN}	-	±40	μA	2
Output high voltage (DV_{DD} = min, I_{OH} = -2 mA)	V_{OH}	2.4	-	V	-
Output low voltage (DV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	-	0.4	V	-

Notes:
1. The min VIL and max VIH values are based on the min and max DV_{IN} respective values found in Table 4.
2. The symbol DV_{IN}, in this case, represents the DV_{IN} symbol referenced in Table 4.
3. For recommended operating conditions, see Table 4.

3.16.2 MPIC AC timing specifications

This table provides the MPIC input and output AC timing specifications.

Table 100: MPIC Input AC timing specifications[2]

Characteristic	Symbol	Min	Max	Unit	Notes
MPIC inputs-minimum pulse width	t_{PIWID}	3	-	SYSCLKs	1, 3

Notes:
1. MPIC inputs and outputs are asynchronous to any visible clock. MPIC outputs must be synchronized before use by any external synchronous logic. MPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.
2. For recommended operating conditions, see Table 4.
3. Entry and exit from deep sleep respectively require a minimum pulse width t_{PIWID} of 25 SYSCLK. See the Reference Manual for details on Entry and Exit from deep sleep.

3.17 JTAG controller

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface.

3.17.1 JTAG DC electrical characteristics

This table provides the JTAG DC electrical characteristics.

Table 101: JTAG DC electrical characteristics (OVDD = 1.8V)3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.2	-	V	1
Input low voltage	V_{IL}	-	0.6	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	-	±50	µA	2
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (OV_{DD} = min, I_{OL}= 0.5 mA)	V_{OL}	-	0.4	V	-

Notes:
1. The min VIL and max VIH values are based on the respective min and max OVIN values found in Table 4.
2. The symbol VIN, in this case, represents the OVIN symbol found in Table 4.
3. For recommended operating conditions, see Table 4.

3.17.2 JTAG AC timing specifications

This table provides the JTAG AC timing specifications as defined in Figure 53 through Figure 56.

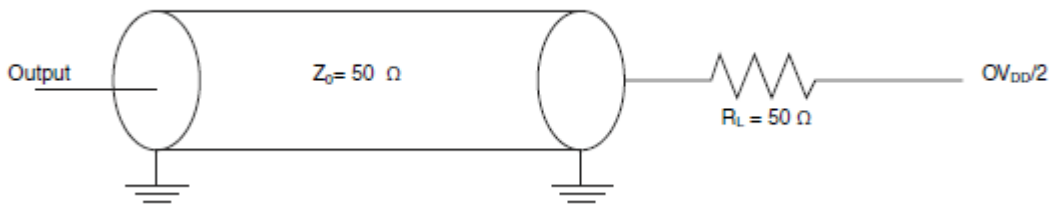
Table 102: JTAG AC timing specifications[4]

Parameter	Symbol[1]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	-
JTAG external clock cycle time	t_{JTG}	30	-	ns	-
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	-	ns	-
JTAG external clock rise and fall times	t_{JTGR}/t_{JTGF}	0	2	ns	-
TRST_B assert time	t_{TRST}	25	-	ns	2
Input setup times	t_{JTDVKH}	4	-	ns	-
Input hold times	t_{JTDXKH}	10	-	ns	-
Output valid times	t_{JTKLDV}			ns	3
Boundary-scan data		-	15		
TDO		-	10		
Output hold times	t_{JTKLDX}	0	-	ns	3

Notes:
1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, tJTDVKH symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the tJTG clock reference (K) going to the high (H) state or setup time. Also, tJTDXKH symbolizes JTAG timing (JT) with respect to the time data input signals (D) reaching the invalid state (X) relative to the tJTG clock reference (K) going to the high (H) state. Note that in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. TRST_B is an asynchronous level sensitive signal. The setup time is for test purposes only.
3. All outputs are measured from the midpoint voltage of the falling edge of tTCLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
4. For recommended operating conditions, see Table 4.

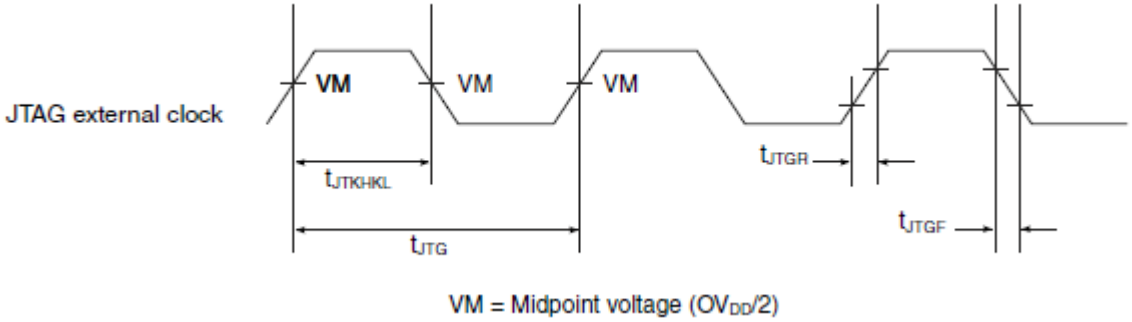
This figure provides the AC test load for TDO and the boundary-scan outputs of the device.

Figure 53: AC test load for the JTAG interface



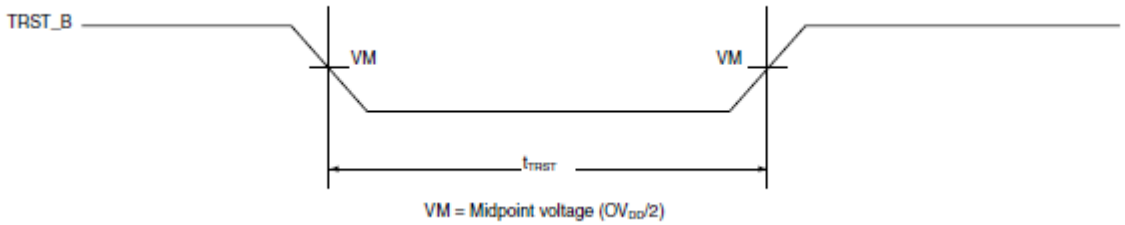
This figure provides the JTAG clock input timing diagram.

Figure 54: JTAG clock input timing diagram



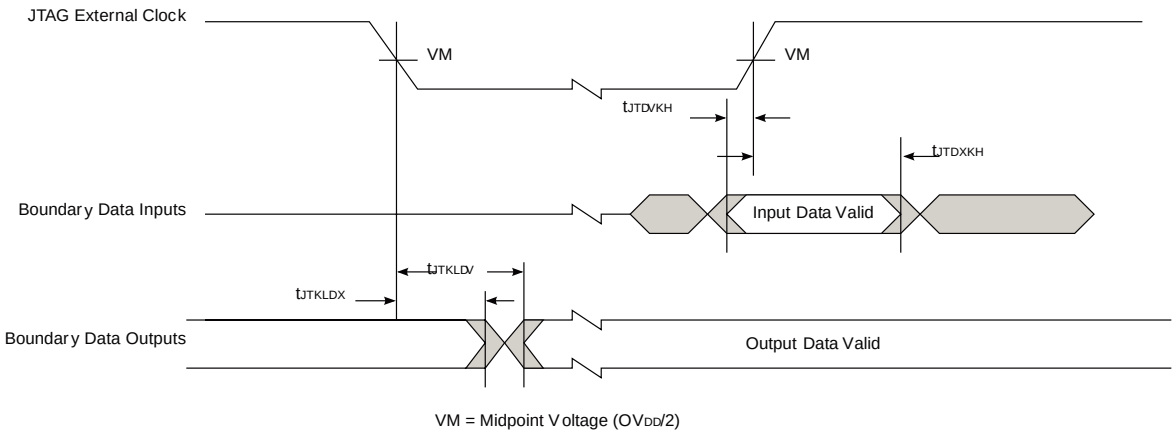
This figure provides the TRST_B timing diagram.

Figure 55: TRST_B timing diagram



This figure provides the boundary-scan timing diagram.

Figure 56: Boundary-scan timing diagram



3.18 I^2C interface

This section describes the DC and AC electrical characteristics for the I^2C interface.

3.18.1 I^2C DC electrical characteristics

This table provides the DC electrical characteristics for the I^2C interfaces operating at 3.3V.

Table 103: I^2C DC electrical characteristics (DV_{DD} = 3.3V)[5]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	VIH	0.7 x DVDD	-	V	1
Input low voltage	VIL	-	0.2 x DVDD	V	1
Output low voltage (IOL = 3.0 mA)	VOL	-	0.4	V	2
Pulse width of spikes which must be suppressed by the input filter	tI2KHKL	0	50	ns	3
Input current each I/O pin (input voltage is between 0.1 x DVDD and 0.9 x DVDD(max)	II	-50	50	µA	4
Capacitance for each I/O pin	CI	-	10	pF	-

Notes:
1. The min VIL and max VIH values are based on the respective min and max DVIN values found in Table 4.
2. The output voltage (open drain or open collector) condition = 3 mA sink current.
3. See the chip reference manual for information about the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if DV_{DD} is switched off.
5. For recommended operating conditions, see Table 4.

This table provides the DC electrical characteristics for the I^2C interfaces operating at 2.5V.

Table 104: I^2C DC electrical characteristics (DV_{DD} = 2.5V)[5]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	-	V	1
Input low voltage	V_{IL}	-	0.2 x DV_{DD}	V	1
Output low voltage (DV_{DD} = min, I_{OL} = 3 mA)	V_{OL}	0	0.4	V	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between 0.1 x DV_{DD} and 0.9 x DV_{DD}(max)	I_I	-50	50	µA	4
Capacitance for each I/O pin	C_I	-	10	pF	-

Notes:
1. The min VIL and max VIH values are based on the respective min and max DV_{IN} values found in Table 4.
2. The output voltage (open drain or open collector) condition = 3 mA sink current.
3. See the chip reference manual for information about the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if DV_{DD} is switched off.
5. For recommended operating conditions, see Table 4.

This table provides the DC electrical characteristics for the I^2C interfaces operating at 1.8V.

Table 105: I^2C DC electrical characteristics (DV_{DD} = 1.8V)[5]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	-	V	1
Input low voltage	V_{IL}	-	0.2 x DV_{DD}	V	1
Output low voltage (DV_{DD} = min, I_{OL} = 3 mA)	V_{OL}	0	0.36	V	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between 0.1 x DV_{DD} and 0.9 x DV_{DD}(max)	I_I	-50	50	µA	4
Capacitance for each I/O pin	C_I	-	10	pF	-

Notes:
1. The min VIL and max VIH values are based on the respective min and max DV_{IN} values found in Table 4.
2. The output voltage (open drain or open collector) condition = 3 mA sink current.
3. See the chip reference manual for information about the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if DV_{DD} is switched off.
5. For recommended operating conditions, see Table 4.

3.18.2 I²C AC timing specifications

This table provides the AC timing parameters for the I²C interfaces.

Table 106: I²C AC timing specifications[5]

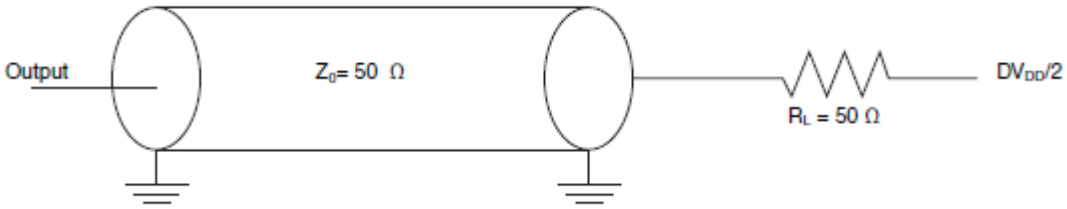
Parameter	Symbol1	Min	Max	Unit	Notes
SCL clock frequency	f_{I2C}	0	400	kHz	2
Low period of the SCL clock	t_{I2CL}	1.3	-	µs	-
High period of the SCL clock	t_{I2CH}	0.6	-	µs	-
Setup time for a repeated START condition	t_{I2SVKH}	0.6	-	µs	-
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	-	µs	-
Data setup time	t_{I2DVKH}	100	-	ns	-
Data input hold time:	t_{I2DXKL}			µs	3
CBUS compatible masters		-	-		
I²C bus devices		0	-		
Data output delay time	t_{I2OVKL}	-	0.9	µs	4
Setup time for STOP condition	t_{I2PVKH}	0.6	-	µs	-
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	-	µs	-
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	0.1 x OV_{DD}	-	V	-
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	0.2 x OV_{DD}	-	V	-
Capacitive load for each bus line	Cb	-	400	pF	-

Notes:

1. The symbols used for timing specifications herein follow the pattern t(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, tI2DVKH symbolizes I2C timing (I2) with respect to the time data input signals (D) reaching the valid state (V) relative to the tI2C clock reference (K) going to the high (H) state or setup time. Also, tI2SXKL symbolizes I2C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the tI2C clock reference (K) going to the low (L) state or hold time. Also, tI2PVKH symbolizes I2C timing (I2) for the time that the data with respect to the STOP condition (P) reaches the valid state (V) relative to the tI2C clock reference (K) going to the high (H) state or setup time.
2. The requirements for I²C frequency calculation must be followed. See *Determining the I²C Frequency Divider Ratio for SCL* (AN2919).
3. As a transmitter, the chip provides a delay time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of a START or STOP condition. When the chip acts as the I²C bus master while transmitting, it drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the chip does not generate an unintended START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for the chip as transmitter, see *Determining the I²C Frequency Divider Ratio for SCL* (AN2919).
4. The maximum t_{I2OVKL} has to be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
5. For recommended operating conditions, see Table 4.

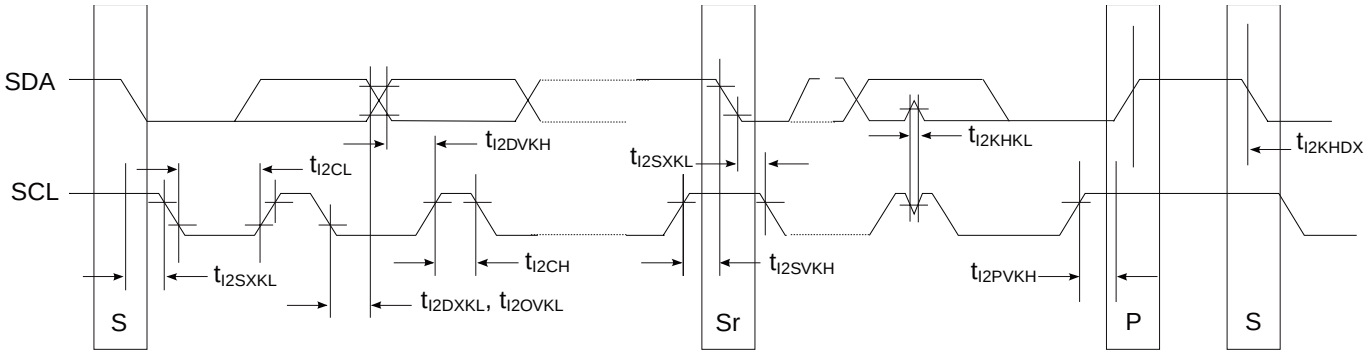
This figure provides the AC test load for the I^2C.

Figure 57: I^2C AC test load



This figure shows the AC timing diagram for the I^2C bus.

Figure 58: I^2C Bus AC timing diagram



3.19 GPIO interface

This section describes the DC and AC electrical characteristics for the GPIO interface. There are GPIO pins on various power supplies in this device. For the rest of this section, LVIN and LVDD would stand in for any power supply that the GPIO is running off.

3.19.1 GPIO DC electrical characteristics

This table provides the DC electrical characteristics for GPIO pins operating at CV_{DD} / DV_{DD} / EV_{DD} = 3.3 V.

Table 107: GPIO DC electrical characteristics (CV_{DD} / DV_{DD} / EV_{DD} = 3.3 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	-	V	1
Input low voltage	V_{IL}	-	0.2 x DV_{DD}	V	1
Input current (V_{IN} = 0 V or V_{IN}= LV_{DD})	I_{IN}	-	±50	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = -2 mA)	V_{OH}	2.4	-	V	-
Output low voltage (LV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	-	0.4	V	-

Notes:
1. The min VIL and max VIH values are based on the respective min and max LVIN values found in Table 4.
2. The symbol VIN, in this case, represents the LVIN symbol referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 4

This table provides the DC electrical characteristics for GPIO pins operating at CV_{DD} / DV_{DD} / EV_{DD} = 2.5 V.

Table 108: GPIO DC electrical characteristics (CVDD / DVDD / EVDD = 2.5 V)3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	-	V	1
Input low voltage	V_{IL}	-	0.2 x DV_{DD}	V	1
Input current (V_{IN} = 0 V or V_{IN}= LV_{DD})	I_{IN}	-	±50	µA	2
Output high voltage (LV_{DD} = min, I_{OH} = -1 mA)	V_{OH}	2.0	-	V	-
Output low voltage (LV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	-	0.4	V	-

Notes:
1. The min VIL and max VIH values are based on the respective min and max LV_{IN} values found in Table 4.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Recommended operating.
3. For recommended operating conditions, see Table 4.

This table provides the DC electrical characteristics for GPIO pins operating at CV_{DD} / DV_{DD} / EV_{DD} = 1.8V.

Table 109: GPIO DC electrical characteristics (CV_{DD} / DV_{DD} / EV_{DD} = 1.8 V)3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	-	V	1
Input low voltage	V_{IL}	-	0.2 x DV_{DD}	V	1
Input current (VIN = 0 V or VIN = LVDD)	I_{IN}	-	±50	µA	2
Output high voltage (LVDD = min, IOH = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (LVDD = min, IOL = 0.5 mA)	V_{OL}	-	0.4	V	-

Notes:
1. The min VIL and max VIH values are based on the respective min and max LV_{IN} values found in Table 4.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 4.

This table provides the DC electrical characteristics for GPIO pins operating at OV_{DD}/ $O1V_{DD}$ = 1.8V.

Table 110: GPIO DC electrical characteristics (OVDD/ O1VDD= 1.8V)3

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.2	-	V	1
Input low voltage	V_{IL}	-	0.6	V	1
Input current (VIN = 0 V or VIN = LVDD)	I_{IN}	-	±50	µA	2
Output high voltage (LVDD = min, IOH = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (LVDD = min, IOL = 0.5 mA)	V_{OL}	-	0.4	V	-

Notes:
1. The min VIL and max VIH values are based on the respective min and max LV_{IN} values found in Table 4.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 4.

3.19.2 GPIO AC timing specifications

This table provides the GPIO input and output AC timing specifications.

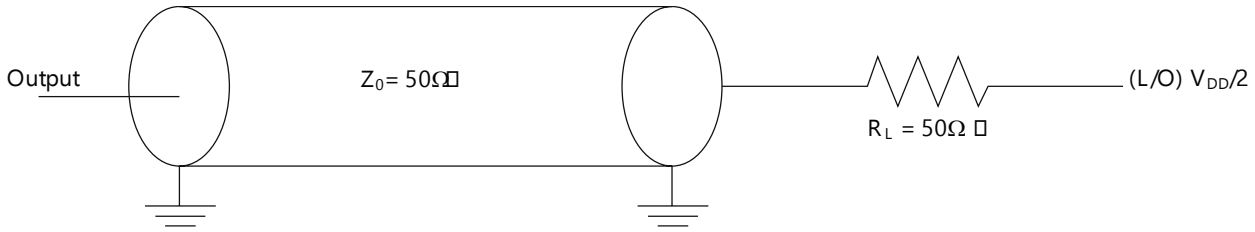
Table 111: GPIO input AC timing specifications2

Parameter	Symbol	Min	Unit	Notes
GPIO inputs–minimum pulse width	t_{PIWID}	20	ns	1, 3

Notes:
1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} to ensure proper operation.
2. For recommended operating conditions, see Table 4.
3. Entry and exit from deep sleep respectively require a minimum pulse width t_{PIWID} of 35 SYSCLK. See the Reference Manual for details on Entry and Exit from deep sleep.

This figure provides the AC test load for the GPIO

Figure 59: GPIO AC test load



3.20 Display interface unit

This section describes the DIU DC and AC electrical characteristics.

3.20.1 DIU DC electrical characteristics

This table provides the DIU DC electrical characteristics.

Table 112: DIU DC electrical characteristics (3.3V)1

Parameter	Symbol	Min	Max	Unit	Notes
Output high voltage (DVDD = min, IOH = -2 mA)	V_{OH}	2.4	-	V	-
Output low voltage (DVDD = min, IOL = 2 mA)	V_{OL}	-	0.4	V	-

Note:
1. For recommended operating conditions, see Table 4.

3.20.2 DIU AC timing specifications (Preliminary)

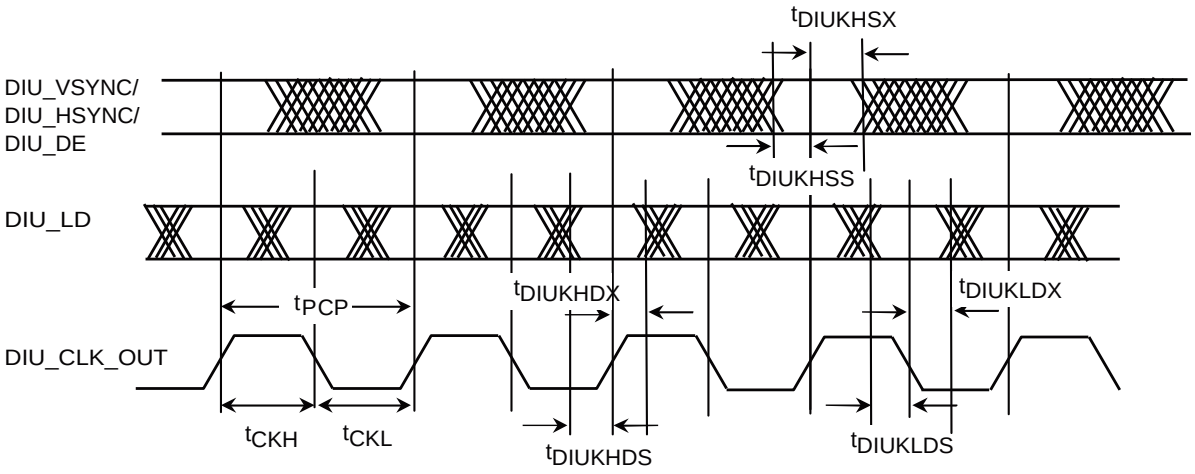
The table provides the output AC timing specifications for DIU interface.

Table 113: DIU interface timing parameters

Parameter	Symbol	Min	Typ	Max	Unit
Display pixel clock period	t_{pcp}	10	-	-	ns
Display pixel clock high time	t_{CKH}	0.45 x t_{PCP}	0.5 x t_{PCP}	0.55 x t_{PCP}	ns
LCD interface pixel clock low time	t_{CKL}	0.45 x t_{PCP}	0.5 x t_{PCP}	0.55 x t_{PCP}	ns
Pixel data output setup with respect to pixel clock	$t_{DIUKHDS}$ $t_{DIUKLDS}$	1.2	-	-	ns
Pixel data output hold with respect to pixel clock	$t_{DIUKHDX}$ $t_{DIUKLDX}$	1.2	-	-	ns
VSYNC/ HSYNC/ DE output setup respect to pixel clock	$t_{DIUKHSS}$	1.2	-	-	ns
VSYNC/ HSYNC/ DE output hold respect to pixel clock	$t_{DIUKHSX}$	3.8	-	-	ns

Note:
1. Display pixel clock frequency must be less than or equal to 1/4 of the platform clock.

Figure 60: DIU interface AC timing diagram



3.21 High-speed serial interfaces (HSSI)

The chip features a serializer/deserializer (SerDes) interface to be used for high-speed serial interconnect applications. The SerDes interface can be used for PCI Express, SATA, SGMII and QSGMII data transfers.

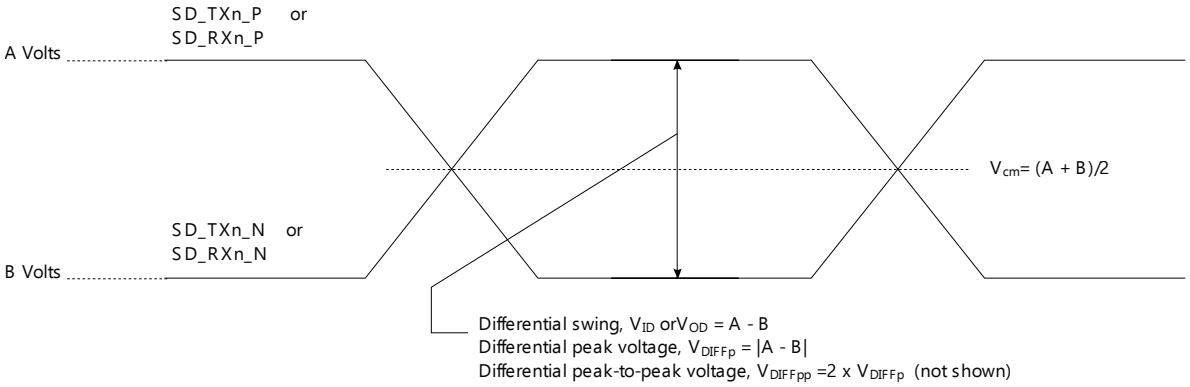
This section describes the common portion of SerDes DC electrical specifications: the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter (Tx) and receiver (Rx) reference circuits are also shown.

3.21.1 Signal terms definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines the terms that are used in the description and specification of differential signals.

This figure shows how the signals are defined. For illustration purposes only, one SerDes lane is used in the description. This figure shows the waveform for either a transmitter output (SD_TX*n*_P and SD_TX*n*_N) or a receiver input (SD_RX*n*_P and SD_RX*n*_N). Each signal swings between A volts and B volts where A > B.

Figure 61: Differential voltage definitions for transmitter or receiver



Using this waveform, the definitions are as shown in the following list. To simplify the illustration, the definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment:

Single-Ended Swing

The transmitter output signals and the receiver input signals SD_TX*n*_P, SD_TX*n*_N, SD_RX*n*_P and SD_RX*n*_N each have a peak-to-peak swing of A - B volts. This is also referred as each signal wire's single-ended swing.

Differential Output Voltage, V_{OD} (or Differential Output Swing)

The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complementary output voltages: $V_{SD\_TXn\_P}$ - $V_{SD\_TXn\_N}$. The V_{OD} value can be either positive or negative.

Differential Peak Voltage, V_{DIFFp}

The peak value of the differential transmitter output signal or the differential receiver input signal is defined as the differential peak voltage, V_{DIFFp} = |A - B| volts.

Differential Peak-to-Peak, $V_{DIFFp-p}$

Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A - B to -(A - B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p}$ = 2 x V_{DIFFp} = 2 x |(A - B)| volts, which is twice the differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-to-peak voltage can also be calculated as V_{TX-} DIFFp-p = 2 x |V_{OD}|.

Differential Waveform

The differential waveform is constructed by subtracting the inverting signal (SD_TX*n*_N, for example) from the non-inverting signal (SD_TX*n*_P, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. See Figure 66 as an example for differential waveform.

Common Mode Voltage, V_{cm}

The common mode voltage is equal to half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm\_out} = (V_{SD\_TXn+} V_{SD\_TXn\_B}) \div 2 = (A + B) \div 2$, which is the arithmetic mean of the two complementary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. It may be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset on some occasions.

To illustrate these definitions using real values, consider the example of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and outputs, TD and TD_B. If these outputs have a swing from 2.0 V to 2.5 V, the peak-to-peak voltage swing of each signal (TD or TD_B) is 500 mV p-p, which is referred to as the single-ended swing for each signal. Because the differential signaling environment is fully symmetrical in this example, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and -500 mV. In other words, V_{OD} is 500 mV in one phase and -500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

3.21.2 SerDes reference clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD1_REF_CLK[1:2]_P and SD1_REF_CLK[1:2]_N.

Electrical characteristics

SerDes may be used for various combinations of the following IP blocks based on the RCW Configuration field SRDS_PRTCLn:

- SGMII (1.25 or 3.125 Gbaud), QSGMII (5 Gbps only)
- XFI (10 Gbps)
- PEX1/2/3 (2.5 and 5 Gbps)
- Aurora (2.5 and 5 Gbps)
- SATA (1.5 and 3.0 Gbps)

The following sections describe the SerDes reference clock requirements and provide application information.

3.21.2.1 SerDes spread-spectrum clock source recommendations

SDn_REF_CLKn_P/SDn_REF_CLKn_N are designed to work with spread-spectrum clock for PCI Express protocol only with the spreading specification defined in Table 114. When using spread-spectrum clocking for PCI Express, both ends of the link partners should use the same reference clock. For best results, a source without significant unintended modulation must be used.

For SATA protocol, the SerDes transmitter does not support spread-spectrum clocking. The SerDes receiver does support spread-spectrum clocking on receive, which means the SerDes receiver can receive data correctly from a SATA serial link partner using spread- spectrum clocking.

The spread-spectrum clocking cannot be used if the same SerDes reference clock is shared with other non-spread-spectrum supported protocols. For example, if the spread- spectrum clocking is desired on a SerDes reference clock for PCI Express and the same reference clock is used for any other protocol such as SATA/SGMII/QSGMII due to the SerDes lane usage mapping option, spread-spectrum clocking cannot be used at all.

Table 114: SerDes spread-spectrum clock source recommendations[1]

Parameter	Min	Max	Unit	Notes
Frequency modulation	30	33	kHz	-
Frequency spread	+0	-0.5	%	2

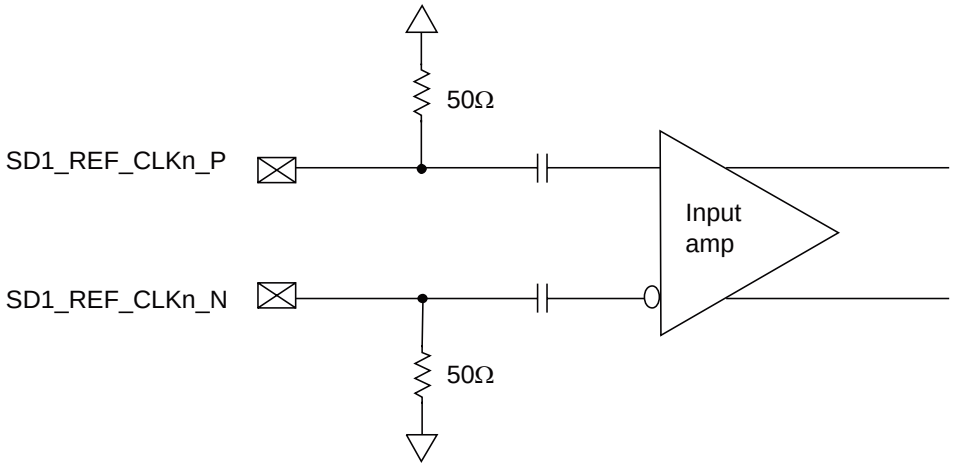
Notes:

1. At recommended operating conditions. See Table 4.
2. Only down-spreading is allowed.

3.21.2.2 SerDes reference clock receiver characteristics

This figure shows a receiver reference diagram of the SerDes reference clocks.

Figure 62: Receiver of SerDes reference clocks



The characteristics of the clock signals are as follows:

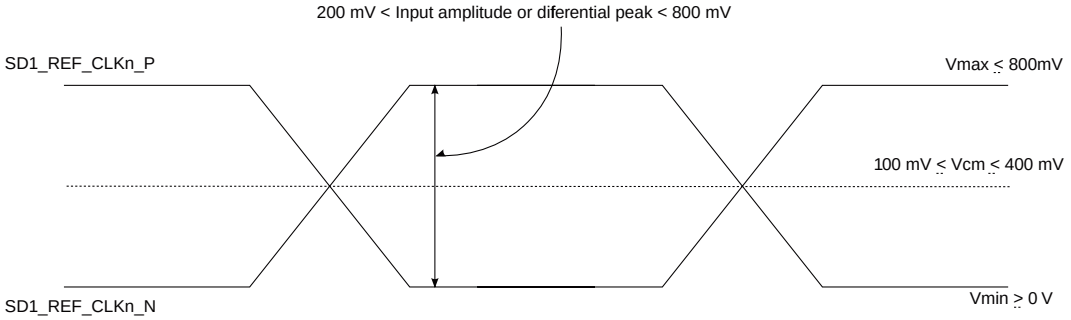
- The SerDes transceivers core power supply voltage requirements ($S1V_{DD}$) are as specified in Recommended operating conditions.
- The SerDes reference clock receiver reference circuit structure is as follows:
- The SD1_REF_CLKn_P and SD1_REF_CLKn_N are internally AC-coupled differential inputs as shown in Figure 62. Each differential clock input (SD1_REF_CLKn_P or SD1_REF_CLKn_N) has on-chip 50-Ω termination to SGNDn followed by on-chip AC-coupling.
- The external reference clock driver must be able to drive this termination.
- The SerDes reference clock input can be either differential or single-ended. See the differential mode and single-ended mode descriptions below for detailed requirements.
- The maximum average current requirement also determines the common mode voltage range.
- When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA because the input is AC-coupled on-chip.
- This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V ÷ 50 = 8 mA) while the minimum common mode input level is
- 0.1 V above SGND*n*. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0-0.8 V), such that each phase of the differential input has a single- ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
- If the device driving the SD1_REF_CLK*n*_P and SD1_REF_CLK*n*_N inputs cannot drive 50 Ω to SGND*n* DC or the drive strength of the clock driver chip exceeds the maximum input current limitations, it must be AC-coupled off-chip.
- The input amplitude requirement is described in detail in the following sections.

3.21.2.3 DC-level requirement for SerDes reference clocks

The DC level requirement for the SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs, as described below:

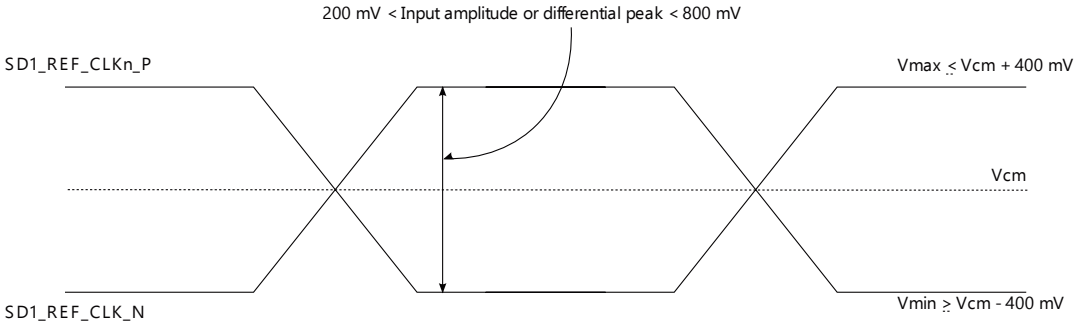
- Differential Mode
- The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-to-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing of less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
- For an external DC-coupled connection, as described in SerDes reference clock receiver characteristics, the maximum average current requirements sets the requirement for average voltage (common mode voltage) as between 100 mV and 400 mV. Figure 63 shows the SerDes reference clock input requirement for DC-coupled connection scheme.

Figure 63: Differential reference clock input DC requirements (external DC-coupled)



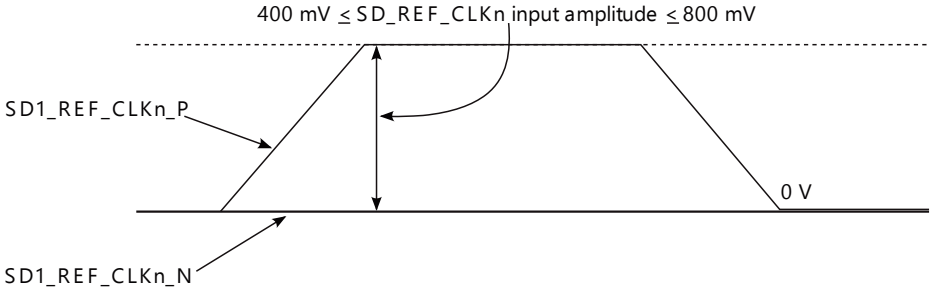
- For an external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Because the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different common mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND*n*. Each signal wire of the differential inputs is allowed to swing below and above the common mode voltage (SGND*n*). Figure 64 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

Figure 64: Differential reference clock input DC requirements (external AC-coupled)



- Single-Ended Mode
- The reference clock can also be single-ended. The SD1_REF_CLK*n*_P input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-to- peak (from V_{MIN} to V_{MAX}) with SD1_REF_CLK*n*_N either left unconnected or tied to ground.
- The SD1_REF_CLK*n* input average voltage must be between 200 and 400 mV. Figure 65 shows the SerDes reference clock input requirement for single-ended signaling mode.
- To meet the input amplitude requirement, the reference clock inputs may need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase (SD1_REF_CLK*n*_N) through the same source impedance as the clock input (SD1_REF_CLK*n*) in use.

Figure 65: Single-ended reference clock input DC requirements



3.21.2.4 AC requirements for SerDes reference clocks

This table lists the AC requirements for SerDes reference clocks for protocols running at data rates up to 5 Gb/s.

This includes PCI Express (2.5, 5 GT/s), SGMII (1.25Gbps), QSGMII (5Gbps). SerDes reference clocks to be guaranteed by the customer's application design.

Table 115: SD1_REF_CLK*n*_P and SD1_REF_CLK*n*_N input clock requirements ($S1V_{DD}n$ = 1.0 V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SD1_REF_CLKn_P/SD1_REF_CLKn_N frequency range	t_{CLK_REF}	-	100/125	-	MHz	2
SD1_REF_CLKn_P/SD1_REF_CLKn_N clock frequency tolerance	t_{CLK_TOL}	-300	-	300	ppm	3
SD1_REF_CLKn_P/SD1_REF_CLKn_N clock frequency tolerance	t_{CLK_TOL}	-100	-	100	ppm	4
SD1_REF_CLKn_P/SD1_REF_CLKn_N reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	5
SD1_REF_CLKn_P/SD1_REF_CLKn_N max deterministic peak-to-peak jitter at 10^{-6} BER	t_{CLK_DJ}	-	-	42	ps	-
SD1_REF_CLKn_P/SD1_REF_CLKn_N total reference clock jitter at 10^{-6} BER (peak-to-peak jitter at refClk input)	t_{CLK_TJ}	-	-	86	ps	6
SD1_REF_CLKn_P/SD1_REF_CLKn_N 10 kHz to 1.5 MHz RMS jitter	$t_{REFCLK\text{-}LF\text{-}RMS}$	-	-	3	ps RMS	7
SD1_REF_CLKn_P/SD1_REF_CLKn_N > 1.5 MHz to Nyquist RMS jitter	$t_{REFCLK\text{-}HF\text{-}RMS}$	-	-	3.1	ps RMS	7
SD1_REF_CLKn_P/SD1_REF_CLKn_N rising/falling edge rate	t_{CLKRR}/t_{CLKFR}	0.6	-	4	V/ns	8
Differential input high voltage	V_{IH}	150	-	-	mV	5
Differential input low voltage	V_{IL}	-	-	-150	mV	5
Rising edge rate (SD1REF_CLKn_P) to falling edge rate (SD1_REF_CLKn_N) matching	Rise-Fall Matching	-	-	20	%	10, 10

Notes:

1. For recommended operating conditions, see Table 4.
2. Caution: Only 100 and 125 have been tested. In-between values do not work correctly with the rest of the system.
3. For PCI Express(2.5, 5 GT/s)
4. For SGMII, QSGMII
5. Measurement taken from differential waveform
6. Limits from PCI Express CEM Rev 2.0
7. For PCI Express-5 GT/s, per PCI Express base specification rev 3.0
8. Measured from -150 mV to +150 mV on the differential waveform (derived from SD1_REF_CLKn_P minus SD1_REF_CLKn_N). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing. See Figure 66.
9. Measurement taken from single-ended waveform.

10. Matching applies to rising edge for SD1_REF_CLKn_P and falling edge rate for SD1_REF_CLKn_N. It is measured using a 200 mV window centered on the median cross point where SD1_REF_CLKn_P rising meets SD1_REF_CLKn_N falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SD1_REF_CLKn_P must be compared to the fall edge rate of SD1_REF_CLKn_N, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 67.

This table lists the AC requirements for SerDes reference clocks for protocols running at data rates greater than 8 GBaud.

This includes XFI (10.3125 GBaud) and 10GBase-KR (10.3125 GBaud), SerDes reference clocks to be guaranteed by the customer's application design.

Table 116: SD1_REF_CLKn_P/ SD1_REF_CLKn_N input clock requirements ($SV_{DD}n$ = 1.0 V)[1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SD1_REF_CLKn_P/ SD1_REF_CLKn_N frequency range	t_{CLK_REF}	-	156.25	-	MHz	2
SD1_REF_CLKn_P/ SD1_REF_CLKn_N clock frequency tolerance	t_{CLK_TOL}	-100	-	100	ppm	-
SD1_REF_CLKn_P/ SD1_REF_CLKn_N reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	3
SD1_REF_CLKn_P/ SD1_REF_CLKn_N single side band noise	@1 kHz	-	-	-85	dBC/Hz	4
SD1_REF_CLKn_P/ SD1_REF_CLKn_N single side band noise	@10 kHz	-	-	-108	dBC/Hz	4
SD1_REF_CLKn_P/ SD1_REF_CLKn_N single side band noise	@100 kHz	-	-	-128	dBC/Hz	4
SD1_REF_CLKn_P/ SD1_REF_CLKn_N single side band noise	@1 MHz	-	-	-138	dBC/Hz	4
SD1_REF_CLKn_P/ SD1_REF_CLKn_N single side band noise	@10MHz	-	-	-138	dBC/Hz	4
SD1_REF_CLKn_P/ SD1_REF_CLKn_N random jitter (1.2 MHz to 15 MHz)	t_{CLK_RJ}	-	-	0.8	ps	-
SD1_REF_CLKn_P/ SD1_REF_CLKn_N total reference clock jitter at 10^{-12} BER (1.2 MHz to 15 MHz)	t_{CLK_TJ}	-	-	11	ps	-
SD1_REF_CLKn_P/ SD1_REF_CLKn_N spurious noise (1.2 MHz to 15 MHz)	-	-	-	-75	dBC	-

Notes:

1. For recommended operating conditions, see Table 4.
2. **Caution:** Only 156.25 have been tested. In-between values do not work correctly with the rest of the system.
3. Measurement taken from differential waveform.
4. Per XFP Spec. Rev 4.5, the Module Jitter Generation spec at XFI Optical Output is 10mUI (RMS) and 100 mUI (p-p). In the CDR mode the host is contributing 7 mUI (RMS) and 50 mUI (p-p) jitter.

Figure 66: Differential measurement points for rise and fall time

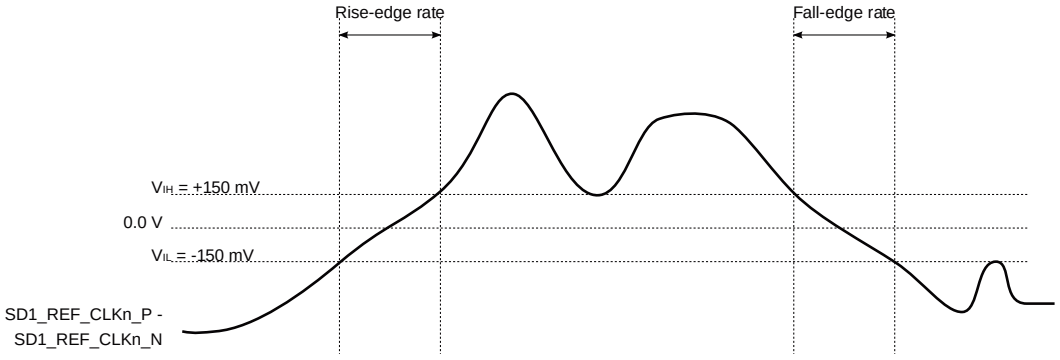
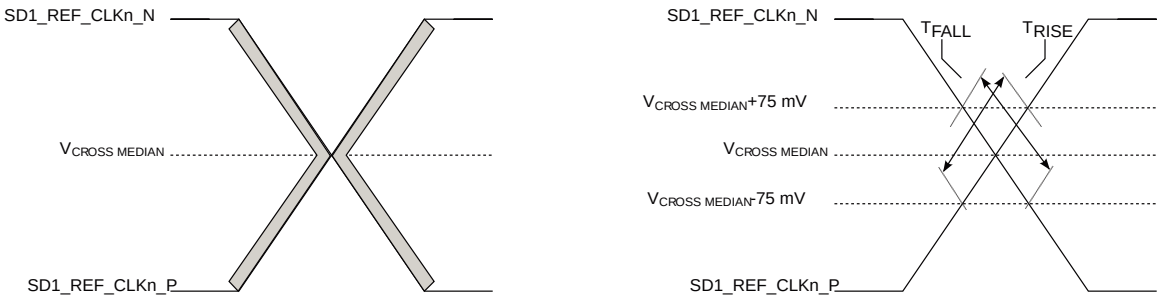


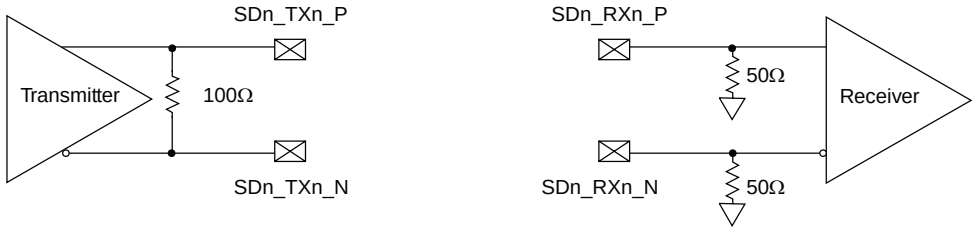
Figure 67: Single-ended measurement points for rise and fall time matching



3.21.3 SerDes transmitter and receiver reference circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.

Figure 68: SerDes transmitter and receiver reference circuits



The DC and AC specification of SerDes data lanes are defined in each interface protocol section below based on the application usage:

- PCI Express
- Aurora interface
- Serial ATA (SATA) interface
- SGMII interface
- QSGMII interface

Note that external AC-coupling capacitor is required for the above serial transmission protocols with the capacitor value defined in the specification of each protocol section.

3.21.4 PCI Express

This section describes the clocking dependencies, DC and AC electrical specifications for the PCI Express bus.

3.21.4.1 Clocking dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

The platform clock frequency must be 400 MHz for PCI Express Gen 2. For more details, refer to Minimum platform frequency requirements for high-speed interfaces.

3.21.4.2 PCI Express DC physical layer specifications

This section contains the DC specifications for the physical layer of PCI Express on this chip.

3.21.4.2.1 PCI Express DC physical layer transmitter specifications

This section discusses the PCI Express DC physical layer transmitter specifications for 2.5 GT/s and 5 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 117: PCI Express 2.0 (2.5 GT/s) differential transmitter output DC specifications ($X1V_{DD}$ = 1.35 V)[1]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential peak-to-peak output voltage	$V_{TX-DIFFp-p}$	800	1000	1200	mV	$V_{TX-DIFFp-p} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.
DC differential transmitter impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	Transmitter DC differential mode low Impedance
Transmitter DC impedance	Z_{TX-DC}	40	50	60	Ω	Required transmitter D+ as well as D- DC Impedance during all states

Note:
1. For recommended operating conditions, see Table 4.

This table defines the PCI Express 2.0 (5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 118: PCI Express 2.0 (5 GT/s) differential transmitter output DC specifications ($X1V_{DD}$ = 1.35 V)[1]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential peak-to-peak output voltage	$V_{TX-DIFFp-p}$	800	1000	1200	mV	$V_{TX-DIFFp-p} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$
Low power differential peak-to-peak output voltage	$V_{TX-DIFFp-p\_low}$	400	500	1200	mV	$V_{TX-DIFFp-p} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-3.5dB}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.
DC differential transmitter impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	Transmitter DC differential mode low impedance
Transmitter DC Impedance	Z_{TX-DC}	40	50	60	Ω	Required transmitter D+ as well as D- DC impedance during all states

Notes:
1. For recommended operating conditions, see Table 4.

3.21.4.3 PCI Express DC physical layer receiver specifications

This section discusses the PCI Express DC physical layer receiver specifications for 2.5 GT/s and 5 GT/s.

This table defines the DC specifications for the PCI Express 2.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 119: PCI Express 2.0 (2.5 GT/s) differential receiver input DC specifications (SV_{DD} = 1.0 V)[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Differential input peak-to-peak voltage	$V_{RX-DIFFp-p}$	120	1000	1200	mV	$V_{RX-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ See Note 1.
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	Receiver DC differential mode impedance. See Note 2
DC input impedance	Z_{RX-DC}	40	50	60	Ω	Required receiver D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	-	-	kΩ	Required receiver D+ as well as D- DC Impedance when the receiver terminations do not have power. See Note 3.
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	-	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ Measured at the package pins of the receiver

Notes:

1. Measured at the package pins with a test load of 50Ω to GND on each pin.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
3. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the receiver ground.
4. For recommended operating conditions, see Table 4.
5. This table defines the DC specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 120: PCI Express 2.0 (5 GT/s) differential receiver input DC specifications (SVDD = 1.0 V)4

Parameter	Symbol	Min	Typ	Max	Units	Notes
Differential input peak-to-peak voltage	$V_{RX-DIFFp-p}$	120	1000	1200	mV	$V_{RX-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ See Note 1.
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	Receiver DC differential mode impedance. See Note 2
DC input impedance	Z_{RX-DC}	40	50	60	Ω	Required receiver D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	-	-	kΩ	Required receiver D+ as well as D- DC Impedance when the receiver terminations do not have power. See Note 3.
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	-	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$
						Measured at the package pins of the receiver

Notes:

1. Measured at the package pins with a test load of 50 Ω to GND on each pin.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
3. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the receiver ground.
4. For recommended operating conditions, see Table 4.

3.21.4.4 PCI Express AC physical layer specifications

This section contains the AC specifications for the physical layer of PCI Express on this device.

3.21.4.4.1 PCI Express AC physical layer transmitter specifications

This section discusses the PCI Express AC physical layer transmitter specifications for 2.5 GT/s and 5 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 121: PCI Express 2.0 (2.5 GT/s) differential transmitter output AC specifications[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit interval	UI	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Minimum transmitter eye width	T_{TX-EYE}	0.75	-	-	UI	The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.25$ UI. Does not include spread-spectrum or RefCLK jitter. Includes device random jitter at 10^{-12}. See Notes 1 and 2.
Maximum time between the jitter median and maximum deviation from the median	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	-	-	0.125	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p} = 0$ V) in relation to a recovered transmitter UI. A recovered transmitter UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the transmitter UI. See Notes 1 and 2.
AC coupling capacitor	C_{TX}	75	-	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 3.

Notes:

1. Specified at the measurement point into a timing and voltage test load as shown in Figure 70 and measured over any 250 consecutive transmitter UIs.
2. A $T_{TX-EYE} = 0.75$ UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX} = 0.25$ UI for the transmitter collected over any 250 consecutive transmitter UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total transmitter jitter budget collected over any 250 consecutive transmitter UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
3. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.
4. For recommended operating conditions, see Table 4.

This table defines the PCI Express 2.0 (5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 122: PCI Express 2.0 (5 GT/s) differential transmitter output AC specifications[3]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	199.94	200.00	200.06	ps	Each UI is 200 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Minimum transmitter eye width	T_{TX-EYE}	0.75	-	-	UI	The maximum transmitter jitter can be derived as: $T_{TX-MAX-JITTER}$ = 1 - T_{TX-EYE} = 0.25 UI. See Note 1.
Transmitter RMS deterministic jitter > 1.5 MHz	$T_{TX-HF-DJ-DD}$	-	-	0.15	ps	-
Transmitter RMS deterministic jitter < 1.5 MHz	$T_{TX-LF-RMS}$	-	3.0	-	ps	Reference input clock RMS jitter (< 1.5 MHz) at pin < 1 ps
AC coupling capacitor	C_{TX}	75	-	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 2.

Notes:
1. Specified at the measurement point into a timing and voltage test load as shown in Figure 70 and measured over any 250 consecutive transmitter UIs.
2. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.
3. For recommended operating conditions, see Table 4.

3.21.4.4.2 PCI Express AC physical layer receiver specifications

This section discusses the PCI Express AC physical layer receiver specifications for 2.5 GT/s and 5 GT/s.

This table defines the AC specifications for the PCI Express 2.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 123: PCI Express 2.0 (2.5 GT/s) differential receiver input AC specifications[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	399.88	400.00	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Minimum receiver eye width	T_{RX-EYE}	0.4	-	-	UI	The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as TRX-MAX- JITTER = 1 - TRX-EYE= 0.6 UI. See Notes 1 and 2.
Maximum time between the jitter median and maximum deviation from the median.	$T_{RX-EYE-MEDIAN- to-MAX-JITTER}$	-	-	0.3	UI	Jitter is defined as the measurement variation of the crossing points (VRX-DIFFp-p= 0 V) in relation to a recovered transmitter UI. A recovered transmitter UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the transmitter UI. See Notes 1, 2 and 3.

Notes:
1. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 70 must be used as the receiver device when taking measurements. If the clocks to the receiver and transmitter are not derived from the same reference clock, the transmitter UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.

2. A TRX-EYE = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The TRX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive transmitter UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the receiver and transmitter are not derived from the same reference clock, the transmitter UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
3. It is recommended that the recovered transmitter UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.
4. For recommended operating conditions, see Table 4.

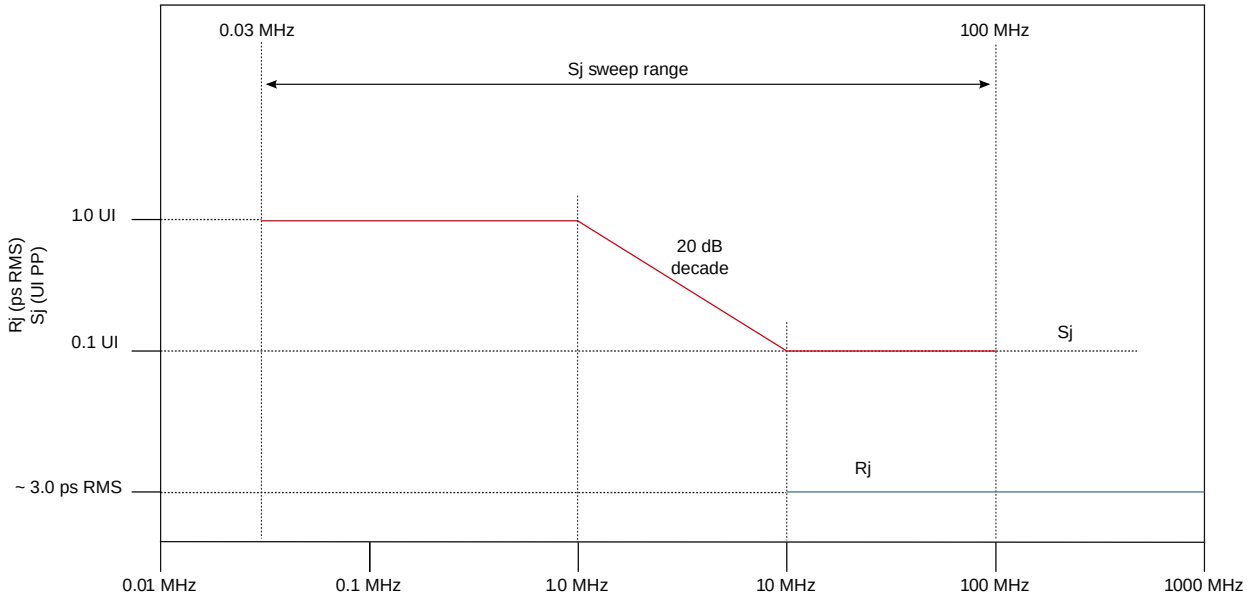
   This table defines the AC specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 124: PCI Express 2.0 (5 GT/s) differential receiver input AC specifications[1]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	199.94	200.00	200.06	ps	Each UI is 200 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Max receiver inherent timing error	$T_{RX-TJ-CC}$	-	-	0.4	UI	The maximum inherent total timing error for common RefClk receiver architecture
Max receiver inherent deterministic timing error	$T_{RX-DJ-DD-CC}$	-	-	0.30	UI	The maximum inherent deterministic timing error for common RefClk receiver architecture

Note:
1. For recommended operating conditions, see Table 4.

Figure 69: Swept sinusoidal jitter mask

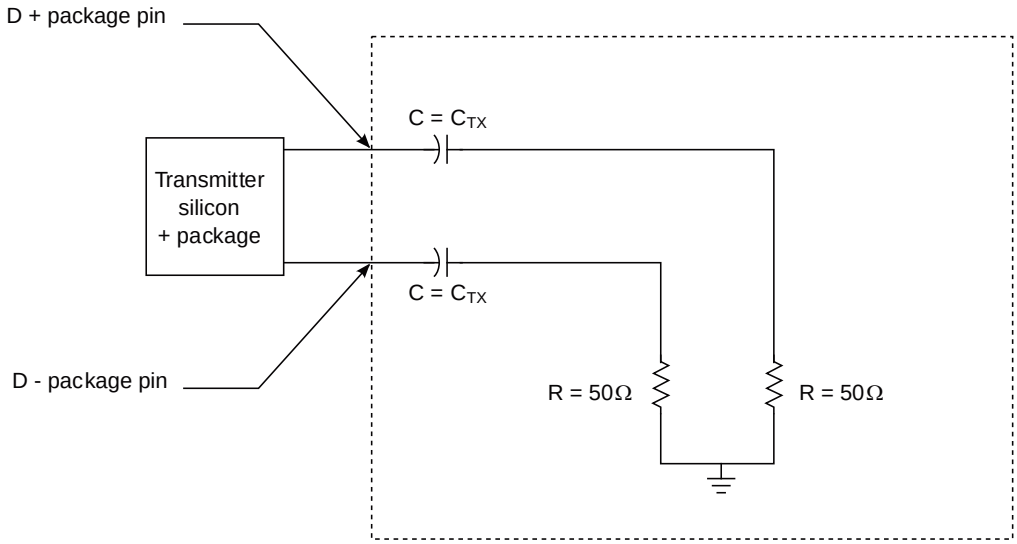


3.21.4.5 Test and measurement load

The AC timing and voltage parameters must be verified at the measurement point. The package pins of the device must be connected to the test/measurement load within 0.2 inches of that load, as shown in the following figure.

NOTE
The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/ board routing may benefit from D+ and D- not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D- package pins.

Figure 70: Test/measurement load



3.21.5 Aurora interface

This section describes the Aurora clocking requirements and its DC and AC electrical characteristics.

3.21.5.1 Aurora clocking requirements for SD1_REF_CLK*n*_P and SD1_REF_CLKn_N

For more information on these specifications, see SerDes reference clocks.

3.21.5.2 Aurora DC electrical characteristics

This section describes the DC electrical characteristics for the Aurora interface.

3.21.5.2.1 Aurora transmitter DC electrical characteristics

This table defines the Aurora transmitter DC electrical characteristics.

Table 125: Aurora transmitter DC electrical characteristics (XV_{DD} = 1.35 V)[1]

Parameter	Symbol	Min	Typical	Max	Unit
Differential output voltage	V_{DIFFPP}	800	1000	1600	mV p-p
DC Differential transmitter impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω

Note:
1. For recommended operating conditions, see Table 4.

3.21.5.2.2 Aurora receiver DC electrical characteristics

This table defines the Aurora receiver DC electrical characteristics for the Aurora interface.

Table 126: Aurora receiver DC electrical characteristics (SV_{DD} = 1.0V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Differential input voltage	V_{IN}	200	-	1600	mV p-p	2
DC Differential receiver impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	3

Notes:
1. For recommended operating conditions, see Table 4.
2. Measured at receiver.
3. DC Differential receiver impedance

3.21.5.3 Aurora AC timing specifications

This section describes the AC timing specifications for Aurora.

3.21.5.3.1 Aurora transmitter AC timing specifications

This table defines the Aurora transmitter AC timing specifications. RefClk jitter is not included.

Table 127: Aurora transmitter AC timing specifications[1]

Parameter	Symbol	Min	Typical	Max	Unit
Deterministic jitter	J_D	-	-	0.17	UI p-p
Total jitter	J_T	-	-	0.35	UI p-p
Unit interval: 2.5 GBaud	UI	400 - 100 ppm	400	400 + 100 ppm	ps
Unit interval: 5.0 GBaud	UI	200 - 100 ppm	200	200 + 100 ppm	ps

Note:
1. For recommended operating conditions, see Table 4.

3.21.5.3.2 Aurora receiver AC timing specifications

This table defines the Aurora receiver AC timing specifications. RefClk jitter is not included.

Table 128: Aurora receiver AC timing specifications[3]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Deterministic jitter tolerance	J_D	-	-	0.37	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	-	-	0.55	UI p-p	1
Total jitter tolerance	J_T	-	-	0.65	UI p-p	1, 2
Bit error rate	BER	-	-	10^{-12}	-	-
Unit Interval: 2.5 GBaud	UI	400 - 100 ppm	400	400 + 100 ppm	ps	-
Unit Interval: 5.0 GBaud	UI	200 - 100 ppm	200	200 + 100 ppm	ps	-

Notes:
1. Measured at receiver
2. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 21. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.
3. For recommended operating conditions, see Table 4.

3.21.6 Serial ATA (SATA) interface

This section describes the DC and AC electrical specifications for the serial ATA (SATA) interface.

3.21.6.1 SATA DC electrical characteristics

This section describes the DC electrical characteristics for SATA.

3.21.6.1.1 SATA DC transmitter output characteristics

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen1i/1m or 1.5 Gbits/s transmission.

Table 129: Gen1i/1m 1.5G transmitter DC specifications ($X1V_{DD}$ = 1.35 V)[3]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Tx differential output voltage	V_{SATA_TXDIFF}	400	500	600	mV p-p	0
Tx differential pair impedance	$Z_{SATA\_TXDIFFIM}$	85	100	115	Ω	2

Notes:
1. Terminated by 50 Ω load
2. DC impedance
3. For recommended operating conditions, see Table 4.

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen2i/2m or 3.0 Gbits/s transmission.

Table 130: Gen 2i/2m 3G transmitter DC specifications ($X1V_{DD}$ = 1.35 V)[2]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Transmitter differential output voltage	V_{SATA_TXDIFF}	400	-	700	mV p-p	1
Transmitter differential pair impedance	$Z_{SATA\_TXDIFFIM}$	85	100	115	Ω	-

Notes:
1. Terminated by 50Ω load.
2. For recommended operating conditions, see Table 4.

3.21.6.1.2 SATA DC receiver input characteristics

This table provides the Gen1i/1m or 1.5 Gbits/s differential receiver input DC characteristics for the SATA interface.

Table 131: Gen1i/1m 1.5 G receiver input DC specifications (SV_{DD} = 1.0 V)[3]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input voltage	V_{SATA_RXDIFF}	240	500	600	mV p-p	1
Differential receiver input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	2
OOB signal detection threshold	V_{SATA_OOB}	50	120	240	mV p-p	-

Notes:
1. Voltage relative to common of either signal comprising a differential pair
2. DC impedance
3. For recommended operating conditions, see Table 4.

This table provides the Gen2i/2m or 3 Gbits/s differential receiver input DC characteristics for the SATA interface.

Table 132: Gen2i/2m 3 G receiver input DC specifications (SV_{DD} = 1.0 V)[3]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input voltage	V_{SATA_RXDIFF}	240	-	750	mV p-p	1
Differential receiver input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	2
OOB signal detection threshold	V_{SATA_OOB}	75	120	240	mV p-p	2

Notes:
1. Voltage relative to common of either signal comprising a differential pair
2. DC impedance
3. For recommended operating conditions, see Table 4.

3.21.6.2 SATA AC timing specifications

This section discusses the SATA AC timing specifications.

3.21.6.2.1 AC requirements for SATA REF_CLK

The AC requirements for the SATA reference clock listed in this table are to be guaranteed by the customer's application design.

Table 133: SATA reference clock input requirements[6]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SD1_REF_CLKn_P/SD1_REF_CLKn_N frequency range	t_{CLK_REF}	-	100/125	-	MHz	1
SD1_REF_CLKn_P/SD1_REF_CLKn_N clock frequency tolerance	t_{CLK_TOL}	-350	-	+350	ppm	-
SD1_REF_CLKn_P/SD1_REF_CLKn_N reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	5
SD1_REF_CLKn_P/SD1_REF_CLKn_N cycle- to-cycle clock jitter (period jitter)	t_{CLK_CJ}	-	-	100	ps	2
SD1_REF_CLKn_P/SD1_REF_CLKn_N total reference clock jitter, phase jitter (peak-to-peak)	t_{CLK_PJ}	-50	-	+50	ps	2, 3, 4

Notes:
1. Caution: Only 100 and 125MHz have been tested. In-between values do not work correctly with the rest of the system.
2. At RefClk input
3. In a frequency band from 150 kHz to 15 MHz at BER of 10-12
4. Total peak-to-peak deterministic jitter must be less than or equal to 50 ps.
5. Measurement taken from differential waveform
6. For recommended operating conditions, see Table 4.

3.21.6.3 AC transmitter output characteristics

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen1i/1m or 1.5 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 134: Gen1i/1m 1.5 G transmitter AC specifications[2]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Channel speed	t_{CH_SPEED}	-	1.5	-	Gbps	-
Unit Interval	T_{UI}	666.4333	666.6667	670.2333	ps	-
Total jitter data-data 5 UI	$U_{SATA\_TXTJ5UI}$	-	-	0.355	UI p-p	1
Total jitter, data-data 250 UI	$U_{SATA\_TXTJ250UI}$	-	-	0.47	UI p-p	1
Deterministic jitter, data-data 5 UI	$U_{SATA\_TXDJ5UI}$	-	-	0.175	UI p-p	1
Deterministic jitter, data-data 250 UI	$U_{SATA\_TXDJ250UI}$	-	-	0.22	UI p-p	1

Notes:
1. Measured at transmitter output pins peak to peak phase variation, random data pattern
2. For recommended operating conditions, see Table 4.

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen2i/2m or 3.0 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 135: Gen 2i/2m 3 G transmitter AC specifications[2]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Channel speed	t_{CH_SPEED}	-	3.0	-	Gbps	-
Unit Interval	T_{UI}	333.2167	333.3333	335.1167	ps	-
Total jitter fC3dB = fBAUD ÷ 500	$U_{SATA\_TXTJfB/500}$	-	-	0.37	UI p-p	1
Total jitter fC3dB = fBAUD ÷ 1667	$U_{SATA\_TXTJfB/1667}$	-	-	0.55	UI p-p	1
Deterministic jitter, fC3dB = fBAUD ÷ 500	$U_{SATA\_TXDJfB/500}$	-	-	0.19	UI p-p	1
Deterministic jitter, fC3dB = fBAUD ÷ 1667	$U_{SATA\_TXDJfB/1667}$	-	-	0.35	UI p-p	1

Notes:
1. Measured at transmitter output pins peak-to-peak phase variation, random data pattern
2. For recommended operating conditions, see Table 4.

3.21.6.4 AC differential receiver input characteristics

This table provides the Gen1i/1m or 1.5 Gbits/s differential receiver input AC characteristics for the SATA interface. The AC timing specifications do not include RefClk jitter.

Table 136: Gen 1i/1m 1.5G receiver AC specifications[2]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Unit Interval	T_{UI}	666.4333	666.6667	670.2333	ps	-
Total jitter data-data 5 UI	$U_{SATA\_RXTJ5UI}$	-	-	0.43	UI p-p	1
Total jitter, data-data 250 UI	$U_{SATA\_RXTJ250UI}$	-	-	0.60	UI p-p	1
Deterministic jitter, data-data 5 UI	$U_{SATA\_RXDJ5UI}$	-	-	0.25	UI p-p	1
Deterministic jitter, data-data 250 UI	$U_{SATA\_RXDJ250UI}$	-	-	0.35	UI p-p	1

Notes:
1. Measured at receiver.
2. For recommended operating conditions, see Table 4.

This table provides the differential receiver input AC characteristics for the SATA interface at Gen2i/2m or 3.0 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 137: Gen 2i/2m 3G receiver AC specifications[2]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Unit Interval	T_{UI}	333.2167	333.3333	335.1167	ps	-
Total jitter fC3dB = fBAUD ÷ 500	$U_{SATA\_RXTJfB/500}$	-	-	0.60	UI p-p	1
Total jitter fC3dB = fBAUD ÷ 1667	$U_{SATA\_RXTJfB/1667}$	-	-	0.65	UI p-p	1
Deterministic jitter, fC3dB = fBAUD ÷ 500	$U_{SATA\_RXDJfB/500}$	-	-	0.42	UI p-p	1
Deterministic jitter, fC3dB = fBAUD ÷ 1667	$U_{SATA\_RXDJfB/1667}$	-	-	0.35	UI p-p	1

Notes:
1. Measured at receiver
2. For recommended operating conditions, see Table 4.

4 HARDWARE DESIGN CONSIDERATIONS

4.1 System clocking

This section describes the PLL configuration of the chip.

4.1.1 PLL characteristics

Characteristics of the chip's PLLs include the following:

- There is a core cluster PLL that generates a clock for each core cluster from the externally supplied SYSCLK input.
- Core cluster Group A PLL
- The frequency ratio between the core cluster PLL and SYSCLK is selected using the configuration bits as described in Core cluster to SYSCLK PLL ratio. The frequency for each core cluster is selected using the configuration bits as described in Table 142.
- The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Platform to SYSCLK PLL ratio.
- Cluster group A generates an asynchronous clock for eSDHC SDR mode from CGA PLL, described in eSDHC SDR mode clock select.
- The DDR block PLL generates an asynchronous DDR clock from the externally supplied DDRCLK input. The frequency ratio is selected using the Memory Controller Complex PLL multiplier/ratio configuration bits as described in DDR controller PLL ratios.
- SerDes block has two PLLs that generate a core clock from their respective
- externally supplied SD1_REF_CLK*n*_P/SD1_REF_CLK*n*_N inputs. The frequency ratio is selected using the SerDes PLL RCW configuration bits as described in SerDes PLL ratio.
- When using Single Oscillator Source clocking mode, a single onboard oscillator can provide the reference clock (100 MHz) to all the PLLs (that is, Platform PLL, Core Cluster PLLs, DDR PLL, USB PLL and SerDes PLLs).

4.1.2 Clock ranges

This table provides the clocking specifications for the processor core, platform, memory, and integrated flash controller.

Table 138: Processor, platform, and memory clocking specifications

Characteristic	Maximum processor core frequency						Unit	Notes
	1000 MHz		1200 MHz		1400 MHz			
	Min	Max	Min	Max	Min	Max		
Core cluster group PLL frequency	1000	1000	1000	1200	1000	1400	MHz	1, 2
Core cluster frequency	500	1000	500	1200	500	1400	MHz	2
Platform clock frequency	256	400	256	400	256	400	MHz	1, 6
Memory bus clock frequency (DDR3L)	500	800	500	800	500	800	MHz	1, 3, 4
Memory bus clock frequency (DDR4)	625	800	625	800	625	800	MHz	1, 3, 4
IFC clock frequency	–	100	–	100	–	100	MHz	5
FMAN	500	500	500	600	500	700	MHz	–

Notes:

1. Caution: The platform clock to SYSCLK ratio and core to SYSCLK ratio settings must be chosen such that the resulting SYSCLK frequency, core frequency, and platform clock frequency do not exceed their respective maximum or minimum operating frequencies
2. The core cluster runs at cluster group A PLL. The core cluster group A PLL minimum frequency is 1000 MHz. With a minimum cluster group PLL frequency of 1000 MHz, this results in a minimum allowable core cluster frequency of 500 MHz. Frequency provided to the e5500 cluster after any dividers must always be greater than or equal to the platform frequency. For the case of the platform frequency = 400 MHz, the minimum core cluster frequency is 500 MHz.
3. The memory bus clock speed is half the DDR3L/DDR4 data rate.
4. The memory bus clock speed is dictated by its own PLL.
5. The integrated flash controller (IFC) clock speed on IFC_CLK[0:1] is determined by the IFC module input clock (platform clock / 2) divided by the IFC ratio programmed in CCR[CLKDIV]. See the chip reference manual for more information.
6. The minimum platform frequency should meet the requirements in Minimum platform frequency requirements for high-speed interfaces.
7. "Single Oscillator Source" Reference clock mode supports differential reference clock pair frequency of 100 MHz.

4.1.2.1.1 DDR clock ranges

The DDR memory controller can run only in asynchronous mode, where the memory bus is clocked with the clock provided on the DDRCLK input pin, which has its own dedicated PLL.

This table provides the clocking specifications for the memory bus.

Table 139: Memory bus clocking specifications

Characteristic		Min	Max	Unit	Notes
Memory bus clock frequency	DDR3L	500	800	MHz	1, 2, 3, 4
	DDR4	625	800		

Notes:

1. Caution: The platform clock to SYSCLK ratio and core to SYSCLK ratio settings must be chosen such that the resulting SYSCLK frequency, core frequency, and platform frequency do not exceed their respective maximum or minimum operating frequencies. See Platform to SYSCLK PLL ratio, Core cluster to SYSCLK PLL ratio, and DDR controller PLL ratios for ratio settings.
2. The memory bus clock refers to the chip's memory controllers' D1_MCK[0:1] and D1_MCK[0:1]_B output clocks, running at half of the DDR data rate.
3. The memory bus clock speed is dictated by its own PLL. See DDR controller PLL ratios.
4. The minimum frequency supported by DDR4 is 1250 MT/s.

4.1.3 Platform to SYSCLK PLL ratio

This table lists the allowed platform clock to SYSCLK ratios.

Because the DDR operates asynchronously, the memory-bus clock frequency is decoupled from the platform bus frequency.

For all valid platform frequencies supported on this chip, set the RCW Configuration field SYS_PLL_CFG = 0b00.

Table 140: Platform to SYSCLK PLL ratios

Binary Value of SYS_PLL_RAT	Platform:SYSCLK Ratio
0_0011	3:1
0_0100	4:1
0_0101	5:1
0_0110	6:1
0_0111	7:1
0_1000	8:1
0_1001	9:1
All Others	Reserved

4.1.4 Core cluster to SYSCLK PLL ratio

The clock ratio between SYSCLK and each of the core cluster PLLs is determined by the binary value of the RCW Configuration field CGA_PLLn_RAT. This table describes the supported ratios. For all valid core cluster frequencies supported on this chip, set the RCW Configuration field CGA_PLLn_CFG = 0b00.

This table lists the supported asynchronous core cluster to SYSCLK ratios.

Table 141: Core cluster PLL to SYSCLK ratios

Binary value of CGA_PLLn_RAT(n=1 or 2)	Core cluster:SYSCLK Ratio
00_0110	6:1
00_0111	7:1
00_1000	8:1
00_1001	9:1
00_1010	10:1
00_1011	11:1
00_1100	12:1
00_1101	13:1
00_1110	14:1
00_1111	15:1
01_0000	16:1
01_0010	18:1
01_0100	20:1
01_0110	22:1
01_1001	25:1
01_1010	26:1
01_1011	27:1
All others	Reserved

4.1.5 Core complex PLL select

The clock frequency of each core cluster is determined by the binary value of the RCW Configuration field Cn_PLL_SEL. These tables describe the selections available to each core cluster, where each individual core cluster can select a frequency from their respective tables.

NOTE
There is a restriction that requires that the frequency provided to the e5500 core cluster after any dividers must always be greater than half of the platform frequency. Special care must be used when selecting the /2 outputs of a cluster PLL in which this restriction is observed.

Table 142: Core cluster PLL select

Binary Value of Cn_PLL_SEL for n=1-4	Core cluster ratio
0000	CGA PLL1 /1
0001	CGA PLL1 /2
All Others	Reserved

4.1.6 DDR controller PLL ratios

The DDR memory controller operates asynchronous to the platform.

In asynchronous DDR mode, the DDR data rate to DDRCLK ratios supported are listed in the following table. This ratio is determined by the binary value of the RCW Configuration field MEM_PLL_RAT (bits 10-15).

The RCW Configuration field MEM_PLL_CFG (bits 8-9) must be set to MEM_PLL_CFG = 0b00 for all valid DDR PLL reference clock frequencies supported on this chip.

Table 143: DDR clock ratio

Binary value of MEM_PLL_RAT	DDR data-rate:DDRCLK ratio	Maximum supported DDR data-rate (MT/s)
00_1000	8:1	1066
00_1010	10:1	1333
00_1011	11:1	1465
00_1100	12:1	1600
00_1101	13:1	1300
00_1110	14:1	1400
00_1111	15:1	1500
01_0000	16:1	1600
1_0100	20:1	1333
1_1000	24:1	1600
All Others	Reserved	–

4.1.7 SerDes PLL ratio

The clock ratio between each of the two SerDes PLLs and their respective externally supplied SD1_REF_CLKn_P/SD1_REF_CLKn_N inputs is determined by a set of RCW Configuration fields (SRDS_PRTCL_S1, SRDS_PLL_REF_CLK_SEL_S1, and SRDS_DIV_*_S1), as shown in this table.

Table 144: Valid SerDes RCW encodings and reference clocks

SerDes protocol (given lane)	Valid reference clock frequency	Legal setting for SRDS_PRTCL_S1	Legal setting for SRDS_PLL_REF_CLK_SEL_S1	Legal setting for SRDS_DIV_*_S1	Notes
High-speed serial interfaces					
PCI Express 2.5 Gbps	100 MHz	Any PCIe	0b0: 100 MHz	2b10: 2.5 G	1
(doesn't negotiate upwards)	125 MHz		0b1: 125 MHz		1
PCI Express 5 Gbps	100 MHz	Any PCIe	0b0: 100 MHz	2b01: 5.0 G	1
(can negotiate up to 5 Gbps)	125 MHz		0b1: 125 MHz		1
SATA (1.5 or 3 Gbps)	100 MHz	SATA	0b0: 100 MHz	Don't care	2
	125 MHz		0b1: 125 MHz		
Debug (2.5 Gbps)	100 MHz	Aurora @ 2.5 or 5 Gbps	0b0: 100 MHz	0b1: 2.5 G	–
	125 MHz		0b1: 125 MHz		–
Debug (5 Gbps)	100 MHz	Aurora @ 2.5 or 5 Gbps	0b0: 100 MHz	0b0: 5.0 G	–
	125 MHz		0b1: 125 MHz		–
Networking interfaces					
SGMII (1.25 Gbps)	100 MHz	SGMII @ 1.25 Gbps	0b0: 100 MHz	Don't care	–
	125 MHz	1000Base-KX @ 1.25 Gbps	0b1: 125 MHz		–
QSGMII (5.0 Gbps)	100 MHz	Any QSGMII	0b0: 100 MHz	0b0: 5.0 G	–
	125 MHz		0b1: 125 MHz		–
2.5G SGMII (3.125 Gbps)	125 MHz	SGMII @ 3.125 Gbps	0b0: 125 MHz	Don't care	–
XFI (10.3125 Gbps)	156.25 MHz	XFI @ 10.3125 Gbps	0b0: 156.25 MHz	Don't care	–

Notes:

1. A spread-spectrum reference clock is permitted for PCI Express. However, if any other high-speed interface, such as SATA, SGMII, QSGMII, 1000Base-KX, or Aurora is used concurrently on the same SerDes PLL, spread-spectrum clocking is not permitted.
2. SerDes lanes configured as SATA initially operate at 3.0 Gbps. A 1.5 Gbps operation may later be enabled through the SATA IP itself. It is possible for software to set each SATA at different rate.

4.1.8 eSDHC SDR mode clock select

The eSDHC SDR mode is asynchronous to the platform.

This table describes the clocking options that may be applied to the eSDHC SDR mode. The clock selection is determined by the binary value of the RCW Clocking Configuration field HWA_CGA_M1_CLK_SEL.

Table 145: eSDHC SDR mode clock select

Binary value of HWA_CGA_M1_CLK_SEL	eSDHC SDR mode frequency[1]
0b000	Reserved
0b001	Cluster group A PLL 1/1
0b010	Cluster group A PLL 1/2
0b011	Cluster group A PLL 1/3
0b100	Cluster group A PLL 1/4
0b101	Reserved

Notes:
1. For asynchronous mode max frequency, see the "Processor clocking specifications" table in the chip reference manual.
2. For SDR104 and HS200 modes, CGA1 PLL should be set to provide a minimum of 1200 MHz.
3. For SDR50 mode, cluster PLL should be set to provide a minimum of 600 MHz.

4.1.9 FMAN clock select

The FMAN clock is asynchronous to the platform clock. The FMAN clock selection is determined by the binary value of the RCW clocking configuration field HWA_CGA_M2_CLK_SEL. For the clock select options, see the *RCW Field Description* table in the chip reference manual.

4.1.10 Frequency options

This section discusses interface frequency options.

4.1.10.1 SYSCLK and core cluster frequency options

This table shows the expected frequency options for SYSCLK and core cluster frequencies.

Table 146: SYSCLK and core cluster frequency options

Core cluster: SYSCLK Ratio	SYSCLK (MHz)				
	64.00	66.67	100.00	125.00	133.33
	Core cluster Frequency (MHz)[1]				
6:1					
7:1					
8:1				1000	1067
9:1				1125	1200
10:1			1000	1250	1333
11:1			1100	1375	
12:1			1200		
13:1			1300		
14:1			1400		
15:1		1000			
16:1	1024	1067			
18:1	1152	1200			
20:1	1280	1333			
21:1	1344	1400			

Notes:
1. Core cluster frequency values are shown rounded up to the nearest whole number (decimal place accuracy removed).
2. When using single source clocking, only 100 MHz input is available.

4.1.10.2 SYSCLK and platform frequency options

This table shows the expected frequency options for SYSCLK and platform frequencies.

Table 147: SYSCLK and platform frequency options

Platform: SYSCLK Ratio	SYSCLK (MHz)				
	64.00	66.67	100.00	125.00	133.33
	Platform Frequency (MHz)[1]				
3:1			300	375	400
4:1	256	267	400		
5:1	320	333			
6:1	384	400			
7:1					
8:1					
9:1					

Notes:
1. Platform frequency values are shown rounded down to the nearest whole number (decimal place accuracy removed).
2. When using single source clocking, only 100 MHz options are valid.

4.1.10.3 DDRCLK and DDR data rate frequency options

This table shows the expected frequency options for DDRCLK and DDR data rate frequencies.

Table 148: DDRCLK and DDR data rate frequency options

DDR data rate: DDRCLK Ratio	DDRCLK (MHz)				
	64.00	66.67	100.00	125.00	133.33
	DDR Data Rate (MT/s)[1]				
8:1				1000	1066
10:1			1000	1250	1333
11:1			1100	1375	1465
12:1			1200	1500	1600
13:1			1300		
14:1			1400		
15:1		1000	1500		
16:1	1024	1067	1600		
20:1	1280	1333			
24:1	1536	1600			

Notes:
1. DDR data rate values are shown rounded up to the nearest whole number (decimal place accuracy removed).
2. When using single source clocking, only 100 MHz options are available.
3. The minimum frequency supported by DDR4 is 1250 MT/s.

4.1.10.4 SYSCLK and eSDHC high speed modes frequency options

These table shows the expected frequency options for SYSCLK and eSDHC high speed modes.

Table 149: SYSCLK and eSDHC high speed mode frequency options (clocked by CGA PLL1 / 1)

Core cluster: SYSCLK ratio	SYSCLK (MHz)				
	64.00	66.67	100.00	125.00	133.33
	Resultant frequency (MHz)[1]				
9:1					1200
12:1			1200		
18:1	1152	1200			

Notes:
1. Resultant frequency values are shown rounded up to the nearest whole number (decimal place accuracy removed).
2. For low speed operation, eSDHC is clocked from platform PLL and does not use CGA PLL.

4.1.10.5 Minimum platform frequency requirements for high-speed interfaces

The platform clock frequency must be considered for proper operation of high-speed interfaces as described below:

The platform clock frequency must be equal to 400 MHz for PCI Express Gen 2.

For proper PCI Express operation, the platform clock frequency must be greater than or equal to:

Figure 71: Gen 1 PEX minimum platform frequency

$$\frac{527\ \text{MHz} \times (\text{PCI Express Link width})}{8}$$

Figure 72: Gen 2 PEX minimum platform frequency

$$\frac{527\ \text{MHz} \times (\text{PCI Express Link width})}{4}$$

See section "Link Width," in the chip reference manual for PCI Express interface width details. Note that "PCI Express link width" in the above equation refers to the negotiated link width as the result of PCI Express link training, which may or may not be the same as the link width POR selection. It refers to the widest port in use, not the combined width of the number ports in use.

4.2 Power supply design

4.2.1 Core and platform supply voltage filtering

The V_{DD}, V_{DDC} supply is normally derived from a high current capacity linear or switching power supply which can regulate its output voltage very accurately despite changes in current demand from the chip within the regulator's relatively low bandwidth. Several bulk decoupling capacitors must be distributed around the PCB to supply transient current demand above the bandwidth of the voltage regulator.

These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. However, customers should work directly with their power regulator vendor for best values and types of bulk capacitors.

As a guideline for customers and their power regulator vendors, TELEDYNE E2V recommends that these bulk capacitors be chosen to maintain the positive transient power surges to less than 1.0 V+50 mV (negative transient undershoot should comply with specification of 1.0 V-30 mV) for current steps of up to 10A with a slew rate of 12 A/us.

These bulk decoupling capacitors will ideally supply a stable voltage for current transients into the megahertz range. Above that, see Decoupling recommendations for further decoupling recommendations.

4.2.2 PLL power supply filtering

Each of the PLLs described in System clocking is provided with power through independent power supply pins (AV_{DD}_PLAT, AV_{DD}_CGA1, AV_{DD}_D1 and AV_{DD}_SD1_PLLn). AV_{DD}_PLAT, AV_{DD}_CGA1 and AV_{DD}_D1 voltages must be derived directly from a 1.8 V voltage source through a low frequency filter scheme. AV_{DD}_SD1_PLLn voltages must be derived directly from the $X1V_{DD}$ source through a low frequency filter scheme. The recommended solution for PLL filtering is to provide independent filter circuits per PLL power supply, as illustrated in Figure 73, one for each of the AV_{DD} pins. By providing independent filters to each PLL, the opportunity to cause noise injection from one PLL to the other is reduced. This circuit is intended to filter noise in the PLL's resonant frequency range from a 500 kHz to 10 MHz range.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the footprint, without the inductance of vias.

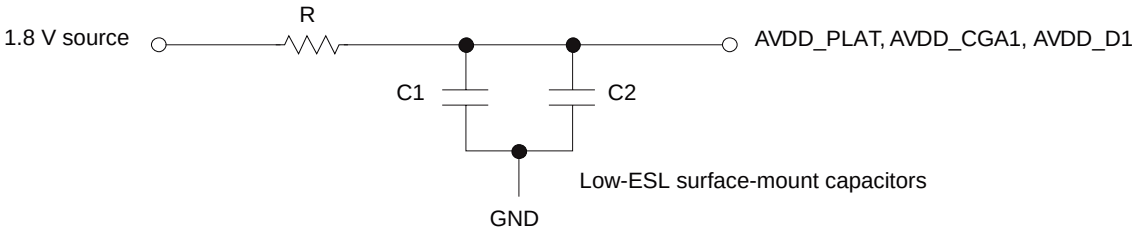
This figure shows the PLL power supply filter circuit. Where:

- R = 5 Ω ± 5%
- C1 = 10 µF ± 10%, 0603, X5R, with ESL ≤ 0.5 nH
- C2 = 1.0 µF ± 10%, 0402, X5R, with ESL ≤ 0.5 nH

NOTE
A higher capacitance value for C2 may be used to improve the filter as long as the other C2 parameters do not change (0402 body, X5R, ESL ≤ 0.5 nH).

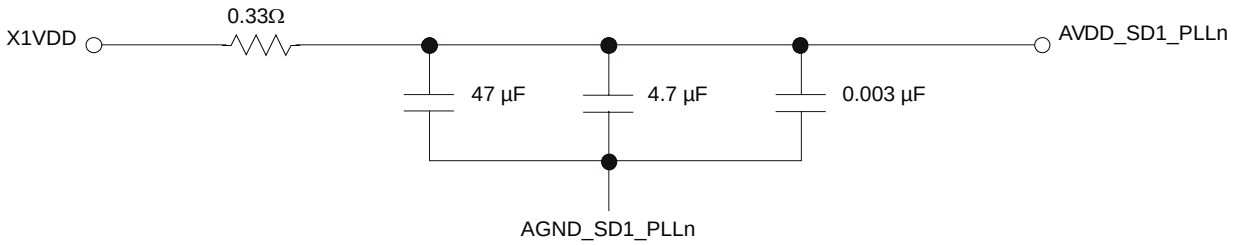
NOTE
Voltage for AVDD is defined at the input of the PLL supply filter and not the pin of AVDD.

Figure 73: PLL power supply filter circuit



The AV_{DD}_SD1_PLLn signals provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following Figure 74. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD}_SD1_PLLn balls to ensure it filters out as much noise as possible. The ground connection should be near the AV_{DD}_SD1_PLLn balls. The 0.003-µF capacitors closest to the balls, followed by a 4.7-µF and 47-µF capacitor, and finally the 0.33 Ω resistor to the board supply plane. The capacitors are connected from AV_{DD}_SD*1*_PLL*n* to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide, and direct.

Figure 74: SerDes PLL power supply filter circuit



Note the following:

- AV_{DD}_SD*n*_PLL*n* should be a filtered version of XnV_{DD}.
- Signals on the SerDes interface are fed from the $X1V_{DD}$ power plane.
- Voltage for AVDD_SD1_PLLn is defined at the PLL supply filter and not the pin of AVDD_SD1_PLLn.
- A 47-µF 0805 XR5 or XR7, 4.7-µF 0603, and 0.003-µF 0402 capacitor are recommended. The size and material type are important. A 0.33-Ω ± 1% resistor is recommended.
- There needs to be dedicated analog ground, AGND_SD1_PLL*n* for each AV_{DD}_SD1_PLL*n* pin up to the physical local of the filters themselves.

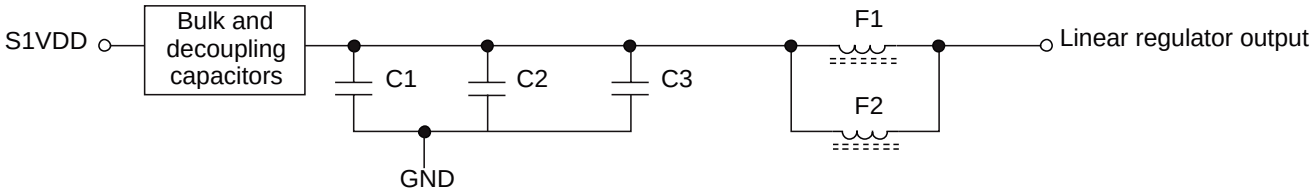
4.2.3 $S1V_{DD}$ power supply filtering

$S1V_{DD}$ should be supplied by a linear regulator.

An example solution for $S1V_{DD}$ filtering, is illustrated in Figure 75. The component values in this example filter are system dependent and are still under characterization, component values may need adjustment based on the system or environment noise.
Where:

- C1 = 0.003 µF ± 10%, X5R, with ESL ≤ 0.5 nH
- C2 and C3 = 2.2 µF ± 10%, X5R, with ESL ≤ 0.5 nH
- F1 and F2 = 120 Ω at 100 MHz 2A 25% 0603 Ferrite (for example, Murata BLM18PG121SH1)
- Bulk and decoupling capacitors are added, as needed, per power supply design.

Figure 75: SV_{DD} power supply filter circuit



Note the following:

- Refer to Power-on ramp rate, for maximum S1VDD power-up ramp rate.
- There needs to be enough output capacitance or a soft start feature to assure ramp rate requirement is met.
- The ferrite beads should be placed in parallel to reduce voltage droop.
- Besides a linear regulator, a low noise dedicated switching regulator can also be used. 10 mVp-p, 50kHz - 500MHz is the noise goal.

4.2.4 $X1V_{DD}$ power supply filtering

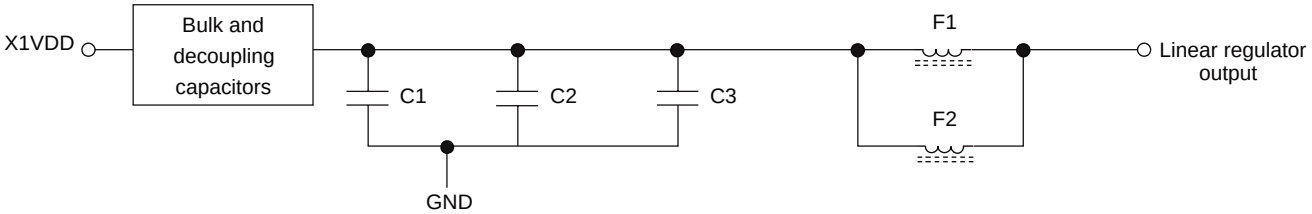
$X1V_{DD}$ may be supplied by a linear regulator or sourced by a filtered $G1V_{DD}$. Systems may design in both options to allow flexibility to address system noise dependencies. However, for initial system bring-up, the linear regulator option is highly recommended.

An example solution for $X1V_{DD}$ filtering, where $X1V_{DD}$ is sourced from a linear regulator, is illustrated in Figure 76. The component values in this example filter are system dependent and are still under characterization, component values may need adjustment based on the system or environment noise.

Where:

- C1 = 0.003 µF ± 10%, X5R, with ESL ≤ 0.5 nH
- C2 and C3 = 2.2 µF ± 10%, X5R, with ESL ≤ 0.5 nH
- F1 and F2 = 120 Ω at 100 MHz 2A 25% 0603 Ferrite (for example, Murata BLM18PG121SH1)
- Bulk and decoupling capacitors are added, as needed, per power supply design.

Figure 76: $X1V_{DD}$ power supply filter circuit



Note the following:

- See Power-on ramp rate for maximum X1VDD power-up ramp rate.
- There needs to be enough output capacitance or a soft-start feature to assure ramp rate requirement is met.
- The ferrite beads should be placed in parallel to reduce voltage droop.
- Besides a linear regulator, a low-noise, dedicated switching regulator can be used. 10 mVp-p, 50 kHz - 500 MHz is the noise goal.

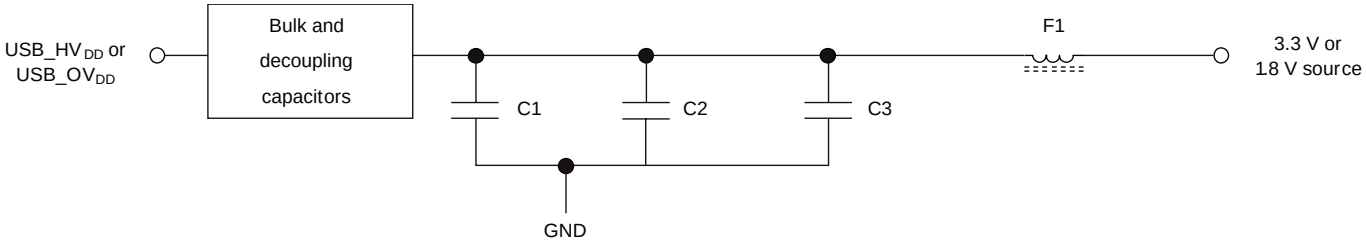
4.2.5 USB_HV$_{DD}$ and USB_OV$_{DD}$ power supply filtering

USB_HV$_{DD}$ and USB_OV$_{DD}$ must be sourced by a filtered 3.3 V and 1.8 V voltage source using a star connection. An example solution for USB_HV$_{DD}$ and USB_OV$_{DD}$ filtering, where USB_HV$_{DD}$ and USB_OV$_{DD}$ are sourced from a 3.3 V and 1.8 V voltage source, is illustrated in the following figure. The component values in this example filter is system dependent and are still under characterization, component values may need adjustment based on the system or environment noise.

Where:

- C1 = 0.003 µF ± 10%, X5R, with ESL ≤ 0.5 nH
- C2 and C3 = 2.2 µF ± 10%, X5R, with ESL ≤ 0.5 nH
- F1 = 120 Ω at 100 MHz 2A 25% 0603 Ferrite (for example, Murata BLM18PG121SH1)
- Bulk and decoupling capacitors are added, as needed, per power supply design.

Figure 77: USB_HV$_{DD}$ and USB_OV$_{DD}$ power supply filter circuit



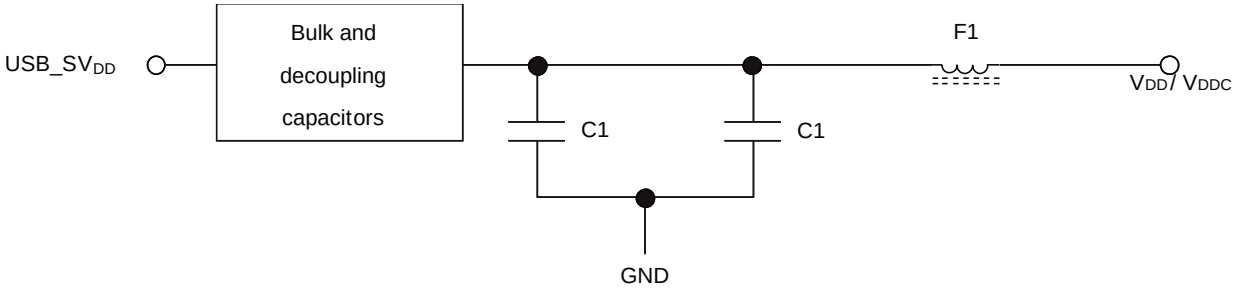
4.2.6 USB_SV$_{DD}$ power supply filtering

USB_SV$_{DD}$ must be sourced by a filtered V$_{DD}$or V$_{DDC}$using a star connection. An example solution for USB_SV$_{DD}$ filtering, where USB_SV$_{DD}$ is sourced from V$_{DD}$, is illustrated in the following figure. The component values in this example filter is system dependent and are still under characterization, component values may need adjustment based on the system or environment noise.

Where:

- C1 = 2.2 µF ± 20%, X5R, with Low ESL (for example, Panasonic ECJ0EB0J225M)
- F1 = 120 Ω at 100-MHz 2A 25% Ferrite (for example, Murata BLM18PG121SH1)
- Bulk and decoupling capacitors are added, as needed, per power supply design.

Figure 78: USB_SV$_{DD}$ power supply filter circuit



4.3 Decoupling recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the chip system, and the chip itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V$_{DD}$, V$_{DDC}$, CV$_{DD}$, On V$_{DD}$, DV$_{DD}$, EV$_{DD}$, GnV$_{DD}$, and LnV$_{DD}$ pin of the device. These decoupling capacitors should receive their power from separate V$_{DD}$, CV$_{DD}$, OnV$_{DD}$, DV$_{DD}$, EV$_{DD}$, GnV$_{DD}$, LnV$_{DD}$, and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0201 sizes.

As presented in Core and platform supply voltage filtering, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, V_{DDC} and other planes (for example, CV_{DD}, On V_{DD}, DV_{DD}, EV_{DD}, GnV_{DD}, and LnV_{DD}), to enable quick recharging of the smaller chip capacitors.

4.4 SerDes block power supply decoupling recommendations

The SerDes block requires a clean, tightly regulated source of power ($S1V_{DD}$ and $X1V_{DD}$) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

NOTE
Only SMT capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

1. The board should have at least 1 x 0.1-uF SMT ceramic chip capacitor placed as close as possible to each supply ball of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.
2. Between the device and any SerDes voltage regulator there should be a lower bulk capacitor for example a 10-uF, low ESR SMT tantalum or ceramic and a higher bulk capacitor for example a 100uF - 300-uF low ESR SMT tantalum or ceramic capacitor.

4.5 Connection recommendations

The following is a list of connection recommendations:

- To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unless otherwise noted in this document, all unused active low inputs should be tied to V_{DD}, On V_{DD}, DV_{DD}, GnV_{DD}, EV_{DD}, CV_{DD} and LnV_{DD} as required. All unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected. Power and ground connections must be made to all external V_{DD}, OnV_{DD}, DV_{DD}, GnV_{DD}, LnV_{DD} , EV_{DD} , CV_{DD} and GND pins of the device.
- The TEST_SEL_B pin must be pulled to $O1V_{DD}$ through a 100-ohm to 1k-ohm resistor for T1024 and tied to ground for T1014.
- The chip has temperature diodes on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461A™). If a temperature diode monitoring device is not connected, these pins may be connected to test points or grounded.

4.5.1 Legacy JTAG configuration signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 80: Legacy JTAG Interface Connection. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The TRST_B signal is optional in the IEEE Std 1149.1 specification, but it is provided on all processors built on Power Architecture technology. The device requires TRST_B to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert TRST_B during the power-on reset flow. Simply tying TRST_B to PORESET_B is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert PORESET_B or TRST_B in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 80: Legacy JTAG Interface Connection allows the COP port to independently assert PORESET_B or TRST_B, while ensuring that the target can drive PORESET_B as well.

The COP interface has a standard header, shown in Figure 79, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to- bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 79 is common to all known emulators.

4.5.1.1 Termination of unused signals

If the JTAG interface and COP header will not be used, TELEDYNE E2V recommends the following connections:

- TRST_B should be tied to PORESET_B through a 0 kΩ isolation resistor so that it is asserted when the system reset signal (PORESET_B) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. TELEDYNE E2V recommends that the COP header be designed into the system as shown in Figure 80. If this is not possible, the isolation resistor will allow future access to TRST_B in case a JTAG interface may need to be wired onto the system in future debug situations.
- No pull-up/pull-down is required for TDI, TMS or TDO.

Figure 79: Legacy COP Connector Physical Pinout

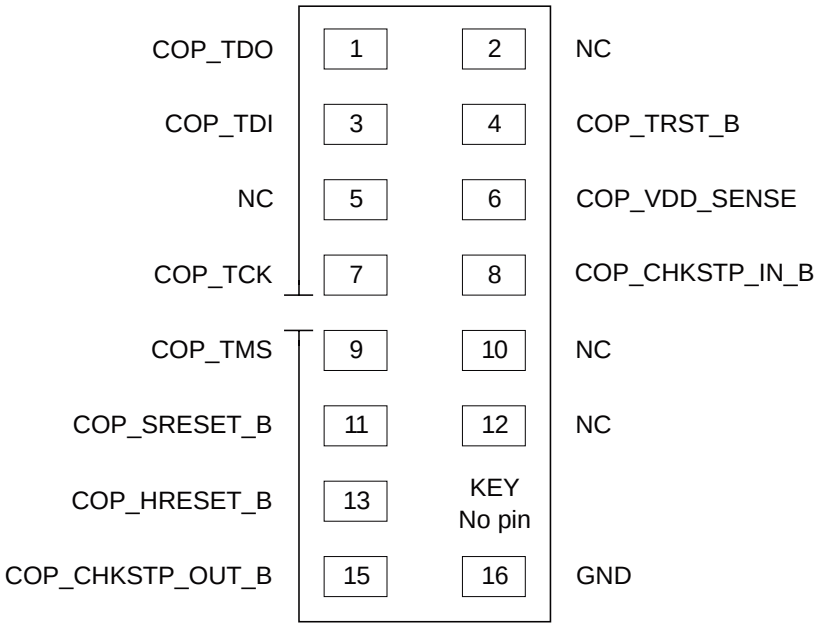
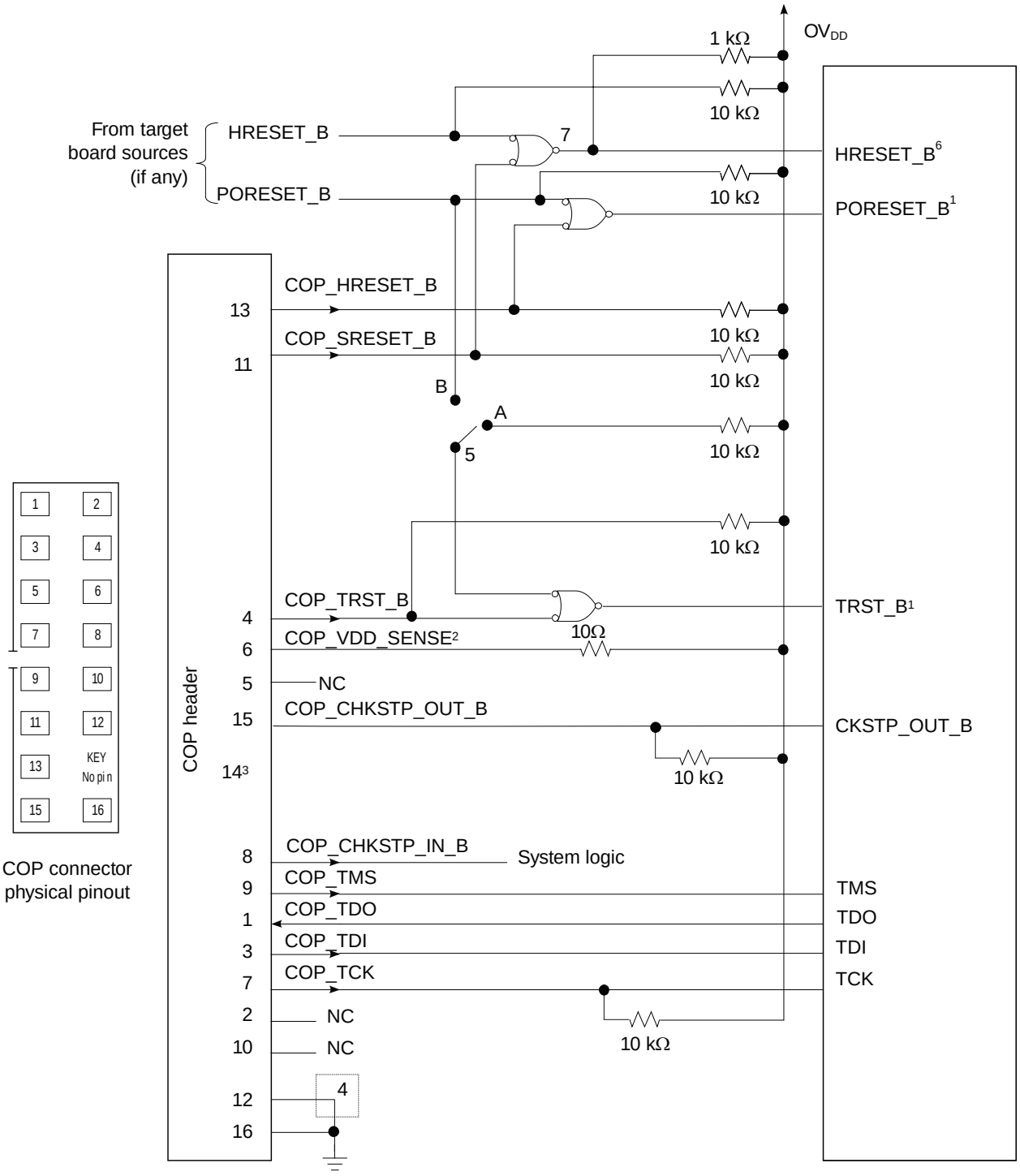


Figure 80: Legacy JTAG Interface Connection



Notes:

1. The COP port and target board should be able to independently assert PORESET_B and TRST_B to the processor in order to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a no-connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the TRST_B line. If BSDL testing is not being performed, this switch should be closed to position B.
6. Asserting HRESET_B causes a hard reset on the device
7. This is an open-drain output gate.

4.5.2 Aurora configuration signals

Correct operation of the Aurora interface requires configuration of a group of system control pins as demonstrated in the figures below. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

TELEDYNE E2V recommends that the Aurora 34 pin duplex connector be designed into the system as shown in Figure 83 or the 70 pin duplex connector be designed into the system as shown in Figure 84.

If the Aurora interface will not be used, TELEDYNE E2V recommends the legacy COP header be designed into the system as described in.

Figure 81: Aurora 34 pin connector duplex pinout

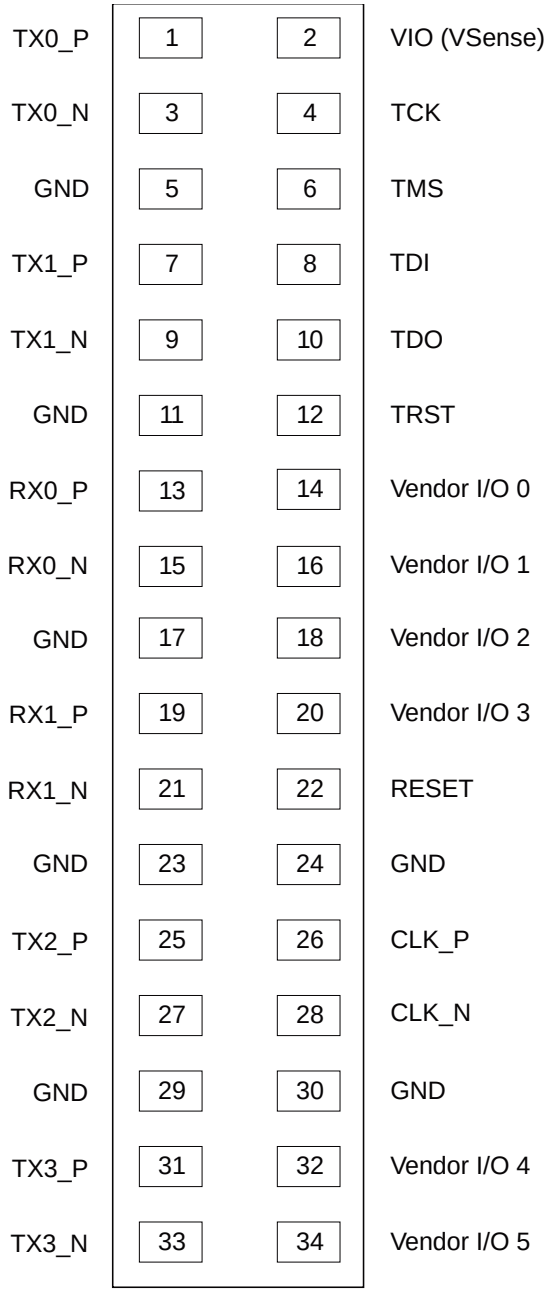


Figure 82: Aurora 70 pin connector duplex pinout

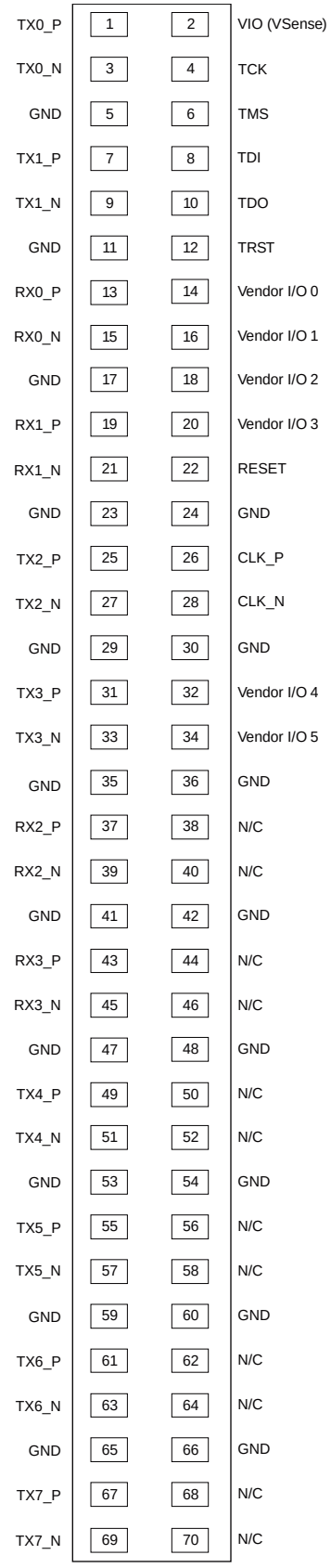
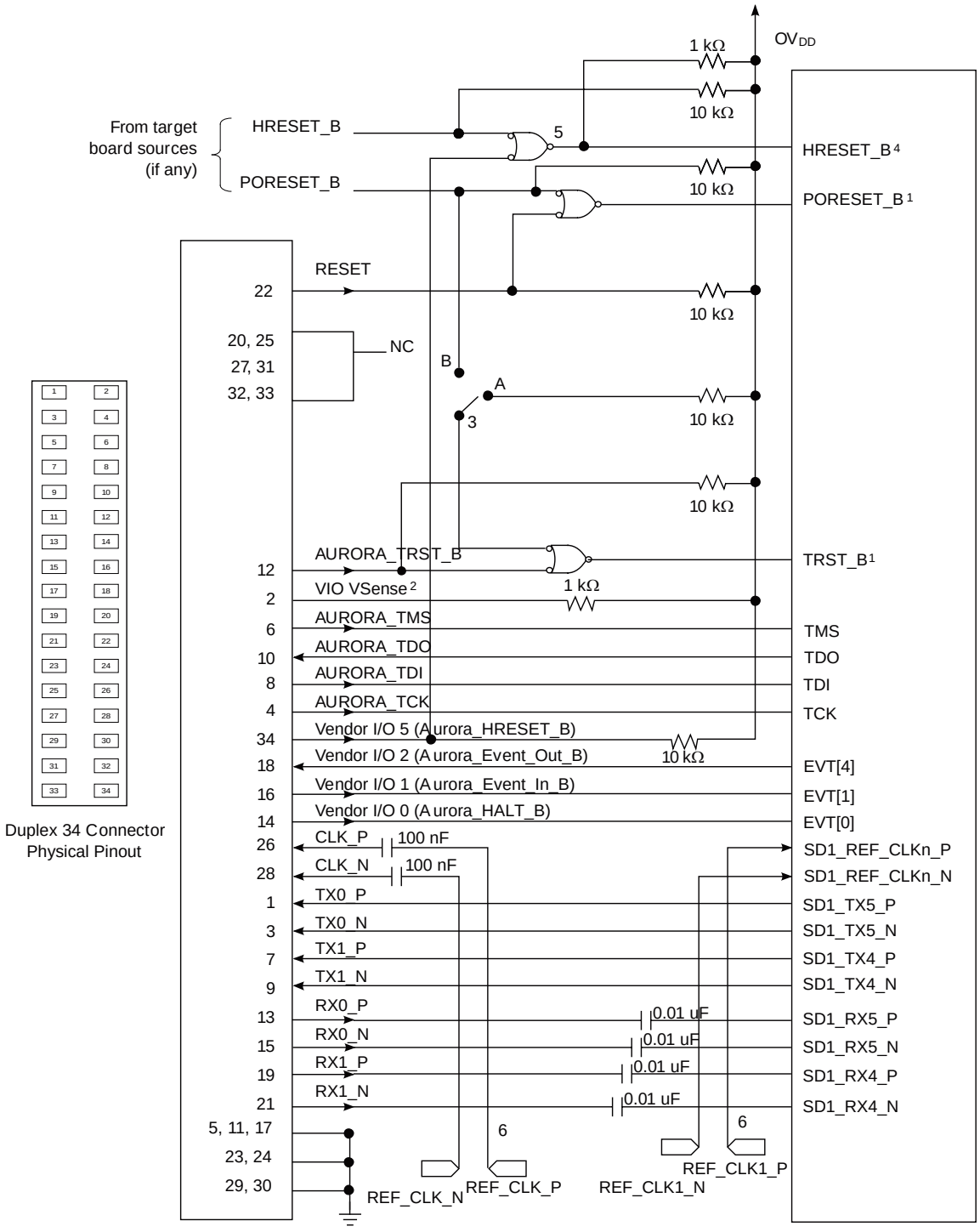


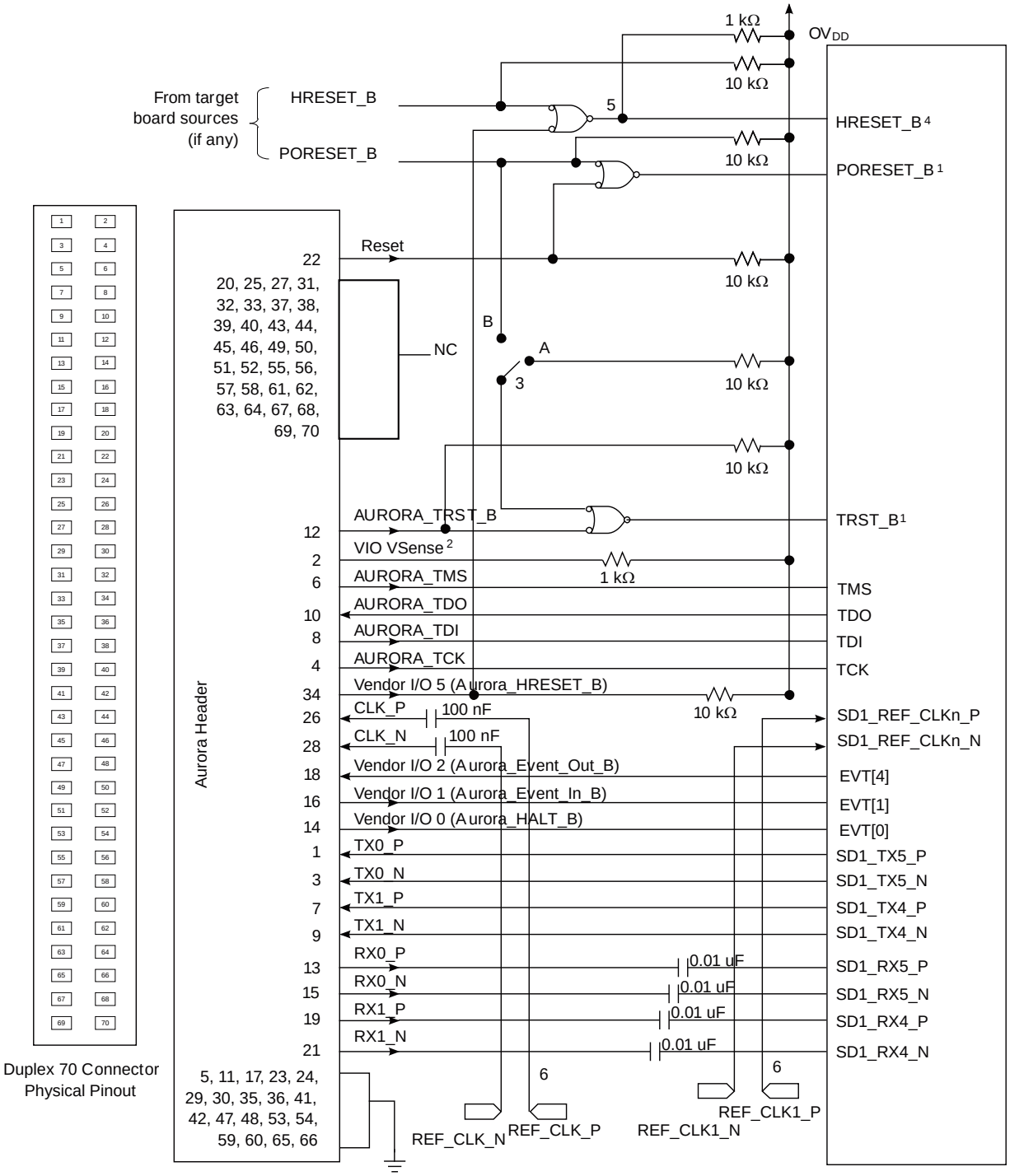
Figure 83: Aurora 34 pin connector duplex interface connection



Notes:

1. The Aurora port and target board should be able to independently assert PORESET_B and TRST_B to the processor in order to fully control the processor as shown here.
2. Populate this with a 1 kΩ resistor for short-circuit/current-limiting protection.
3. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the TRST_B line. If BSDL testing is not being performed, this switch should be closed to position B.
4. Asserting HRESET_B causes a hard reset on the device
5. This is an open-drain output gate.
6. REF_CLK_P/REF_CLK_N and REF_CLK1_P/REFCLK1_N are buffered clocks from the same common source.

Figure 84: Aurora 70 pin connector duplex interface connection



Notes:

1. The Aurora port and target board should be able to independently assert PORESET_B and TRST_B to the processor in order to fully control the processor as shown here.
2. Populate this with a 1 kΩ resistor for short-circuit/current-limiting protection.
3. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the TRST_B line. If BSDL testing is not being performed, this switch should be closed to position B.
4. Asserting HRESET_B causes a hard reset on the device
5. This is an open-drain output gate.
6. REF_CLK_P/REF_CLK_N and REF_CLK1_P/REFCLK1_N are buffered clocks from the same common source.

4.5.3 Guidelines for high-speed interface termination

4.5.3.1 SerDes interface entirely unused

If the high-speed SerDes interface is not used at all, the unused pin should be terminated as described in this section.

Note that $S1V_{DD}$, $X1V_{DD}$ and AVDD_SD1_PLL1 must remain powered.

For AVDD_SD1_PLL1, it must be connected to $X1V_{DD}$ through a zero ohm resistor (instead of filter circuit shown in Figure 74).

The following pins must be left unconnected:

- SD1_TX[3:0]_P
- SD1_TX[3:0]_N
- SD1_IMP_CAL_RX
- SD1_IMP_CAL_TX

The following pins must be connected to S1GND:

- SD1_REF_CLK1_P, SD1_REF_CLK2_P
- SD1_REF_CLK1_N, SD1_REF_CLK2_N

It is recommended for the following pins to be connected to S1GND:

- SD1_RX[3:0]_P
- SD1_RX[3:0]_N

It is possible to disable SerDes module by disabling all PLLs associated with it.

SerDes is disabled as follows:

- SRDS_PLL_PD_S1 = 2'b11 (both PLLs configured as powered down, all data lanes selected by the protocols defined in SRDS_PRTCL_S1 associated to the PLLs are powered down as well)
- SRDS_PLL_REF_CLK_SEL_S1 = 2'b00
- SRDS_PRTCL_S1 = 2 (no other values permitted when both PLLs are powered down

4.5.3.2 SerDes interface partly unused

If only part of the high speed SerDes interface pins are used, the remaining high-speed serial I/O pins should be terminated as described in this section.

Note that both $S1V_{DD}$ and $X1V_{DD}$ must remain powered.

If any of the PLLs are un-used, the corresponding AVDD_SD1_PLL1 must be connected to $X1V_{DD}$ through a zero ohm resistor (instead of filter circuit shown in Figure 74).

The following unused pins must be left unconnected:

- SD1_TX[3:0]_P
- SD1_TX[3:0]_N

The following unused pins must be connected to S1GND:

- SD1_REF_CLK[1:2]_P, SD1_REF_CLK[1:2]_N (If entire SerDes unused)

It is recommended for the following unused pins to be connected to S1GND:

- SD1_RX[3:0]_P
- SD1_RX[3:0]_N

In the RCW configuration field SRDS_PLL_PD_S1, the respective bits for each unused PLL must be set to power it down. A module is disabled when both its PLLs are turned off.

Unused lanes must be powered down through the SRDSx Lane m General Control Register 0 (SRDSxLNmGCR0) as follows:

- SRDSxLNmGCR0[RRST] = 0
- SRDSxLNmGCR0[TRST] = 0
- SRDSxLNmGCR0[RX_PD] = 1
- SRDSxLNmGCR0[TX_PD] = 1

Note that in the case where the SerDes pins are connected to slots , it is acceptable to have these pins unterminated when unused.

4.5.4 USB controller connections

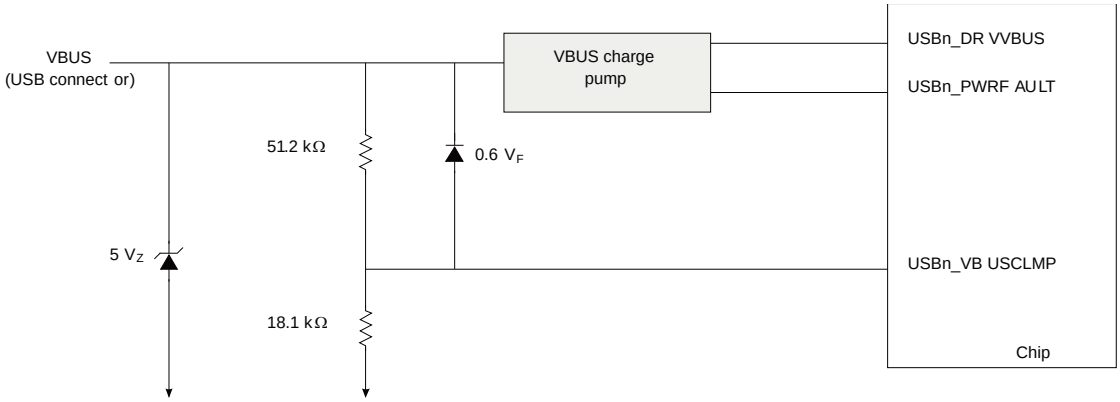
This section details the hardware connections required for the USB controllers.

4.5.4.1 USB divider network

This figure shows the required divider network for the VBUS interface for the chip. Additional requirements for the external components are:

- Both resistors require 1% accuracy and a current capability of up to 1 mA. They must both have the same temperature coefficient and accuracy.
- The zener diode must have a value of 5 V−5.25 V.
- The 0.6 V diode requires an IF = 10 mA, IR < 500 nA and VF(Max) = 0.8 V. If the USB PHY does not support OTG mode, this diode can be removed from the schematic or made a DNP component.

Figure 85: Divider network at VBUS



4.6 Thermal

This table shows the thermal characteristics for the chip. Note that these numbers are based on design estimates and are preliminary.

Table 150: Package thermal characteristics6

Rating	Board	Symbol	Value	Unit	Notes
Junction to ambient, natural convection	Single-layer board (1s)	$R_{\Theta JA}$	31	°C/W	1, 2
Junction to ambient, natural convection	Four-layer board (2s2p)	$R_{\Theta JA}$	22	°C/W	1, 3
Junction to ambient (at 200 ft./min.)	Single-layer board (1s)	$R_{\Theta JMA}$	24	°C/W	1, 2
Junction to ambient (at 200 ft./min.)	Four-layer board (2s2p)	$R_{\Theta JMA}$	18	°C/W	1, 2
Junction to board	-	$R_{\Theta JB}$	13	°C/W	3
Junction to case top	-	$R_{\Theta JCtop}$	<0.1	°C/W	4

Notes:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-3 and JESD51-6 with the board (JESD51-9) horizontal.
3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Junction-to-case-top at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
5. See Thermal management information, for additional details.

This table provides the thermal resistance with heat sink in open flow

Table 151: Thermal Resistance with Heat Sink in Open Flow

Heat Sink with Thermal Grease	Air Flow	Thermal Resistance(°C/ W)
53 x 53 x 25 mm Pin Fin	Natural Convection	7.1
	0.5 m/s	4.4
	1 m/s	3.4
	2 m/s	2.9
	4 m/s	2.6
35x31x23 mm Pin Fin	Natural Convection	9.3
	0.5 m/s	5.6
	1 m/s	4.7
	2 m/s	4.1
	4 m/s	3.6
30x30x9.4 mm Pin Fin	Natural Convection	13.4
	0.5 m/s	9.2
	1 m/s	7.2
	2 m/s	5.5
	4 m/s	4.5
43x41x16.5 mm Pin Fin	Natural Convection	9.6
	0.5 m/s	6.1
	1 m/s	4.8
	2 m/s	3.8
	4 m/s	3.3

Notes:

1. Simulations with heat sinks were done with the package mounted on the 2s2p thermal test board. The thermal interface material was a typical thermal grease such as Dow Corning 340 or Wakefield 120 grease.

2. Simulation details:

   - Substrate metal thicknesses: 0.015, 0.025 mm
   - Substrate core thickness: 0.4 mm

4.7 Recommended thermal model

Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local TELEDYNE E2V sales office.

4.8 Temperature diode

The chip has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461A). These devices feature series resistance cancellation using 3 current measurements, where up to 1.5kΩ of resistance can be automatically cancelled from the temperature result, allowing noise filtering and a more accurate reading.

The following are the specifications of the chip's on-board temperature diode:

Operating range: 10 – 230 µA

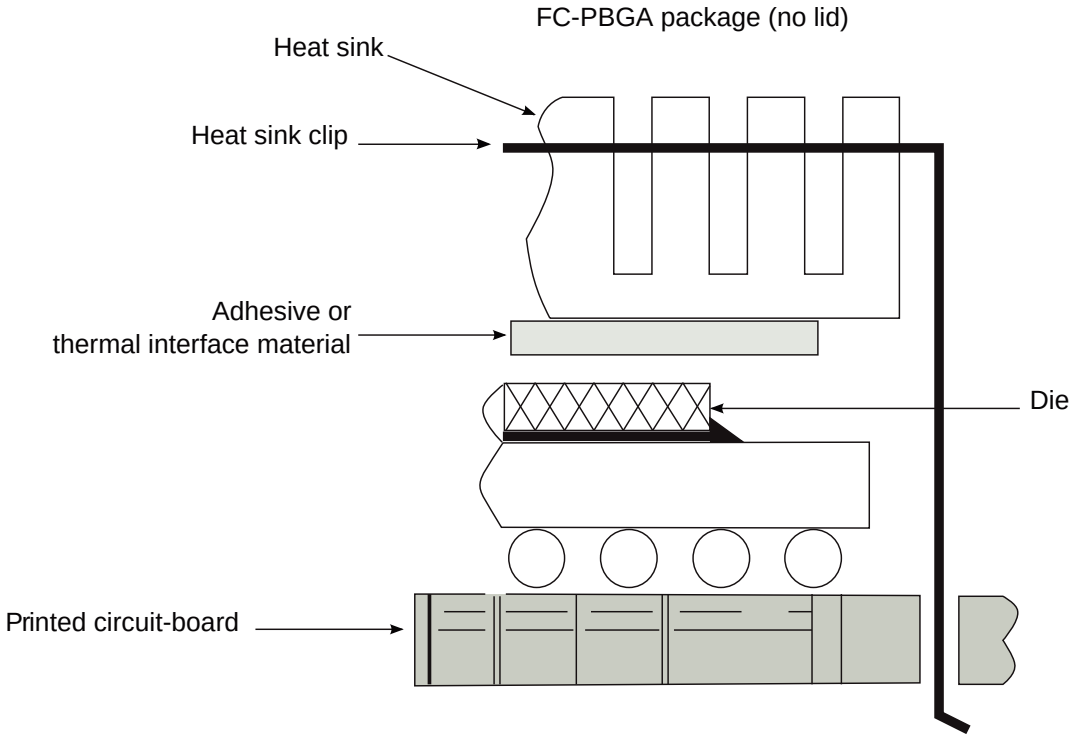
Ideality factor over 13.5 - 220 µA; Temperature range 80°C - 105°C: n = 1.004 ± 0.008

4.9 Thermal management information

This section provides thermal management information for the flip-chip, plastic-ball, grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design-the heat sink, airflow, and thermal interface material.

The recommended attachment method to the heat sink is illustrated in Figure 86: Package exploded, cross-sectional view-FC-PBGA (no lid). The heat sink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 15 pounds force (65 Newton).

Figure 86: Package exploded, cross-sectional view-FC-PBGA (no lid)



The system board designer can choose between several types of heat sinks to place on the device. There are several commercially-available thermal interfaces to choose from in the industry. Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

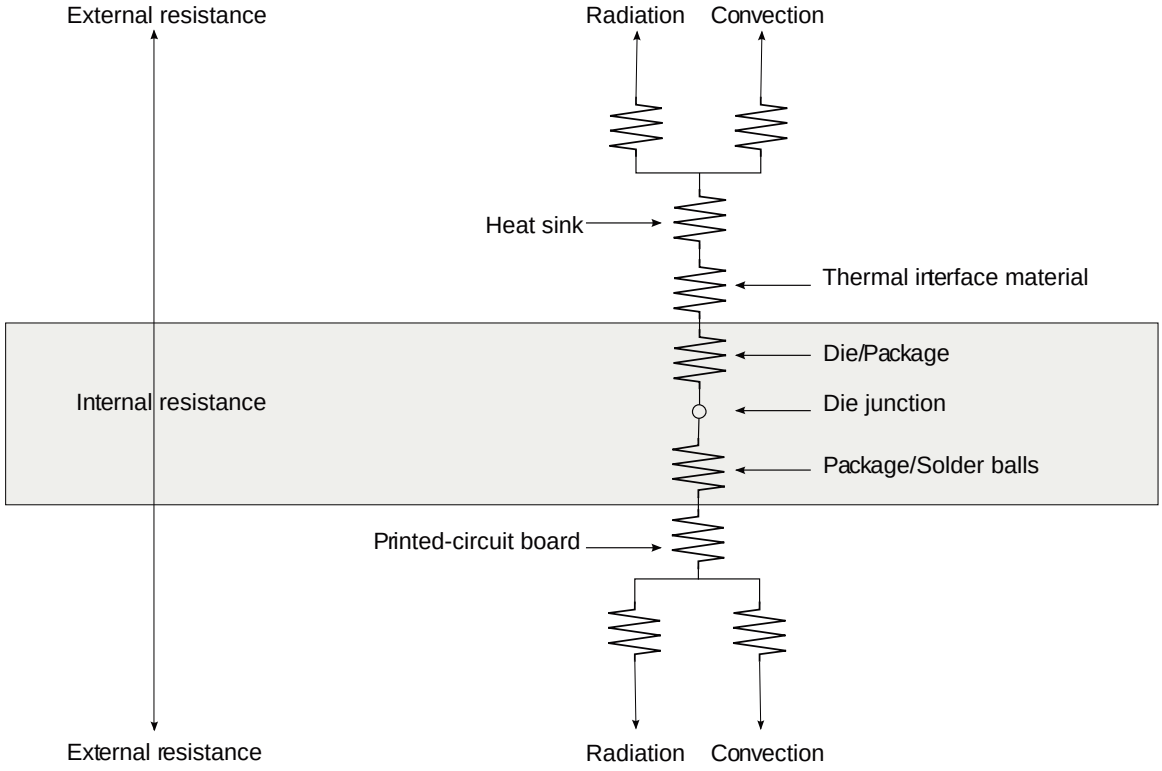
4.9.1 Internal package conduction resistance

For the package, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

This figure depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

Figure 87: Package with heat sink mounted to a printed-circuit board



(Note the internal versus external package resistance)

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

4.9.2 Thermal interface materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. The performance of thermal interface materials improves with increasing contact pressure; this performance characteristic chart is generally provided by the thermal interface vendor. The recommended method of mounting heat sinks on the package is by means of a spring clip attachment to the printed-circuit board (see Figure 86).

The system board designer can choose among several types of commercially-available thermal interface materials.

5 PACKAGE INFORMATION

5.1 Package parameters for the FC-PBGA

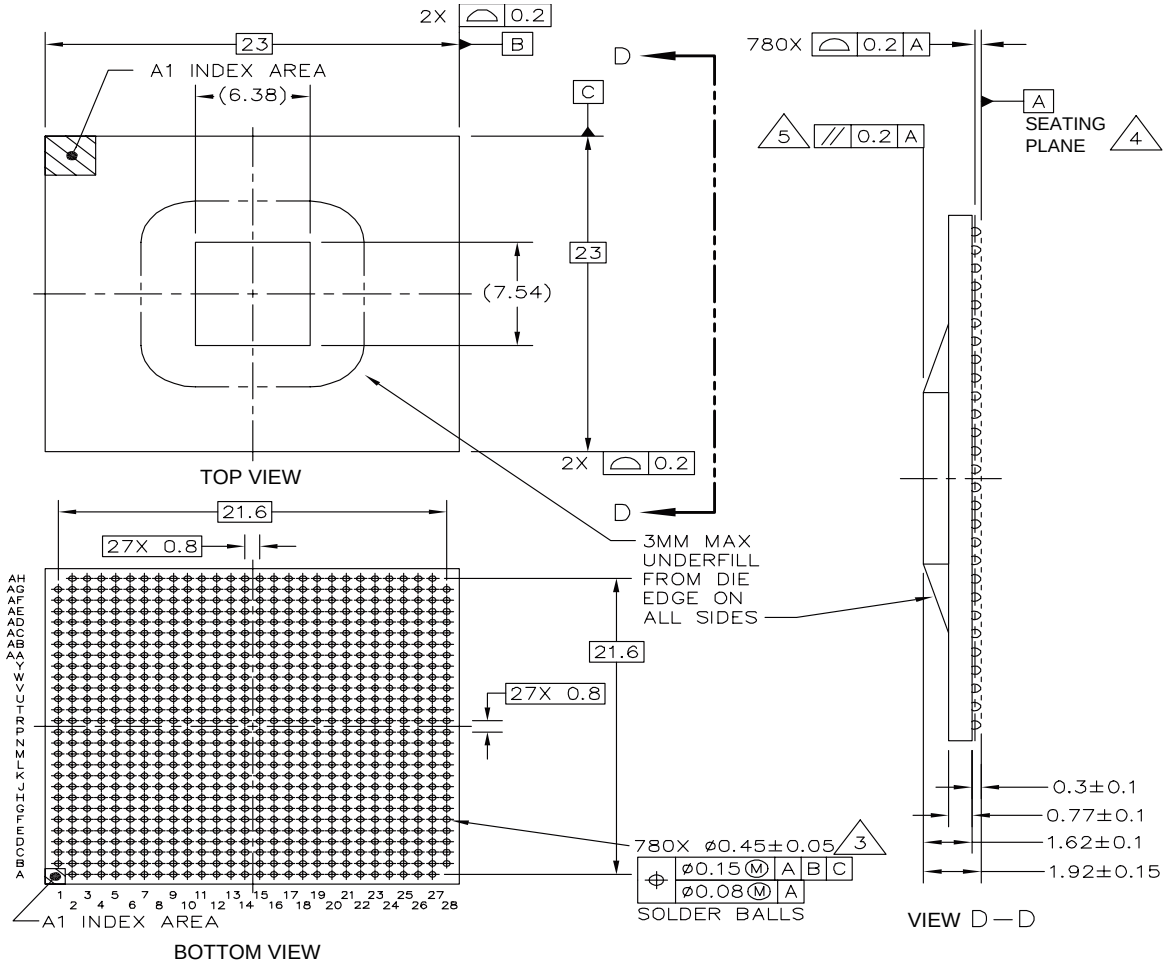
The package parameters are as provided in the following list. The package type is 23 mm x 23 mm, 780 flip-chip, plastic-ball, grid array (FC-PBGA).

- Package outline - 23 mm x 23 mm
- Interconnects - 780
- Ball Pitch - 0.8 mm
- Ball Diameter (typical) - 0.45 mm
- Solder Balls:
- 96.5% Sn, 3% Ag, 0.5% Cu
- 63% Sn, 37% Pb
- Module height - 1.77 mm (minimum), 1.92 mm (typical), 2.07 mm (maximum)

5.2 Mechanical dimensions of the FC-PBGA

This figure shows the mechanical dimensions and bottom surface nomenclature of the chip.

Figure 88: Mechanical dimensions of the FC-PBGA



Notes:

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.

6 SECURITY FUSE PROCESSOR

This chip implements the QorIQ platform's Trust Architecture, supporting capabilities such as secure boot. Use of the Trust Architecture features is dependent on programming fuses in the Security Fuse Processor (SFP). The details of the Trust Architecture and SFP can be found in the chip reference manual.

To program SFP fuses, the user is required to supply 1.8 V to the PROG_SFP pin per Power sequencing. PROG_SFP should only be powered for the duration of the fuse programming cycle, with a per device limit of two fuse programming cycles. All other times PROG_SFP should be connected to GND. The sequencing requirements for raising and lowering PROG_SFP are shown in Figure 10. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Table 4.

NOTE
Users not implementing the QorIQ platform's Trust Architecture features should connect PROG_SFP to GND.

7 ORDERING INFORMATION

Contact your local TELEDYNE E2V sales office or regional marketing team for order information.

This table provides the TELEDYNE E2V QorIQ platform part numbering nomenclature.

Table 152: Ordering information

pt or t	n	nn	n	t	e	n	c	d	r
Generation	Platform	Number of virual cores	Derivatives	Temperature range	Encryption	Package Type	CPU Speed	DDR Data Rate	Product Revision
T(X) = 28 nm	1	02 = 2 cores 01 = 1 core	4 = First product	A = -40/105 F = -40/125 M = -55/125	E = SEC present N = SEC not present	3 = FCPBGA C4 Pb-free/C5 Leaded 7 = FCPBGA C4/C5 Pbfree	K = 1000 MHz M = 1200 MHz P = 1400 MHz	N= 1300 MT/s Q= 1600 MT/s	A = Rev 1.0

8 REVISION HISTORY

This table summarizes revisions to this document.

Issue	Date	Comments
C	May 2020	Removal of Preliminary
B	July 2018	Updated temperature range in Table 153: “Ordering information: . removed V = -40/110 . added A = -40/105 and F = -40/125 Updated Junction temperature in Table 9: “T1024 core power dissipation” and Table 10: “T1014 core power dissipation: . replaced 110 by 105 . updated Power (W) Updated Operating temperature range in Table 4: "Recommended operating conditions” . replaced V range by A range . added F range
A	March 2018	Initial revision

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