Ultra-Low Dark Signal in the AIMO CCD230-84

Ian Moody, Ray Bell, Marc Watkins

Abstract

CCDs are ideal for very low light imaging applications, such as astronomy, clinical diagnostic testing, and bioluminescence. The compatibility of the CCD with very long integration times, and facility for noiseless on-chip charge binning, makes it a very sensitive imager. It remains very competitive for certain applications compared to low light CMOS imagers, since these have higher dark signal and on-chip dissipation, and rely on frame averaging, which is not as efficient as charge binning.

e2v inverted mode (AIMO) CCDs can achieve extremely low dark signal at Peltier temperatures. This paper describes a study of 15 off AIMO CCD230-84s, exploring the limits of dark signal performance, under improved operating conditions, at temperatures down to -80°C. Housekeeping, and optimisation routines were developed, and limiting factors discovered.

For the AIMO devices tested under special conditions, extremely low dark signals down to 1e/pixel PER HOUR were obtained at temperatures in the region of -75°C. By comparison, NIMO CCDs require cooling to -120°C to reach similar low levels of dark signal. The back-thinned devices studied had a range in dark signal between 0.5 e/pix/hour and 2.5 e/pix/hour at -75°C. Front-face devices had a range between 5 e/pix/hour and 21 e/pix/hour at -68°C.

For the range -25°C to -65°C, it was found that the log equation fitting the measured dark signal to temperature had a gradient close to that for depletion dark signal, as in a NIMO device. This is a shallower gradient than in the AIMO equation often cited, including in some Teledyne e2v datasheets, which applies for temperatures from -25°C to 20°C.

1. Introduction

Apart from the highest QE from back-thinning, and readout noise as low as 2e (even lower with EMCCDs), some of the main advantages of the CCD for low light imaging are its exceptionally low dark signal and its ability to noiselessly combine, or 'bin' charge from several pixels prior to readout. Binning works well with large image area CCDs, such as the CCD230-84, with its 60mm square image area and 16M pixels.

At low signal levels, with low dark signal, signal to noise ratio increases linearly with integration time. Furthermore, one long exposure is better than many short exposures to reduce the contribution from readout noise. One 9 second exposure image has 3x the SNR of 9 off 1 second images averaged together, since the SNR after adding multiple exposures increases by the square root of the number of exposures. CCD binning increases the signal without adding noise, the only trade-off being the reduction in spatial resolution.

Dark current describes the rate of generation of thermal electrons at a given CCD temperature. This can be reduced by operating the CCD in inverted or multi-phase-pinned mode. This draws holes to the CCD surface, and these suppress the generation of dark signal electrons from surface discontinuities in the CCD lattice. Since the surface dark signal is much higher than other sources in the bulk and depletion layers, this is very effective.

With Teledyne e2v technology, very low image area dark signal is further preserved by virtually zero contributions from other sources, such as junction and transistor leakages, or on-chip light emission. This makes the CCD compatible with very long integration times of the order of several hours. This imaging mode is mostly associated with astronomical applications, where very low dark signal is usually achieved by liquid nitrogen or cryogenic cooling. This paper shows that many other high-performance low light imaging systems can benefit from reduced dark signal without such strong cooling, by using an AIMO CCD with Peltier cooling.

2. Theoretical Sources of Dark Signal

There are three main areas that contribute to the dark signal:

- Undepleted silicon beneath the potential well and channel stop
- Depleted silicon within the potential wells
- Si-SiO_2 surface interface

Dark current carriers are generated through energy levels (traps) that are introduced into the forbidden band gap by imperfections or impurities within the Si or at the interface. Electron and hole emissions are required nearly simultaneously through the trap state to generate dark charge. The emission of a hole is the transition of an electron from the valence band to the trap state leaving a hole and the emission of the electron is the transition of an electron from the trap state to the conduction band. Once in the conduction band, the electron can be collected by the potential well as dark signal, while the hole that is made leaves via the substrate.

The Si/SiO_2 interface has traps due to the mismatch between the two materials producing “dangling bonds”. The trap energies are distributed throughout the forbidden band gap, although it is the mid-band states that contribute the most to the dark signal. However, this surface dark current can be virtually eliminated by inverting the surface by having the clock low bias significantly lower than the substrate bias. The inversion layer produces a hole population at the surface that occupy the interface trap states and thereby inhibit the emission of electrons to the conduction band. This significantly reduces the surface dark current below the dark current produced in the depletion region and the undepleted silicon. The dark current produced in the undepleted region is known as diffusion dark current. This is because any electrons generated have to diffuse into the electric field generated by the potential well before being collected as dark signal.

The process of generation/recombination is theoretically described by the Shockley/Hall/Read equation:-

$$U = \frac{N_t \sigma v \left(np - n_i^2\right)}{n + p + 2n_i \cosh\left(\frac{E_t - E_i}{kT}\right)}$$

U : net recombination rate
N_t : concentration of traps at energy level E_t
E_i : intrinsic Fermi level
σ : capture cross sections for electrons and holes
v : thermal velocity of the carriers
n : electron concentration
p : hole concentration
n_i : intrinsic carrier concentration

2.1 Depletion Dark Current

The depletion layer is swept of electrons and holes, and so $n = p = 0$. The majority of dark current is caused by mid-band traps, which have an energy equal to the intrinsic Fermi level ($E_t = E_i$). The Shockley/Hall/Read equation can be simplified to

Depletion dark current $\propto e^{-E_g/2kT}$

where E_g is the silicon band gap level

2.2 Diffusion (Undepleted Silicon) Dark Current

It can be assumed that $p \gg n$, $p = N_A$ and $n_i^2 \gg pn$. Again assume the trap states are mid-band. The equation can therefore be simplified to:-

Diffusion Dark Current $\propto e^{-E_g/kT}$

2.3 Dark Signal Equations

Graph of Ln (Dark Current) versus 1/T
The Depletion and Diffusion dark current equations can be represented as a straight line by applying the natural log to both sides:-

$$\mathrm{Ln(Dark\ Current)} \cong c - m(1/T)$$

The gradient of the line m should be $E_g/2k$ for Depletion dark current and E_g/k for Diffusion current. Assuming the band gap of silicon is 1.12 eV and the Boltzmann constant, k, is 8.62×10^{-5} eV/K, this equates to a gradient of 6497 for depletion dark current and 12993 for diffusion dark current.

NIMO Datasheet Dark Signal Equation

$$Qd/Qd_0 = 122T^3e^{-6400/T}$$

where Qd_o is the dark current at 20°C

The dark signal is tested at -100°C (CCD231-84). The equation is validated to predict the dark signal of Teledyne e2v CCDs between -120°C and 20°C

IMO Datasheet Dark Signal Equation

$$Qd/Qd_o = 1.4E{+}6\ T^3e^{-9080/T}$$

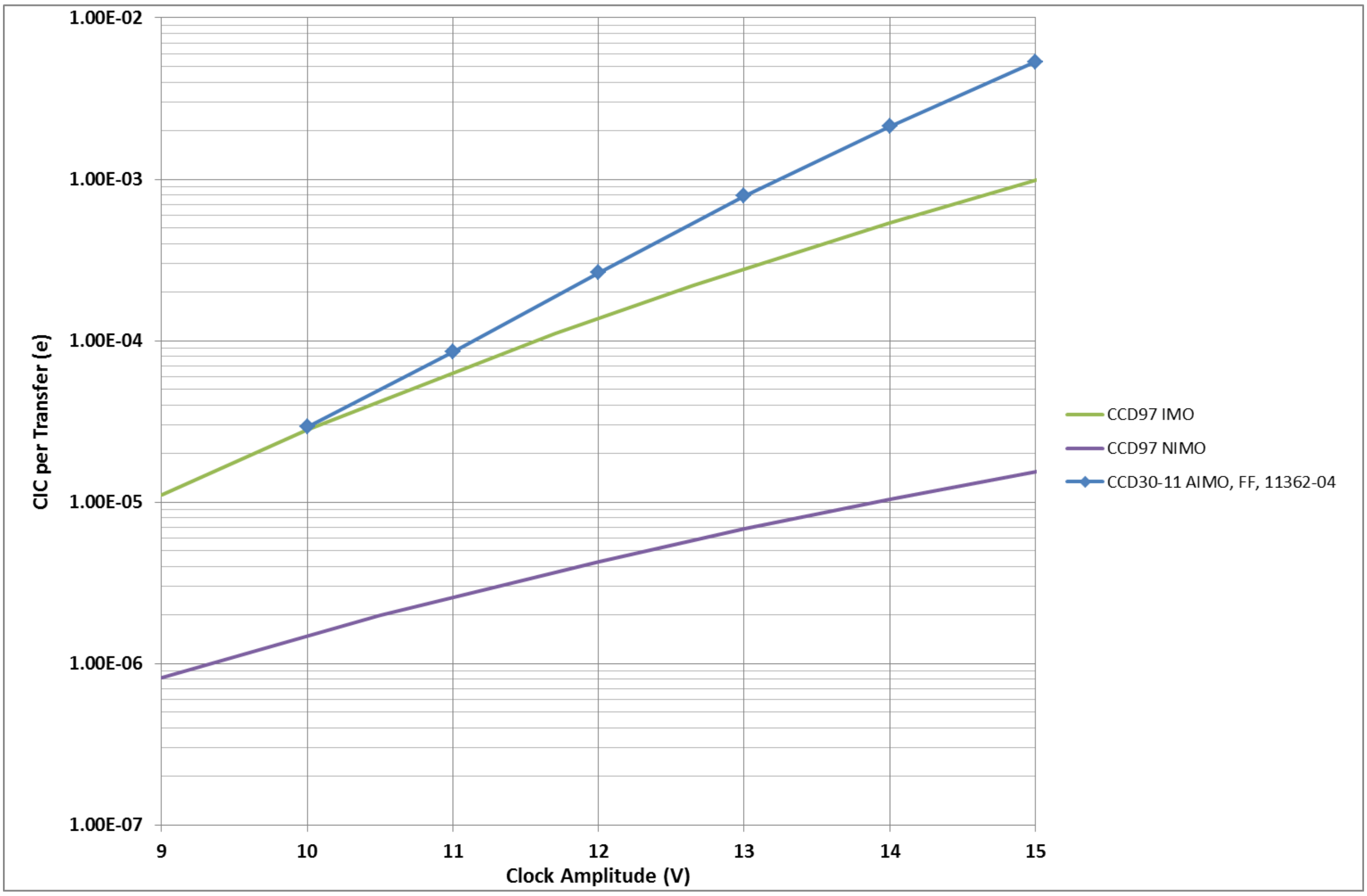
where Qd_o is the dark current at 20°C

The dark signal is tested between -25°C and 0°C. The equation is validated to predict the dark signal of Teledyne e2v CCDs between -25°C and 20°C. It can be seen that the temperature range for which the equation is validated is much smaller for AIMO than for NIMO. This study set out to explore the dark signal for the AIMO CCD230-84 between -25°C and -80°C.

3. Clock-Induced Charge

Clock-induced charge (CIC) is spurious signal generated when transferring signal charge through the device. It contributes an amount to the total dark signal, independent of the integration time and the temperature. The amount of CIC generated depends on a number of factors, most significantly the clock amplitude used, and whether the device operates in inverted or non-inverted mode. Secondary factors include clock frequency and edge speed. The component of CIC generated by the parallel transfers of the AIMO device is the most significant. A smaller amount of CIC is generated by serial transfers in the readout register, as this has a much higher clock frequency.

Graph of Clock Induced Charge versus Clock Amplitude



The curve above is based on CIC data from CCD97 and CCD30-11 tests. Although there are different gradients, both data sets indicate ~ 3.0E-5 e/transfer at 10V clock amplitude. Extrapolating the CCD30-11 data gives a similar value to the CCD97 at 9V of ~ 1.0E-5 e/transfer. The higher values from the CCD30-11 are taken above 10V.

The CIC values in the curve are the number of electrons generated per pixel per parallel transfer. Since the CIC scales linearly with the total number of parallel transfers, the total number of electrons generated per pixel per frame is given by multiplying the CIC by the total number of parallel transfers. In the case of the CCD230-84 in a normal imaging mode, the CIC results from 4096 parallel transfers. Some of these transfers occur during clearing the pixel prior to integration and some during readout of the pixel.

The CIC has an exponential dependence on the clock high to substrate bias, and so can be reduced by reducing the clock amplitude. Using the minimum practical image clock amplitude is important in achieving low CIC, but it is also important to check that full well and CTE are maintained. We preceded all dark signal tests by a functional image test. It was found that the CCD230-84 samples tested had good transfer at 9.0V to 9.5V clock amplitude.

The variation of total transfer generated signal with clock amplitude is thus expected to be:-
12V 0.82 e/pix/frame
11V 0.30 e/pix/frame
10V 0.12e/pix/frame
9V 0.04e/pix/frame
This is per real image pixel, not per dark signal image binned pixel. The lowest dark signal values measured were ~1e /pix / hour to ~3e /pix / hour, measured with a 10 minute integration time. Hence the signal levels were 0.17 to 0.50 e/pixel. It can be clearly seen that reduced image clock amplitude is important in achieving ultra-low dark signal values.

The CIC is in any case eliminated in the analysis routine, when the zero image is subtracted from the long integration time image. Since it was possible that the pre-flush for the zero frame was not exactly the same as for the dark frame, we checked that CIC was exactly subtracted by this routine see Optimisation Aspects below.

4. The Challenges of Measuring Ultra Low Dark Current

The Teledyne e2v standard production dark signal test of NIMO large area devices such as the CCD231-84 is currently at -100°C. The dark signal test of AIMO large area devices such as the CCD230-84 is at -25°C. This higher test temperature has been adequate for most customers' needs, since the dark signal for AIMO devices is already low at -25°C. It will also become clear below that testing lower dark signal at lower temperature adds considerable test time, and therefore cost.

This study set out to explore the limits of the CCD230-84 device, and its test equipment, to investigate how well the AIMO dark signal continued to reduce at temperatures lower than -25°C.

4.1 Practical and Housekeeping Aspects

- Integration times much longer than routine dark signal production test are needed, to collect enough dark signal to measure above the readout noise.
- Higher charge binning ratios than routine dark signal production test are needed, e.g. 128x instead of 16x.
- Cooling the device from room temperature to -80°C takes much longer than cooling it to -25°C, as in routine production test
- Warming the device from -80°C to room temperature takes much longer than warming it from -25°C
- Although the maximum rate of heating or cooling is 5°C /min, e2v test cameras aim for a more typical 1°C /min. Hence the combined time to cool and warm a device from room temperature to -80°C and back, is over 3 hours.
- To achieve lower temperatures down to -80°C, extra care is needed to ensure good thermal contact of the CCD with the test system cooling plate.
- Temperature sensors must be used to monitor the exact CCD temperature. The CCD230-84 has 2 off integral thermistors. Since these are only calibrated down to -55°C, the platinum resistance thermometer reading of the cooling plate can be taken into account, and extrapolation of the curve fitted can be used below -55°C.
- Light leakage through connectors and ports must be carefully shielded
- Leakage from Fe55 calibration sources must be eliminated

4.2 Optimisation Aspects

Having taken care of the above 'housekeeping' aspects, further optimisations need to be carried out:-

- The device must be checked to ensure it is fully inverted, or 'pinned'. Just setting a typical, or predicted, substrate voltage will not be enough to ensure that the surface dark signal is fully suppressed. In practice, most devices were fully pinned at Vss= 9.5V.
- The image area clock induced charge must be reduced to a low level, negligible except at the lowest temperatures, by reducing the image clock amplitude below typical, whilst ensuring that transfer of peak charge is still maintained. In practice, most devices gave full charge transfer at >= 9.0V clock amplitude.
- Trapped charge must be avoided. Biasing and clocking should be in operation at room temperature, before cooling the device down. Biasing and clocking should not be interrupted at any time with the device cold, since 'power-cycling trapped charge' may result. Several measurements of dark signal should be made at each temperature over a 30 minute period, to check for trapped charge emission, which reduces over time.

4.3 Estimation of Errors

4.3.1 Random Errors

Temperature Uncertainty

The most significant component of random error is due to temperature uncertainty. This is caused by both the Eurotherm control instability within the integration time, and the model fit below -50°C, when out of range of the thermistors incorporated in the CCD package. The theoretical depletion dark signal equation can be used to convert temperature uncertainty to electrons/pix/sec.

For the range -50°C to -30°C coldplate settings, the two on-device thermistors give a good reading of the device temperature, and the fit from the solver for the offset between the device and the coldplate can be well established. For -69C and -80C coldplate settings, when the thermistor reading is unavailable, we need to rely on the offset fit from the solver, and it may deviate from the linear progression of the offset from the coldplate at lower temperatures

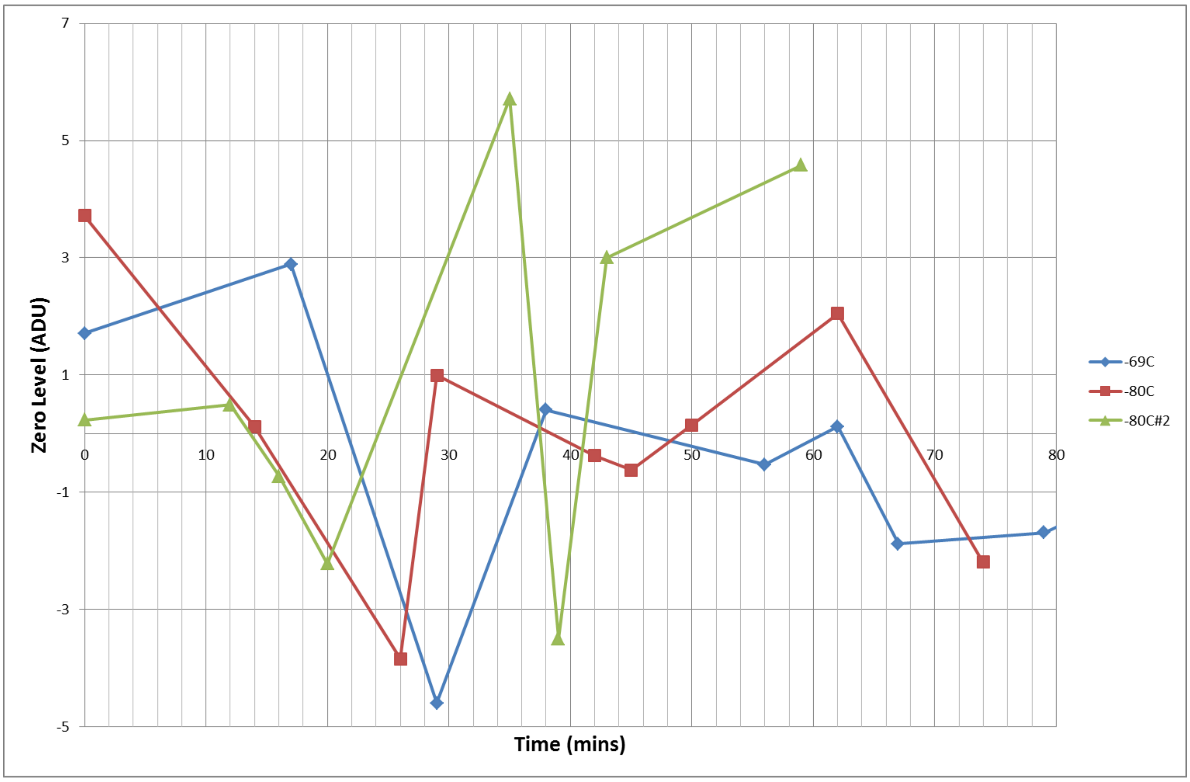
Coldplate (°C)	Eurotherm instability (+/-)	Fit to curve for temp cal below -50°C	Combined	+ve error bar in dark signal	-ve error bar in dark signal
-36	1	0	1.0	11%	-11%
-47	1	0	1.0	12%	-12%
-58	1	1	1.4	13%	-13%
-68	1	1.5	1.8	37%	-28%
-80	1	2	2.2	69%	-30%

Stability of Zero Image

The stability of the average level of the zero image is essential, since the zero image is subtracted from the extended integration time image in order to obtain the dark signal. Since repeated zero images were taken, the stability over time can be obtained. The worst deviation over a one hour period was 5.7 ADU. This can be approximated to 3 sigma, and so sigma is 1.9 ADU or 1.5e (calibration is ~ 0.8e /ADU).

The typical binned dark signal at any temperature was 60 ADU, giving a typical error of 3.2%, with a measurement cycle time of 20 mins. The worst case binned dark signal (lowest reading) at -75C was 15 ADU: an error of 13%.

Graph of Black Level of Zero Image versus Time



Coldplate (°C)	Typ binned dark signal (ADU)	Typical binned dark signal (e)	+ve error bar in dark signal	-ve error bar in dark signal	Comments
-36	50	40	4%	4%	shorter integ. & 16x binning
-47	50	40	4%	4%	shorter integ. & 16x binning
-58	100	80	2%	2%	128x binning
-68	30	24	6%	6%	128x binning
-80	15	12	13%	13%	128x binning

Random and Quantisation Noise

The error in reading the integrated and binned dark signal originates from output circuit noise, dark signal shot noise and quantisation error. The output circuit noise is averaged due to the large number of pixels analysed in the region of interest: approximately 600,000 for 16x binning and 75,000 for 128x binning. The signal is increased by the integration time chosen (up to 600s) and the binning ratio (16x or 128x). For lower dark signals such as 3 e/pix/hour with 128x binning, 600s integration, and output circuit noise and dark signal shot noise each in the region of 9e, the total error from the centre value was calculated as 0.3%.

Total Random Error

Combining the two most significant error sources: temperature uncertainty and stability of the zero image, gives the total random error used in the error bars on the graphs:-

T (°C)	+ve error bar	-ve error bar
-36	12%	12%
-47	13%	13%
-58	14%	14%
-68	38%	28%
-80	70%	33%

4.3.2 Systematic Errors

Systematic errors are important, since they may lead to a dark signal floor at the lowest readings. These errors are expected to be :-

1. Temperature error: offset between device and the coldplate. This has been taken account of in the random error analysis, and the fit to a modelled curve. However, if the thermal contact between the device and the coldplate has a systematic behaviour below -50C, this may go un-noticed in the results graph.
2. Clocked induced charge: CIC. This is subtracted out. See Subtraction of CIC below.
3. Trapped charge – the re-emission of trapped charge is indistinguishable from dark signal, but it can be identified due to its reduction over time. See Limiting Factors below.
4. Light leakage into the camera. If the exclusion of stray light into critical areas such as the feedthroughs was less than perfect, excess dark signal could have resulted. Black cloth was used but more than one layer of clean room black cloth was needed.

Check of Subtraction of CIC

At the lower temperatures, pairs of zero and dark images were taken before and after the main pair of zero and long integration dark images. The additional zero and dark pairs had zero integration time for the dark frame, i.e. the 'zero.fit' and 'dark.fit' for the extra zero images both had zero integration time. If, when compared in level, they are found to have the same level, this would prove that the dark.fit image had the same pre-flush & readout as the zero.fit image. The method used for the comparison was:-

- Add numeric value 1000 to image dark.fit
- Subtract image zero.fit from image dark.fit
- Use Analyse / Measure to obtain the mean level for the resulting image
- If dark.fit has exactly the same average level as zero.fit, the mean will be 1000

15193-06-01 at -80°C

		Mean Level: dark.fit minus zero.fit
Set 1	Pair 1	996.941
	Pair 3	999.728
Set 2	Pair 1	1001.305
	Pair 3	1001.595
Set 3	Pair 1	1001.015
	Pair 3	1000.488
Combined Mean		1000.83

15431-22-01 at -80°C

		Mean Level: dark.fit minus zero.fit
Set 1	Pair 1	1003.278
	Pair 3	1000.325
Set 2	Pair 1	999.408
	Pair 3	1001.462
Set 3	Pair 1	1001.8
	Pair 3	1000.462
Combined Mean		1000.69

The data indicates that the zero integration time dark image had a level 0.69 ADU higher than the zero image, but since the typical level of the long integration time image was 60 ADU, this difference is negligible.

4.4 Limiting Factors

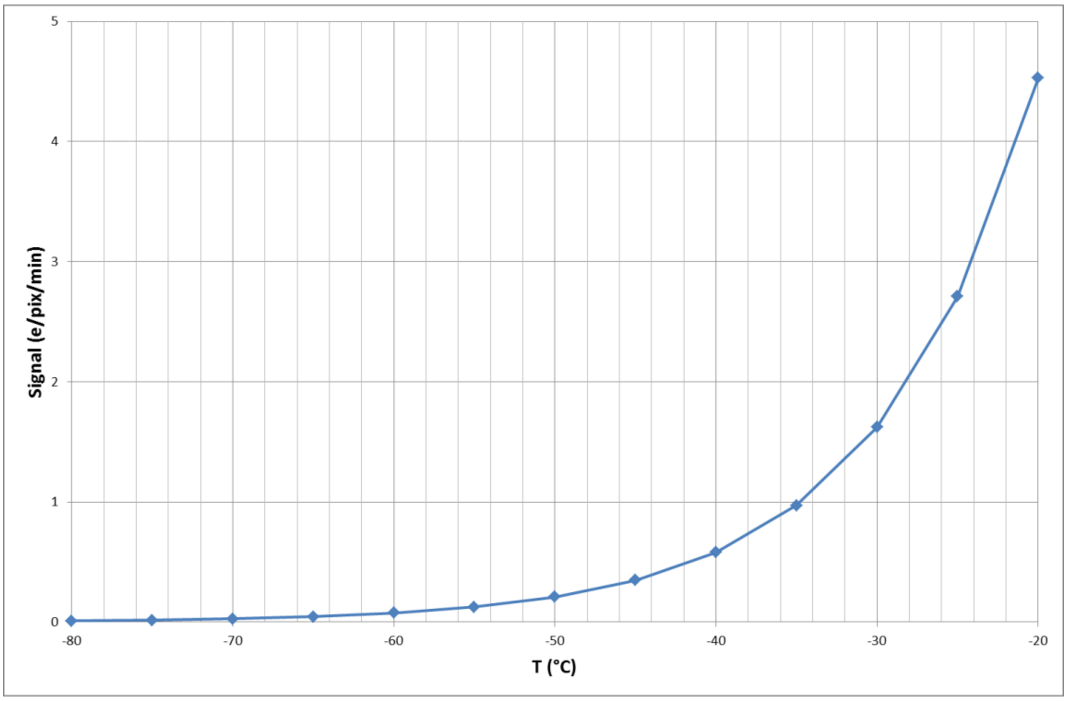
Having taken care of the housekeeping and optimisation aspects, and having estimated measurement errors, we can then see the remaining factors which limit ultra-low dark signal performance. These factors include very small amounts of trapped charge, and light leakage into the camera.

4.4.1 Trapped Charge

Trapped charge can be caused by over-saturating the CCD with light and causing excess signal charge to come in contact with surface states. For imaging at the very lowest light levels in typical applications like astronomy and bioluminescence, such light levels should not be encountered. It seems reasonable to separate high signal mode from low light mode. Simple precautions can be observed when changing from high signal to low light mode, such as warming the CCD to -20°C, to reset the trapped charge, before cooling down again and operating in low light mode.

When in low light mode, there are still bulk traps, but if the device is cold enough, the release rate from these is very low. Previous measurements show the emission of trapped charge immediately following exposure to a light level of ~2500 electrons per pixel is expected to produce only 1 e/pix/hour trap signal at -80°C. This low level signal produces a slightly elevated black level, which decays away over several hours.

Trap Emission at Time t=0, versus Temperature



Integration times for the study were 10 minutes for all tests below -50°C and consecutive images were 20min apart, after also capturing zero images. Dark signal readings at ~ -60°C and ~ -70°C were taken three times at each temperature. These readings allowed the trend over a 40 min period to be examined. A reducing trend in dark signal value in consecutive images at the same temperature can be used to check for the release of trapped charge. In fact, only device 15193-03-01 showed this behaviour, at a single temperature of -80°C coldplate. All other results showed low standard deviation for three readings at the same temperature, indicating that these dark signal results were accurate, in the sense of low trapped charge. Front-face devices, from older batches, consistently showed higher signal, but this was not accompanied by a reducing trend in dark signal value in consecutive images at the same temperature.

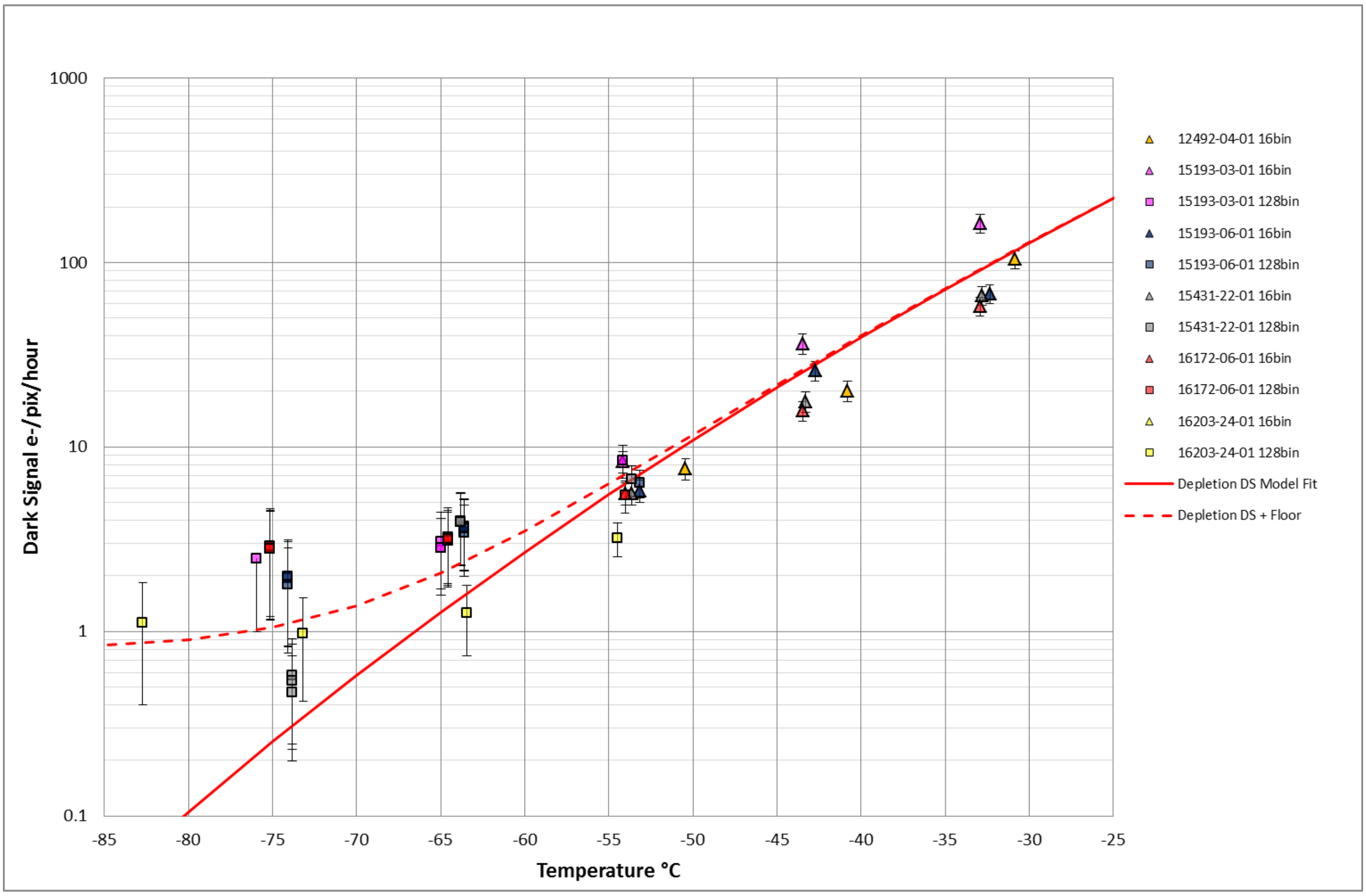
4.4.2 Power Cycling With the Device Cold

The most significant cause of trapped charge noted during the study was relatively un-expected. There were several instances of a poorly recognised effect, whereby charge was trapped if the device was cold and the power was cycled. Once trapped, there was a release time of one or two hours at -40°C, giving a falsely high dark signal reading. The solution was simply to ensure that biasing and clocking was in operation, before cooling the device down. Any remaining accidental occurrences of 'power-cycling trapped charge' could be detected as an isolated deviation of a point from the expected curve of dark signal. As such, these data points could be rejected in the same way as measured values with Fe55 or light leakage were rejected.

5. Results

5.1 Back-Thinned CCDs

Graph of Dark Signal versus Temperature (Back-Thinned CCDs)



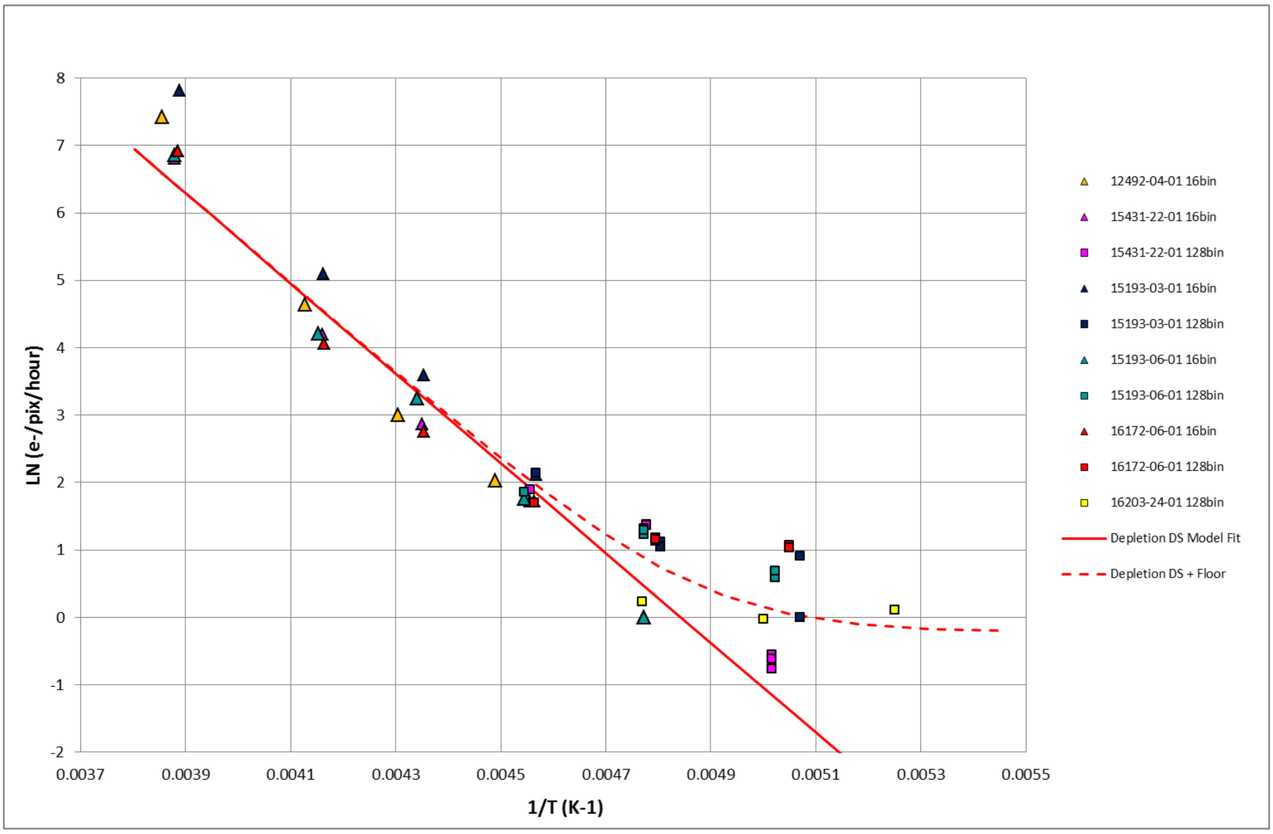
Comments on Fit to the Curve

15193-03-01 (pink/purple triangles and squares) is an example of a device with dark signal above the curve all the way from -33°C to -75°C, for both 16x and 128x binning, i.e. this is a device with high dark signal. The DS is 2.5 e/pix/hr at -75°C.

16203-24-01 (yellow squares) is an example of a device with dark signal below the curve all the way from -54°C to -83°C, for both 16x and 128x binning, i.e. this is a device with low dark signal. The DS is 1 e/pix/hr at -83°C.

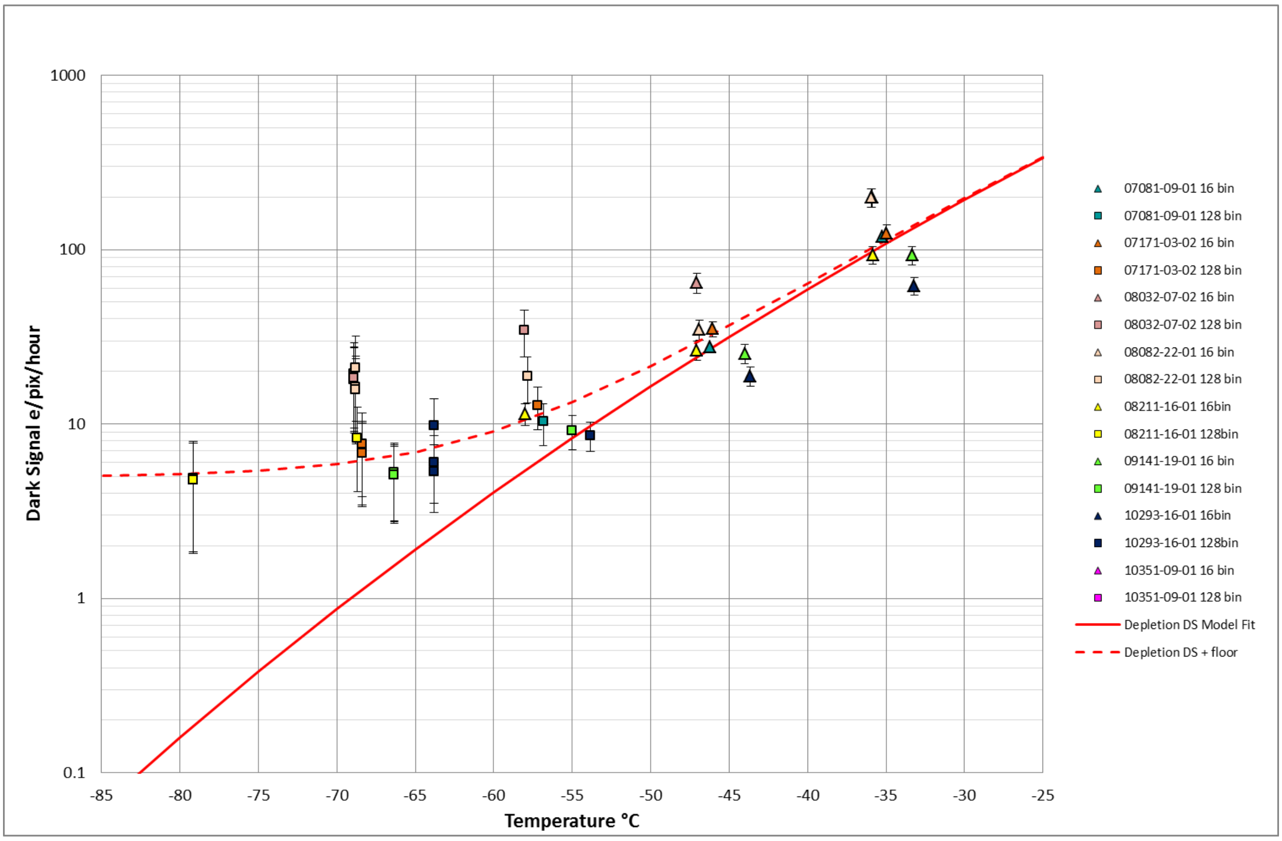
16172-06-01 (red triangles and squares) starts off at higher temperatures (16x bin) with dark signal below the curve, but then it is above the curve at -65°C and -75°C. The difference may be due to changes in limiting factors such as trapped charge and light leakage.

Graph of LN Dark Signal versus 1/T (Back-Thinned CCDs)



5.2 Front-Face CCDs

Graph of Dark Signal versus Temperature (Front-Face CCDs)

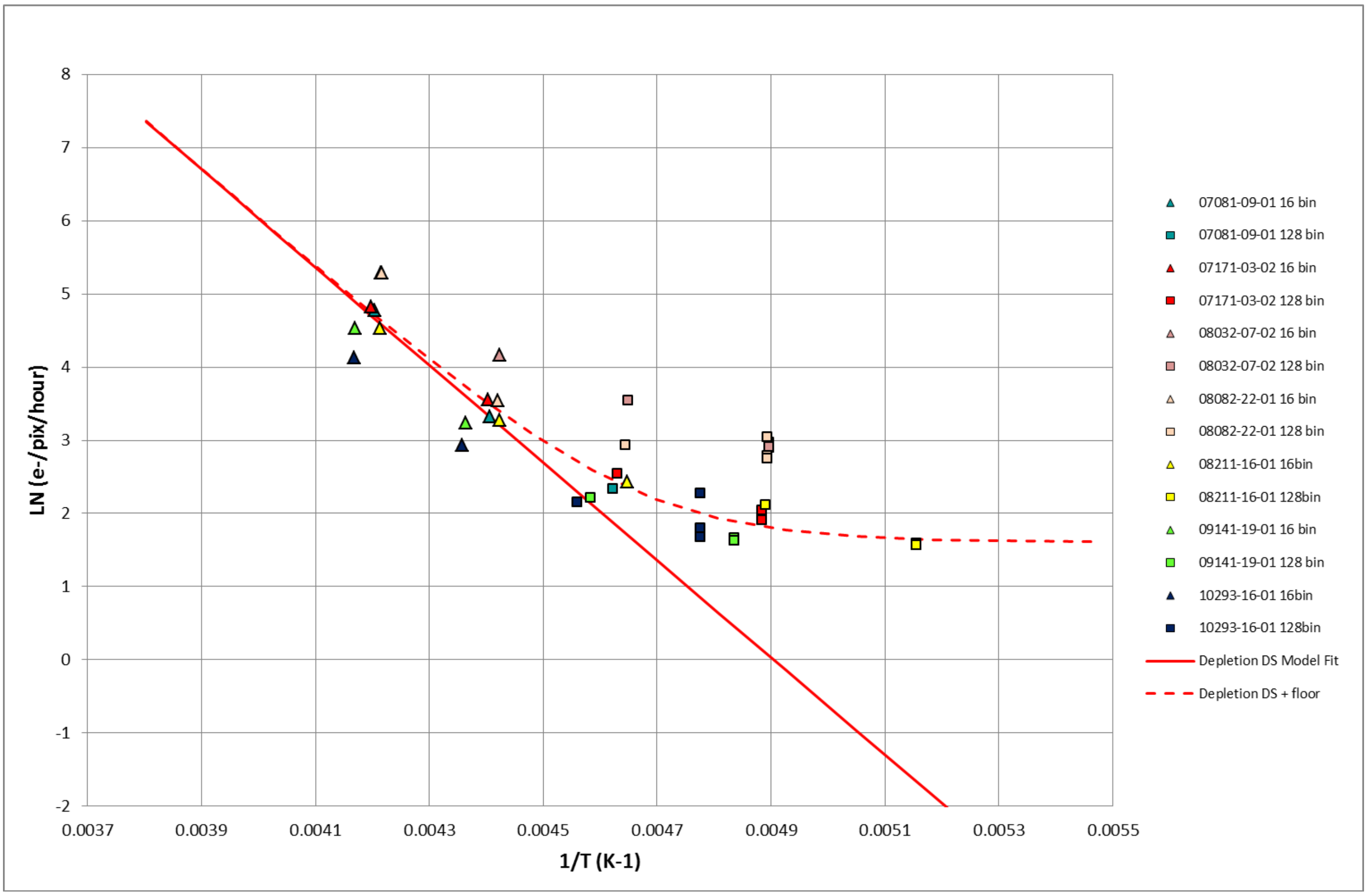


Comments on Fit to the Curve

08082-22-01 (pink triangles and squares) shows a device with dark signal consistently above the curve from -35°C to -69°C, for both 16x and 128x binning, i.e. this is a device with high dark signal: 21 e/pix/hr at -69°C.

09141-19-01 (green triangles and squares) shows a device with dark signal consistently below the curve from -33°C to -67°C, for both 16x and 128x binning, i.e. this is a device with low dark signal: 5 e/pix/hr at -67°C.

Graph of LN Dark Signal versus 1/T (Front-Face CCDs)



5.3 Variation of AIMO Dark Signal with Temperature

To reflect the study of ultra-low dark signal, all measured values are shown in e/pixel/ hour. For the limited number of AIMO devices tested under special conditions, the measured values followed the depletion dark signal equation between -25°C and -65°C. Below -65°C, further reduction of dark signal flattened off. This is assumed to be due to limits imposed by other factors, including trapped charge and light leakage. The lowest dark signals were ~ 1 e/pixel/ hour for back-thinned CCDs. The lowest dark signal for front-face CCDs was significantly higher at ~ 5 e/pixel/ hour, with scatter from the theoretical curve also higher. This was assumed to be due to thicker silicon active depth, generation at the epi /bulk interface, and a higher susceptibility to trapped charge, as well as potentially slightly higher bulk traps from the starting material in the older batches.

5.4 Gradient of Dark Signal with Temperature

For the limited number of AIMO devices tested under special conditions, the natural log of the measured dark signal was plotted with 1 / Temperature, and compared to the Depletion dark signal equation, over the range -25°C to -65°C. The gradient of this curve is much closer to that for the NIMO device, than to the gradient shown in current e2v AIMO datasheet.

6. Conclusions

The special test procedure developed for the study of dark signal in 15 off CCD230-84s has been successful in measuring ultra-low levels. The CCD230-84 datasheet gives the maximum value of dark signal at -25°C as 2 e/pix/sec or 7200 e/pix/hour. Under special conditions, but with only simple optimisation of bias and clock levels, and observing one or two key precautions, only moderate cooling was needed, e.g. to -35°C, to obtain dark signal 100x below this specification, for the devices tested. At -75°C, the back-thinned devices studied had a range in dark signal between 0.5 e/pix/hour and 2.5 e/pix/hour. At -68°C, the front-face devices had a range between 5 e/pix/hour and 21 e/pix/hour.

Reduction of dark signal flattened off below -65°C. The average lowest dark signals seen were ~ 1 e/pixel/ hour for back-thinned CCDs, and ~ 5 e/pixel/ hour for front-face CCDs. The higher value for front-face CCDs was attributed to batch variation, with the back-thinned CCDs being manufactured in 2015 and 2016 (with one exception), and the front-face CCDs between 2007 and 2010.

At temperatures below -65°C, the data indicates a much lower rate of change of dark signal with temperature, which has been interpreted as a temperature independent 'floor'. All imagers tested followed the theoretical depletion dark signal curve until reaching this floor, but then each had slightly different floor values. The floor is not thought to be due to clock induced charge, since this is estimated to be at a much lower level under the conditions of the test, and was in any case eliminated by the subtraction of a zero image from the dark signal image. Trapped charge may have contributed to the floor, but repeated measurement of the dark signal over a 40 minute period should have identified values that were affected, and there was only one instance. Possible sources of the floor remain as a systematic error in temperature offset between the device and the cold-plate at the lowest temperatures, and residual light leakage into the camera. Tests took place in a sealed vacuum test system in a normally illuminated room, with black cloth placed over the few parts known to have some light leakage, such as feedthroughs.

The pinning curve of dark signal versus Vss for each device ensured that correct AIMO mode was used - with 9.5V Vss being sufficient. The transfer of peak charge with good image spatial resolution showed that full charge transfer was maintained at ≥ 9.0V clock amplitude, giving very low CIC. Attention to other operating conditions included the avoidance of power cycling when the device was cold, to avoid trapped charge.

For the 15 off CCD230-84s studied, over the temperature range between -25°C and -65°C, we see that the equation of dark signal versus temperature is much closer to the NIMO (depletion dark signal) one, than to the 'IMO' (diffusion dark signal) one, probably due to incompletely suppressed surface dark signal in the latter. The dark current can be predicted from the Depletion dark signal equation:-

$$C_1 T^{3/4} e^{-E_g/2kT} + C_2$$

where C_1 and C_2 are constants.

The exponential term is $e^{-6662/T}$. This is similar to that in the NIMO dark signal equation in e2v datasheets: $C_3T^3e^{-6400/T}$. The C_2 constant shows the limiting dark signal, due to factors such as trapped charge, and system light leakage.

The datasheet for the AIMO CCD230-84 states that the dark signal is measured at 248 K (-25°C), and that the dark signal equation is valid between 248 K and 300 K. Since this study reports on dark signal between -25°C and -80°C, it is not in conflict with the datasheet. The guaranteed dark signal for the CCD230-84 and other e2v CCDs remains as in the relevant datasheet, with the specified dark signal at the specified test temperature. Similarly, the equation in the AIMO datasheets for typical dark signal remains unchanged for the time being, until further tests are carried out. However, this study shows the potential for ultra-low dark signal in Teledyne e2v AIMO CCDS, and opens the possibility of premium grades tested at lower temperatures, with lower specified dark signal.