Data Sheet
VEGA – CIS113
Large Area and Buttable CMOS Image Sensor

FEATURES

- 1920 × 4608 Pixels

  Pixel size is 16 µm square
- Eight parallel analogue output ports

  Each port has both reset and signal levels; external subtraction can give CDS
- Back-illuminated sensitivity and low readout noise

  Excellent image quality
- An easy to drive image sensor for use in astronomy and science applications

  Serial buses for row and column addresses
- Can be butted together on three sides

  Large focal plane arrays can be built
- Delivered in robust transport and handling jig

OVERVIEW

This sensor has a large image area, 30.72 mm × 73.73 mm, with 1920 × 4608 pixels at 16 µm square. It is read out through 8 parallel analogue output ports, normally in rolling shutter mode. Each port has both reference and signal level outputs for both external CDS subtraction and to improve common mode noise rejection.

Row and column addresses are input on serial buses, with separate row addressing for each half of the device and separate column addressing for each group of 240 columns.

In full frame mode the basic readout rate is 1.8 fps, but by only reading a selection of row and column addresses it is possible to read a large number of small “Regions Of Interest” (ROI) and achieve a frame rate up to 20 fps. This is particularly useful when monitoring images like star fields, where most of the area is black.

This package has minimal dead space on 3 sides to allow close butting to form a mosaic array.

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PERFORMANCE (ELECTRO-OPTICAL SPECIFICATION)

Grade 1 device performance at −25 °C will be within the limits specified by “max” and “min” in Table 1 when operated at the recommended supply voltages and with the recommended read timing. Grade 5 devices may not meet these limits.

Parameter	Min	Typical	Max	Units	Note
Pixel size		16		µm	Square
Number of active rows		4608			1
Number of active columns		1920			1
Image area		73.728 × 30.72		mm × mm	
Output settling time			420	ns	2
Frame rate when reading whole array			1.8	fps	3
Q_{SAT}, saturation charge per pixel	17,500	19,000		e^-/pixel	4
Q_{LIN}, peak linear charge per pixel	15,000	15,500		e^-/pixel	5
Non-linearity		±1.5	±3	%	6
CVF, overall conversion gain	80	90	100	µV/e^-	7
ERS readout noise in electrons	–	2.3	5.0	e^- rms	8
ERS readout noise in µV	–	210	400	µV rms	8
Dynamic range	–	76		dB	
GS readout noise in electrons				e^- rms	9
GS readout noise in µV				µV rms	9
Readout pixel rate	–	2		MP/s	
Time to read and readout one complete row or half row	130			µs	
Dark current	–	0.15	0.5	e^-/pixel/s	10
DSNU at		0.1	0.5	e^-/pixel/s	11
Small signal lag (at 0.3 V)		2	5	%	12
High signal lag (at 1.2 V)		3	5	%	12
Quantum efficiency at 800 nm	45	50	–	%	13
PRNU		2	3	%	14

Table 1: Electro-optical characteristics at −25 °C.

NOTES to Table 1

1) There are also 6 rows or columns of dummy pixels along each edge of the active array. These pixels cannot be read and so have no address.

2) Settling to 99 % of final change in signal voltage. Measured with I_{READ} = 40 µA and I_{OUTPUT} = 24 µA.

3) Reading many small regions of interest will allow a higher frame rate, well over 1000 blocks of 5 by 5 pixels at 20 fps are possible, when spread over the whole array. An extreme version of this is to image just one 5 by 5 block – this has been tested at 10,000 fps, but even faster is possible.

4) Maximum signal level. Set by the sense node and not by the pinned photodiode.

5) Signal level at which non-linearity is 5%. Set by the sense node and not by the pinned photodiode.

6) Measured from 5 % to 90 % Q_{LIN}. See the section *Non-linearity* under DEFINITIONS for more details.

7) Charge to voltage conversion factor (CVF) includes in-pixel source follower and whole path to output pin.

8) Electronic rolling shutter (ERS) readout noise is measured with external subtraction to give Correlated Double Sampling (CDS) and at 2 MP/s nominal pixel rate on each of the eight channels. Ipix set to 80 µA. Dark current shot noise will add to this readout noise. Grade 5 devices may have up to 7.0 e^- rms mean readout noise.

9) Global shutter (GS) readout noise is expected to be dominated by kTC noise from the sense node, but has not yet been measured. This mode cannot use CDS and so will show more noise than ERS.

10) Dark current is typically measured at a device temperature of −25 °C. It is a strong function of temperature and the temperature change to halve the dark current is typically around −5.5 °C.

11) Dark signal non-uniformity (DSNU) is the standard deviation of the pixel by pixel dark current. DSNU excludes defective pixels.

12) Lag is the residual charge in the pinned photodiode after the transfer pulse to move charge to the sense node. Lag varies with signal level, hence the two test levels in Table 1. Lag is measured at −25 °C. Lower operating temperatures give a higher level of lag. Longer transfer pulses on PIX_TRA_L/R can reduce lag.

13) Fill factor is very close to 100 % for BSI so QE is the same as SDE. See blue curve in Figure 1 for typical spectral response.

14) Photo-response non-uniformity (PRNU) is defined as (Standard Deviation of all pixel responses after subtraction of dark offset) × 100 / (Mean of all pixel responses) and is measured at half Q_{LIN}. PRNU excludes defective pixels.

SPECTRAL RESPONSE

The blue line in Figure 1 gives the response with the current production “Mid-band” AR coating at −25 °C:

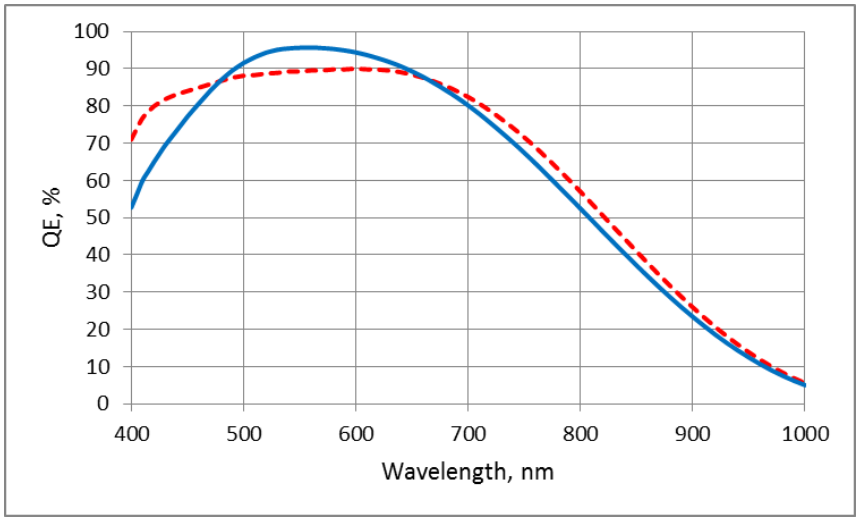

Figure 1: Calculated spectral response at −25 °C.

Different temperatures will change the QE at long wavelengths. Warmer gives a higher response and colder lower, but the main cause of the fall-off from the visible range is that at long wavelengths the absorption depth increases significantly and the available silicon thickness cannot absorb all of the incident radiation.

Devices with an alternate spectral response may be available to custom order – the dotted red line shows the effect of “Multi-2” coating; a flatter response over the visible range and a small improvement in the NIR. Consult e2v technologies for further information.

COSMETIC SPECIFICATIONS

Maximum allowed defect levels are indicated in Table 2:

Grade:	1
Bright pixel defects (% all pixels)	1 %
Pixel photo-response defects, not including those in column or row defects	200
Column defects	10
Row defects	10
Q_{LIN}	As Table 1

Table 2: Cosmetic specifications.

Grade 1 is the default for science use.

Grade 5 devices are fully functional but with an image quality below that of grade 1 (fail on at least one EO test parameter and with up to 7.0 e^- rms mean readout noise) and may not meet all other specifications – not all parameters are necessarily tested at this grade.

Grade 6 devices are mechanical samples. They are not functional, but will have the correct size and threads.

Other grades may be available.

Definitions for cosmetic specifications

Bright pixel defects	A pixel is counted as a bright defect if its dark current is ≥ 1 e^-/pixel/s at −25 °C.
Photo-response defects	A pixel is counted as a photo-response defect if its photo-response is < 80 % or > 120 % of the local mean.
Column defects	A column is counted as a defect if it contains ≥ 100 single pixel defects.
Row defects	A row is counted as a defect if it contains ≥ 100 single pixel defects.

Table 3: Definitions of types of defect.

DEFINITIONS

Back-Thinning

A back-thinned image sensor (CMOS or CCD) is fabricated on the front surface of the silicon and then subsequently processed for illumination from the reverse side. This avoids loss of transmission due to front surface features (metal tracks in CMOS or the electrodes in CCD) and also removes most of the etalon effect caused by multiple reflecting surfaces. Back-thinning reduces the silicon to a thin layer by a combination of chemical and mechanical means.

AR Coating

Anti-reflection coatings are normally applied to the back illuminated image sensor to further improve the quantum efficiency. Silicon has a very high refractive index so the air to silicon interface is highly reflective if it is not suitably coated. Standard coatings optimise the response in the visible, ultra-violet or infrared regions. For EUV, VUV and X-ray detection an uncoated device may be preferable.

Spectral Detection Efficiency (SDE)

The ratio of the number of electrons generated and sensed to the number of incident photons over the whole pixel. This includes the effects of Fill Factor, as well as the electro-optic physics.

Non-linearity

Non-linearity is the maximum difference between the measured output signal and an ideal linear fit in the signal range 5 % to 90 % Q_{LIN}. The chosen linear fit is a "least squares" fit over the range 0 to Q_{LIN}.

$$LinearityError_X(\%) = \left(\frac{Linearfit_X - Signal_X}{Signal_{Q_{LIN}}}\right) \times 100$$

The median non-linearity of all pixels will meet the limit in Table 1.

Correlated Double Sampling (CDS)

Each video output has two pins, an IMAGESIG[n] and an IMAGEREF[n]. The on-chip sampling will put the light-dependent level on IMAGESIG[n] following a transfer from the photodiode to the sense node. This will include the kTC noise from the reset of the sense node. The IMAGEREF[n] output will give the reset (black) level plus the same kTC noise. By means of a differential pre-amplifier it is possible to subtract the kTC noise and black level from the signal level to give low total noise. Using two reads will increase the readout noise by a factor of √2, but this is much less than the kTC noise on CIS113. If not required the IMAGEREF[n] outputs can be ignored.

Readout Noise

CMOS readout noise is the random noise from the pixel, read circuits and output stages which add a random fluctuation to the output voltage.

Dark Signal

This is the output signal of the device with no illumination. This typically consists of thermally generated electrons within the semiconductor material, which are accumulated during signal integration. Dark signal is a strong function of temperature as described in note 10 under Table 1.

ARCHITECTURE

Overall Floorplan

Figure 2 is drawn with the correct aspect ratio and at approximately real size. This shows how the 1920 columns are split into eight blocks of 240. Each block has separate read circuits and column select blocks and then drives a separate output channel (with reference and signal pins) – see also Figure 3. All blocks share the sampling timing from PIX_SHS and PIX_SHR.

All timing signals are input from an external controller to allow full optimisation of the performance of the pixels and read path. A typical timing diagram is given in Figure 12.

As shown in Figure 2, Figure 3 and Figure 16 the row addresses are independent for each half of the pixel array. Pixel timing signals are also input separately for each half and are then gated by the decoded row address to drive the correct half row. Left and right halves are separated only by breaks in the row control tracks, not by any change in the photo-sensitivity.

The terms “right” and “left” apply to this image sensor as orientated in the design database and also apply to the front illuminated early samples if the device is held with the readout end at the bottom. For the back illuminated devices the back thinning process includes a left-right flip of the silicon, so circuit blocks labelled right are on the left and vice-versa.

The read sampling signals drive the read circuits at the bottom of each column to sample all columns in one cycle, ready to be output one by one in each block of 240 columns. Output column address is independent for all eight blocks of columns.

Naming conventions used in this datasheet are (i) signals on pins are in capitals and internal signals in lower case letters and (ii) signals in the left or right sides end with _l or _r, but when either can be meant the end is _l/r.

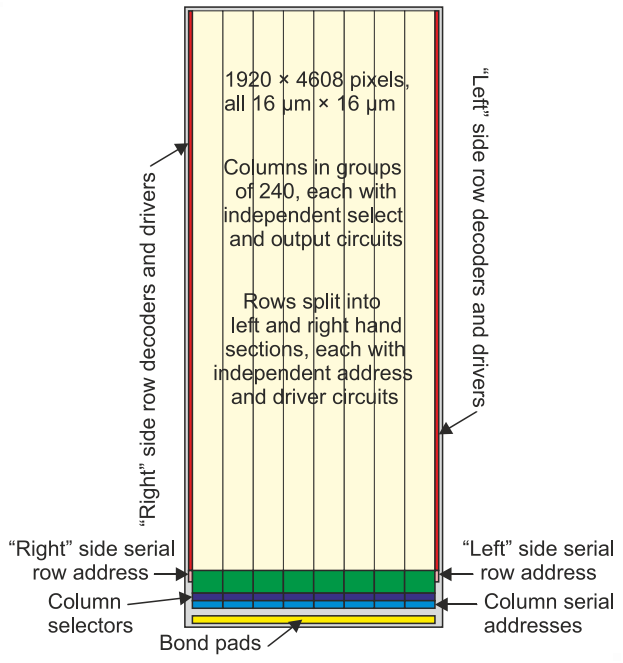

Figure 2: Floorplan of back thinned CIS113 die.

A more detailed floorplan is given in Figure 3:

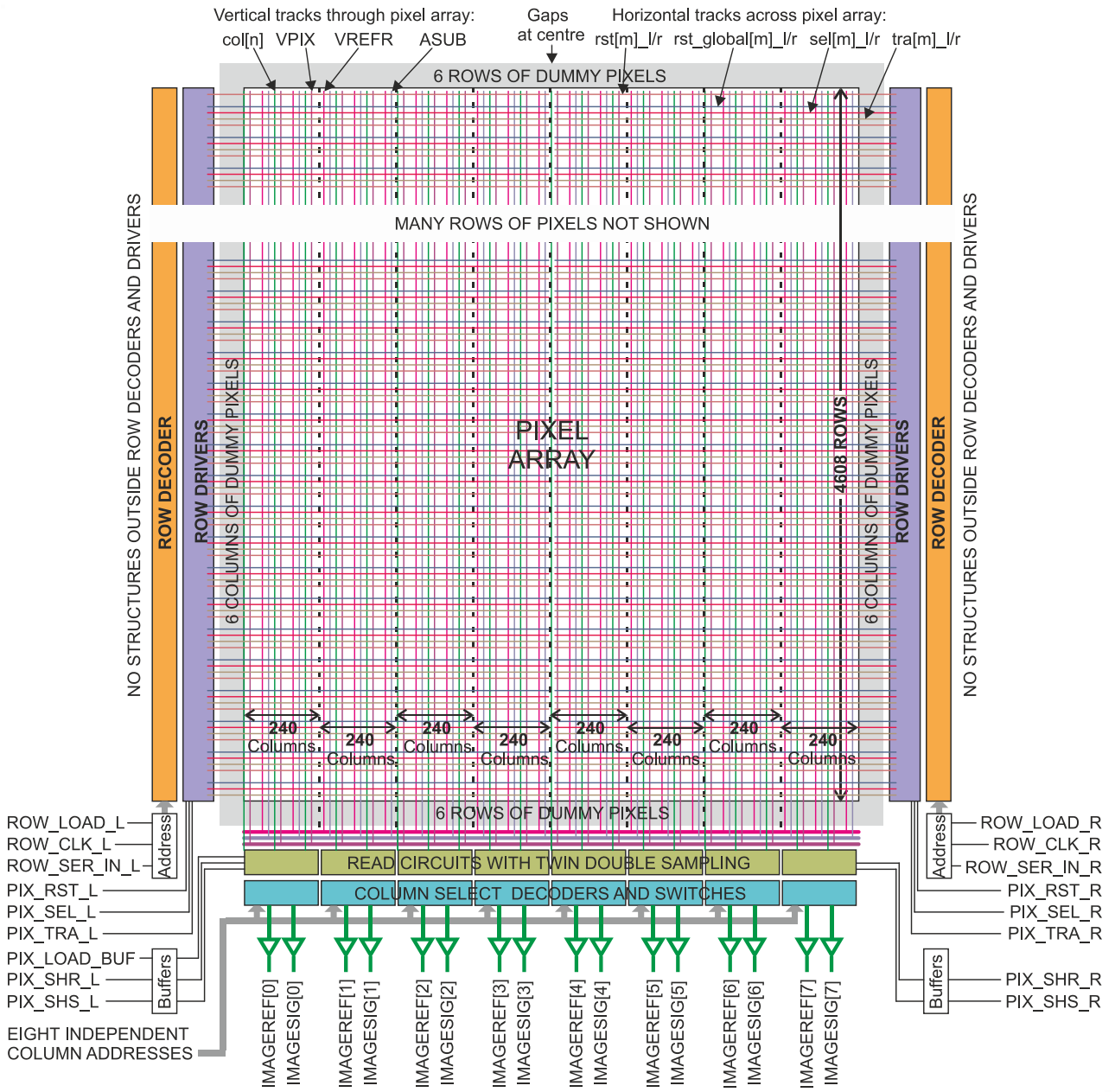

Figure 3: More detailed floorplan of CIS113 (front side view).

Only a few sample tracks for the control signals (rst[m]_l/r, rst_global[m]_l/r, sel[m]_l/r and tra[m]_l/r), are shown in the array area of Figure 3 to keep the diagram clear, while showing that they run horizontally across the array. Similarly only a few column outputs (col[n]) and the power and ground connections (VPIX, VREFR and ASUB) are included to show that they run vertically.

The pixel array is contiguous, but with each block of 240 columns feeding a separate output channel.

Figure 3 shows the left-right separation of the pixel read control signals. Each of the pixel controls PIX_RST_L, PIX_SEL_L, PIX_TRA_L, PIX_RST_R, PIX_SEL_R, PIX_TRA_R and PIX_RST_GLOBAL from pins are gated with the left or right decoded row address to form rst[m]_l, sel[m]_l, tra[m]_l, rst[m]_r, sel[m]_r, tra[m]_r, rst_global[m]_l and rst_global[m]_r to read the required two half rows of pixels. It is common to have different row addresses for the left and right halves of the pixel array as the way to maximise frame rate when monitoring many small ROI scattered over the image area.

By setting PIX_GLB_SHUTTER pin to high, the two sets of signals, rst_global[m]_l and rst_global[m]_r, both driven from pin PIX_RST_GLOBAL, can all be set high together without any gating with addresses as the global reset part of a global shutter. See the

section *Global shutter* under DEVICE OPERATION for further details. When not used as a reset these act as an anti-blooming charge dump on the photodiode.

Row addresses are loaded serially by either set of left or right pin signals, ROW_LOAD_L, ROW_CLK_L and ROW_SER_IN_L or ROW_LOAD_R, ROW_CLK_R and ROW_SER_IN_R. See the section TIMING INFORMATION and Figure 10 for further details.

To sample the levels on the column outputs there are the usual two signals PIX_SHR and PIX_SHS on pins, but to maintain good timing accuracy these are split into two tracks each in the package, to give PIX_SHR_L, PIX_SHS_L, PIX_SHR_R and PIX_SHS_R onto the chip. After their buffers, the left and right pairs are then joined back together in the block of read circuits.

PIX_LOAD_BUF is used to set which sampling circuits will sample the pixel outputs and which will drive the output pins. See *Odd-even sampling* and Figure 6 to Figure 9 later in this section for further details.

Eight independent column addresses are loaded in parallel through the separate bits of COL_SER_IN[7:0], each acting as a serial bus, clocked by COL_CLK and loaded by COL_LOAD. See TIMING INFORMATION and Figure 11 for further details.

Each column select block drives the reset (reference) and signal levels out through one pair of IMAGEREF[7:0] and IMAGESIG[7:0] pins to form a channel.

The device is designed with all connections (bond pads) on one edge (the bottom edge in Figure 2 and Figure 3) to allow the 3-side butting.

Pixel Design

All pixels in CIS113 are of the same 5T design, as in Figure 4. The fifth transistor in the pixel (labelled “Global-reset”) allows two options – either a normal rolling shutter 4T pixel with anti-blooming through this fifth transistor and with external subtraction to give CDS or a global shutter without CDS. All transistors are nmos, but each threshold voltage is carefully chosen for that transistor’s purpose. Ultra-low V_T is used for the source follower to give the lowest readout noise and due to layout constraints is also used for the select transistor. Ultra-low V_T is also used for the reset transistor to remove the need for high voltage drivers on the rst(m)_l/r signals. Transfer transistors are optimised in many ways for charge movement from pinned photodiode to sense node and have their own quite high V_T. Finally the global reset transistor has a V_T chosen so that when the gate is at 0 V, current will pass as soon as the pinned photodiode becomes excessively discharged from its reset level.

In order to improve the SDE at IR wavelengths the epitaxial layer (epi) has been chosen to be thicker than standard. To then maintain good MTF at all wavelengths the epi has also been chosen to have higher resistivity than standard. This combination of resistivity and thickness is becoming standard in CMOS image sensor products.

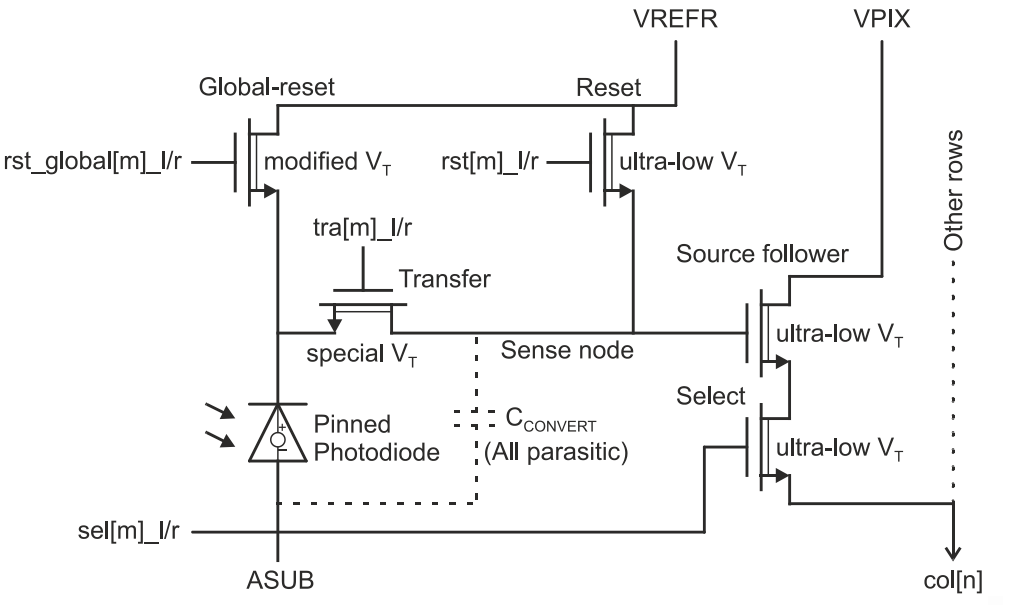

Figure 4: Circuit diagram of each pixel.

Pixel operation

Pixel control signals rst_global[m]_l/r, rst[m]_l/r, sel[m]_l/r and tra[m]_l/r (see Figure 4) are the local versions of the pin signals PIX_RST_GLOBAL, PIX_RST_L/R, PIX_SEL_L/R and PIX_TRA_L/R formed by gating with the decoded row address and then buffering to drive all pixels in the addressed half row. This gating is such that all unaddressed rows have all four signals at low (no sense node reset during integration). For the addressed row the internal signals follow the levels on the associated pin. Each read sequence needs the row select to be at high, so many systems keep the PIX_SEL_L/R pins at high from one read to the next – only the addressed row will see the select.

The signals rst_global[m]_l/r are the internal buffered copies of wire bond signals PIX_RST_GLOBAL_L/R, in turn both driven by pin PIX_RST_GLOBAL. When pin PIX_GLB_SHUTTER is at low only the addressed half rows follow the state of PIX_RST_GLOBAL to high. When pin PIX_GLB_SHUTTER is at high all half rows in both the left and right hand arrays follow PIX_RST_GLOBAL to high. See the section *Global shutter* under DEVICE OPERATION for further details.

Pixel column outputs col[n] drive the read circuits at the bottom of the pixel array. These include a pull-down current source which is biased by IPIX to give a balance of low noise bandwidth and a reasonably fast read speed.

Pixel power and ground connections VPIX, VREFR and ASUB are directly connected to the pins with the same names. The advantage of two supply connections to the pixel is to allow the sense node reset level and the source follower drain supply to be independently adjusted, to find the best operating point. In some applications VREFR and VPIX will be connected together.

One unusual feature of this image sensor is the use of two sets of readout sampling circuits so pixel levels from one row can be sampled while the previous row is being output. When a sparse set of regions of interest (ROI) is imaged, with only a few columns needed for each row, this allows a usefully higher frame rate. Details of this operation are given in the section *Odd-even sampling* under ARCHITECTURE, but in this section the suffixes "_even" and "_odd" are introduced.

In normal rolling shutter operation, each integrate and read cycle starts with the pinned photodiodes charged to their reset level by using the reset and transfer transistors in the previous cycle. Light is absorbed in the silicon in and below the photodiodes and releases electrons which are collected by the photodiodes, reducing their potential from the reset level.

During most of this integration time, all reset control lines rst[m]_l/r are held low, as no more than one row can be addressed at any time. A pulse on the addressed rst[m]_l/r is needed just before half row m is read in order to drive all sense nodes in that half row to the reset level. This is normally provided by loading the address while pins PIX_SEL_L/R are high and then pulsing PIX_RST_L/R, see Figure 12.

Once the addressed rst[m]_l/r and sel[m]_l/r feedthrough are finished and the sense nodes have settled at the reset level, a pulse on pin PIX_SHR drives the shr_even or shr_odd sample and hold circuits at the bottom of every column (see Figure 5) to store the reset levels on nodes vr_even or vr_odd.

The next action is a pulse on pin PIX_TRA_L/R to drive a pulse on the addressed tra[m] to move the charge from the photodiodes to the sense nodes. When the sense nodes have settled to their new levels, a pulse on pin PIX_SHS drives the shs_even or shs_odd sample and hold circuits at the bottom of every column (see Figure 5) to store the signal levels on nodes vs_even or vs_odd.

After this pulse on PIX_SHS, the row has been read, with all reset and signal levels stored in the sample and hold circuits. These levels are ready to be output through the column selector and output pins after PIX_BUF_LOAD changes state (see the section *Odd-even sampling* under ARCHITECTURE and Figure 6). External subtraction can then be used to have the lowest noise by CDS.

Each group of 240 columns has a separate column address decoder, driven to the required addresses by one of COL_SER_IN[7:0,] and by COL_CLK and COL_LOAD, see Figure 11.

The sample and hold circuits have buffers with individual enable signals to minimise power consumption and also two paths, col_sel_even[n] and col_sel_odd[n] for the odd-even sampling. These drive a multiplexor which selects which column will drive the appropriate output channel IMAGEREF[7:0] and IMAGESIG[7:0] for that set of 240 columns (see Figure 5).

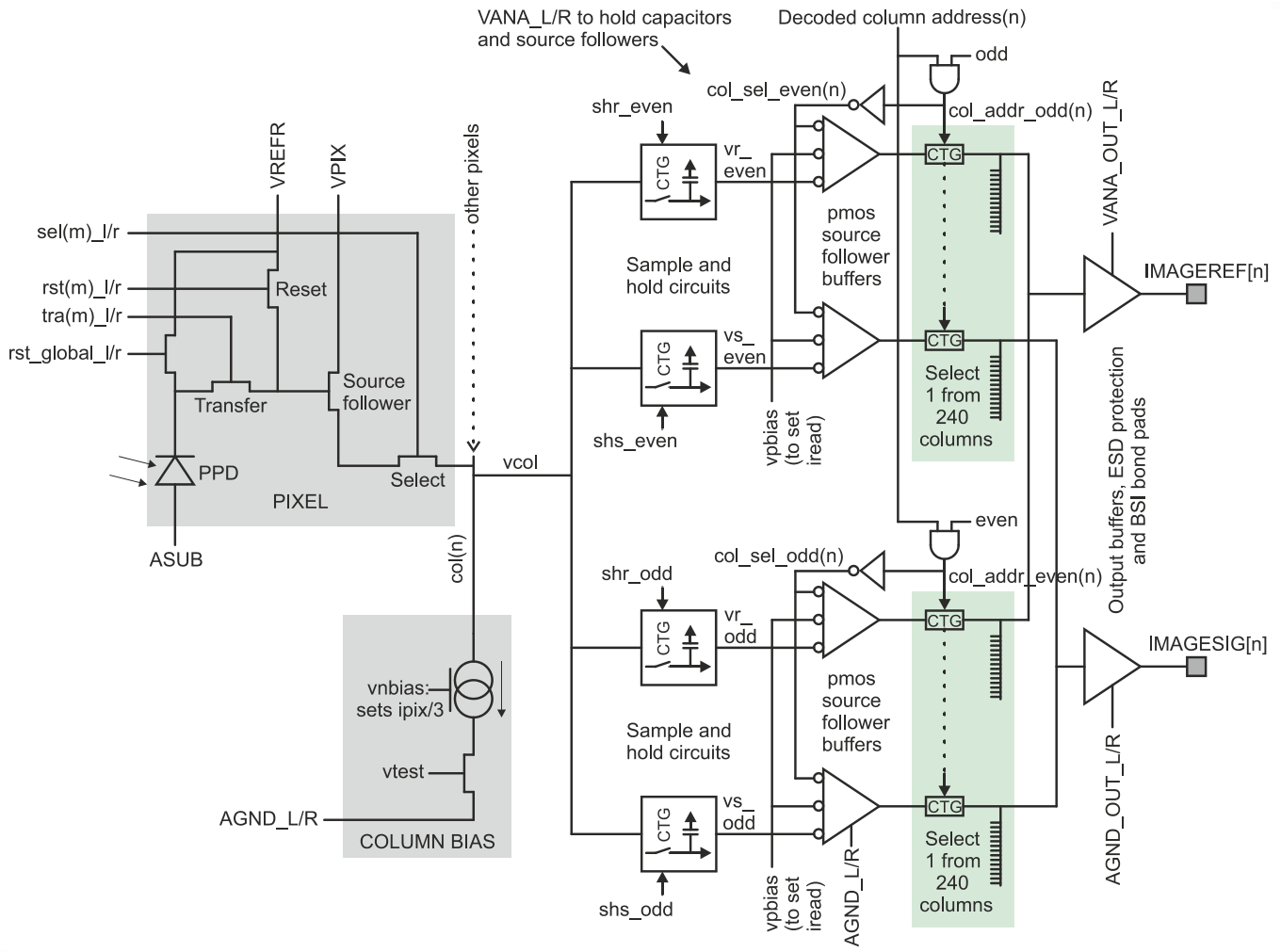

Figure 5: Read path from pixel to output pins for column n.

Odd-even sampling

The two readout sampling circuits operate on alternate rows to be read and have the names even and odd. This refers to the read cycle number, not to the geometric position of the rows. When the even sampling circuits are being driven by a row of pixels the odd sampled values can be output and vice-versa.

Control of even or odd mode is by pin PIX_BUF_LOAD, such that a logic “0” will give sampling into the odd path and reading from the even path and a logic “1” gives sampling into the even path and reading from the odd path.

As shown in Figure 5, col_sel_even[239:0] and col_sel_odd[239:0] drive pmos switches and so are active low. The upper path will sample the pixels in an even state by shr_even and shs_even and will drive the outputs in an odd state through source followers and complimentary transmission gates (CTG). The overall pattern of even and odd timing is shown in Figure 6.

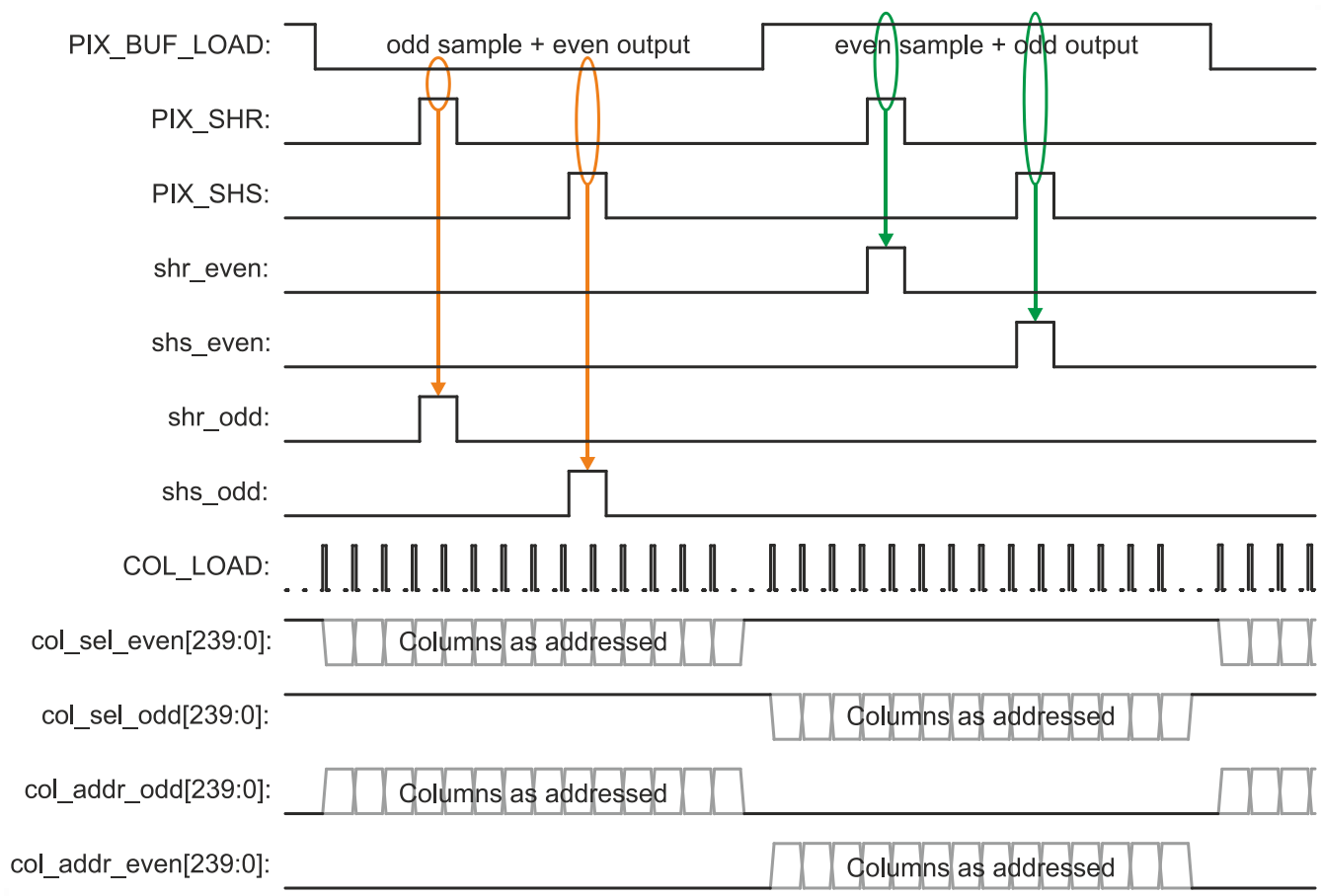

Figure 6: Odd-even sampling and output.

This use of alternating odd and even sampling and output allows a significantly higher frame rate only if the number of columns to be output is kept small. For maximum frame rate, the required set of columns must be output in no more time than the pixel read timing. When full frame image sensing is necessary the column output time will set the row read period, with the pixel timing occurring during the opposite PIX_BUF_LOAD phase.

For initial trials a simple timing plan can be used, with the odd-even switching reduced to loading the row address and doing the pixel timing in one state of PIX_BUF_LOAD and then loading column addresses and driving the outputs in the other state. This is shown in Figure 7. As the odd-even pipelining is not being used there is no need for the two states of PIX_BUF_LOAD to have the same duration.

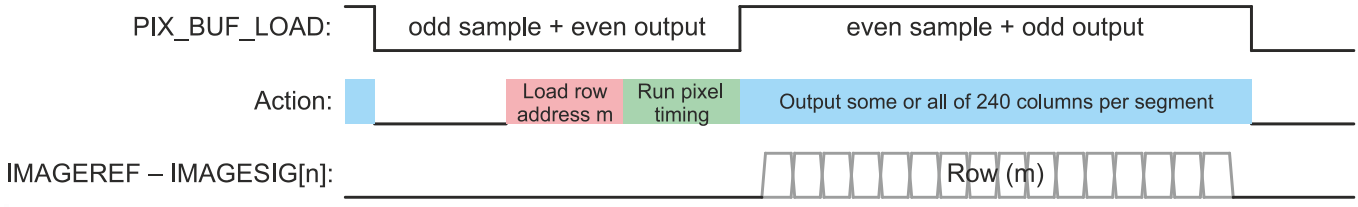

Figure 7: Simple timing mode.

Pipelining can be used to increase the frame rate. The two reset and signal paths shown in Figure 5 can be used alternately for odd and even phases. This allows one row to be read out while the next is being sampled. If the number of columns to be read out is such that the total time to output them is longer than the total of row address loading plus pixel timing, there will be some spare time in the row address plus pixel timing phase. This spare time can be placed whenever convenient. Figure 8 shows a split in the spare time, with some before and some after the row address and pixel timing activities. This figure uses row numbers (m − x), (m) and (m + y) to emphasise that the rows in consecutive read cycles do not need to be adjacent.

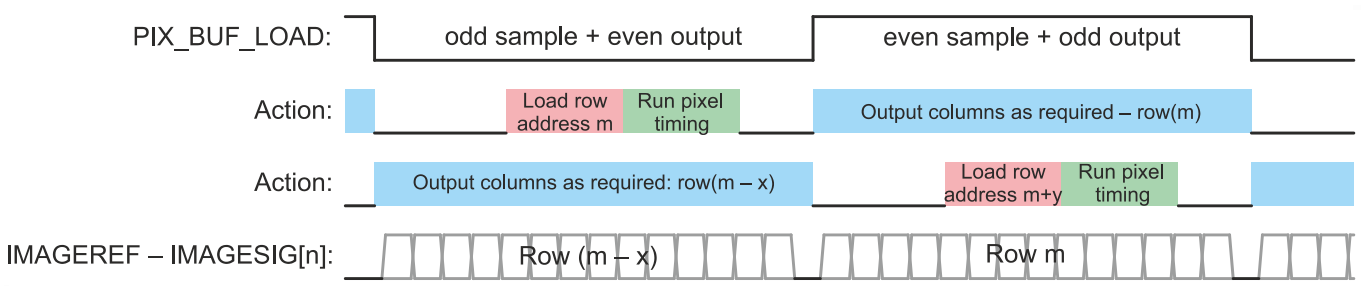

Figure 8: Pipelined timing mode.

For the maximum frame rate the next step is to run the row address loading and the pixel timing in parallel. Clearly the row address must be stable during the pixel timing, so this extra pipelining must complete the row address load after one pixel timing, ready for the next cycle. With a typical row address clock the duration of the address loading will be less than the pixel timing and for maximum frame rate the number of columns to be output must also be limited such that the output duration is also less than the pixel timing. This is all shown in Figure 9, at an expanded time scale when compared to Figure 7 and Figure 8.

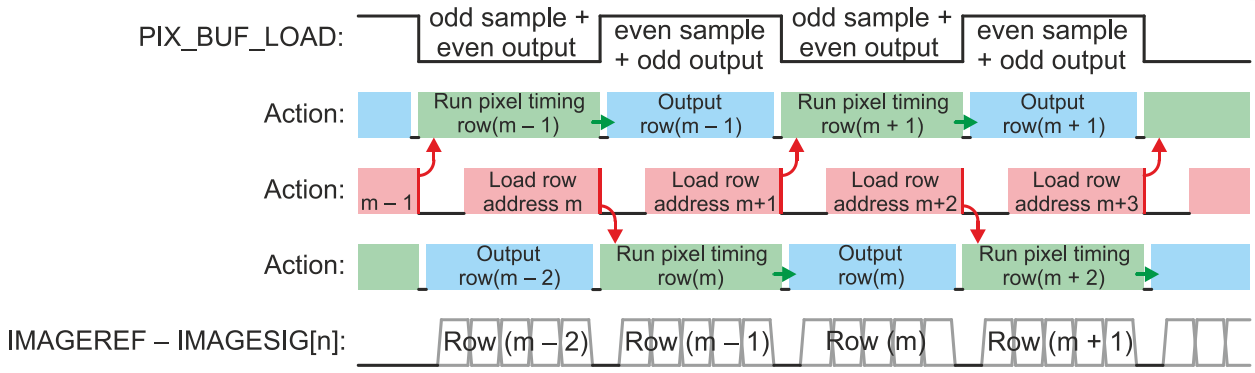

Figure 9: Multiple small ROI and pipelined for high frame rate.

Unlike Figure 8 with its (m − x), (m) and (m + y) phases, the labelling in Figure 9 is (m − 2), (m − 1), (m), ... to (m + 3) to show the sequence, but there is still no need for the rows to be contiguous. In many applications the readout will be from a small number of contiguous rows to give an ROI and then a jump to the next ROI.

In the original application for which CIS113 was designed the primary aim was to monitor at least 1000 ROI each of 5 × 5 pixels at 20 fps. A combination of pixel timing and of the positions of the ROI will determine the maximum number in practice:

With the ipix current set to 80 µA it is possible to run the pixel timing in 10 µs, as in Figure 12 and Table 6. Any timing less than 10.85 µs allows all 4608 rows to be sampled at 20 fps, including at least 921 small (5 × 5) ROI in each half or 1842 in the whole array. As all rows are sampled there are few restrictions on where even more ROI can be placed – the only limit now is ≤ 20 columns to be output per channel.

The small ROI are often described as being 5 × 5, but this is not a fixed feature of this image sensor. Other sizes, for example 6 × 6, 8 × 8 or non-square can also be chosen.

Although anti-blooming by the global reset transistor is described in the section *Pixel design* under ARCHITECTURE there can be some benefit in reading the rows not needed for ROI from time to time to avoid building up charge – this is especially important when some pixels of no interest are lit.

TIMING INFORMATION

There are three phases in the timing to read CIS113: (i) set-up row addresses (left and right can be the same or different), (ii) read and sample the pixel levels and then (iii) scan the required columns (a few for high frame rate or all columns for whole field of view at a low frame rate).

As described in the earlier section *Odd-even sampling* under ARCHITECTURE, the input signal PIX_BUF_LOAD is used to set which of the odd or even sample and hold circuits do sampling and which drive outputs. This signal is common to both left and right halves of the pixel array and the pixel sampling signals PIX_SHR and PIX_SHS are also common, but PIX_RST_L, PIX_RST_R, PIX_TRA_L, PIX_TRA_R, PIX_SEL_L and PIX_SEL_R are separate for the two halves. PIX_RST_GLOBAL and PIX_GLB_SHUTTER are not always used, but are common to both halves for when a global shutter is wanted.

Row address loading

To load the 13 bit row addresses, signals ROW_CLK_L, ROW_SER_IN_L, ROW_LOAD_L ROW_CLK_R, ROW_SER_IN_R and ROW_LOAD_R are used. The left and right addresses do not need to be synchronous, indeed it is possible that only one address is required at times, but as the pixel sampling signals PIX_SHR and PIX_SHS are common to both sides the addresses will often be synchronous, especially at high frame rates. Figure 10 shows the waveforms for ROW_CLK_L, ROW_SER_IN_L and ROW_LOAD_L to load a left address. The timing for ROW_CLK_R, ROW_SER_IN_R and ROW_LOAD_R to load a right address is exactly the same.

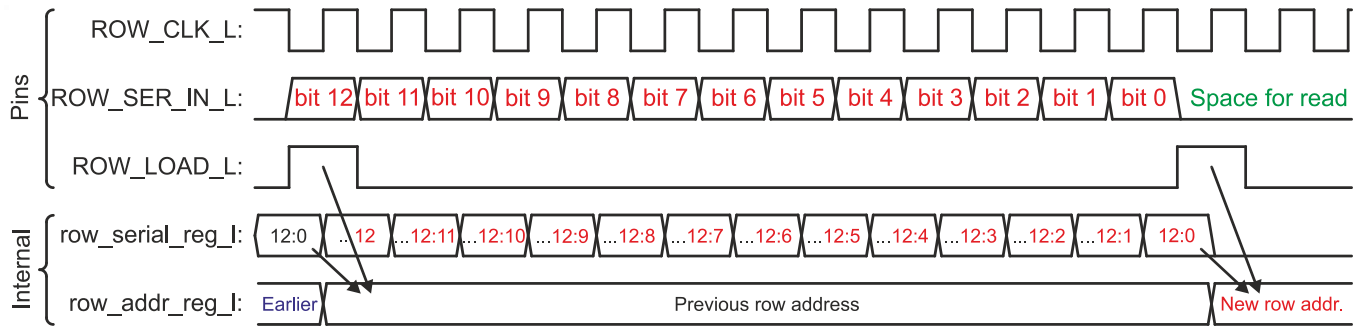

Figure 10: Row address loading.

Every rising edge on ROW_CLK_L/R loads the data on ROW_SER_IN_L/R into a shift register row_serial_reg_l/r and moves the data already there one bit sideways. When a rising edge on ROW_CLK_L/R occurs while ROW_LOAD_L/R is high this edge will also copy the data from row_serial_reg_l/r to a holding register row_addr_reg_l/r to drive the address decoders.

Figure 10 shows the timing sequence with normal pixel timing; extra time is added between row addresses by starting the next address some time after the ROW_LOAD_L/R pulse of the previous address. The need to fit the pixel timing into the row address loading (see Figure 9) allows ROW_CLK_L/R to be at a very low frequency (see Table 4). In this mode 14 clock cycles are used to load one address.

When many small ROI are needed and the pixel timing is fast, each row address can follow immediately after the previous address and only 13 clock cycles are needed per address – one cycle does the ROW_LOAD_L/R and next bit_12 simultaneously.

PIX_BUF_LOAD must be toggled for every address to each side to get the odd-even sampling; when one or both addresses do not change, a PIX_BUF_LOAD toggle will be needed to output the last sample. This toggling is illustrated in Figure 6 to Figure 9 and in Figure 12.

Parameter	Min	Typical	Max	Units	Note
Period of ROW_CLK_L/R		460		ns	
Setup time ROW_SER_IN_L/R and ROW_LOAD_L/R to ROW_CLK_L/R rising edge		TBD		ns	
Hold time ROW_CLK_L/R rising edge to ROW_SER_IN_L/R and ROW_LOAD_L/R		TBD		ns	

Table 4: Row address timing values.

Column address loading

8 bit column addresses are loaded in a way very similar to the row address, except there are eight parallel streams of serial data (one for each channel) to input and the PIX_BUF_LOAD signal must not be changed during the output pattern. See Figure 11:

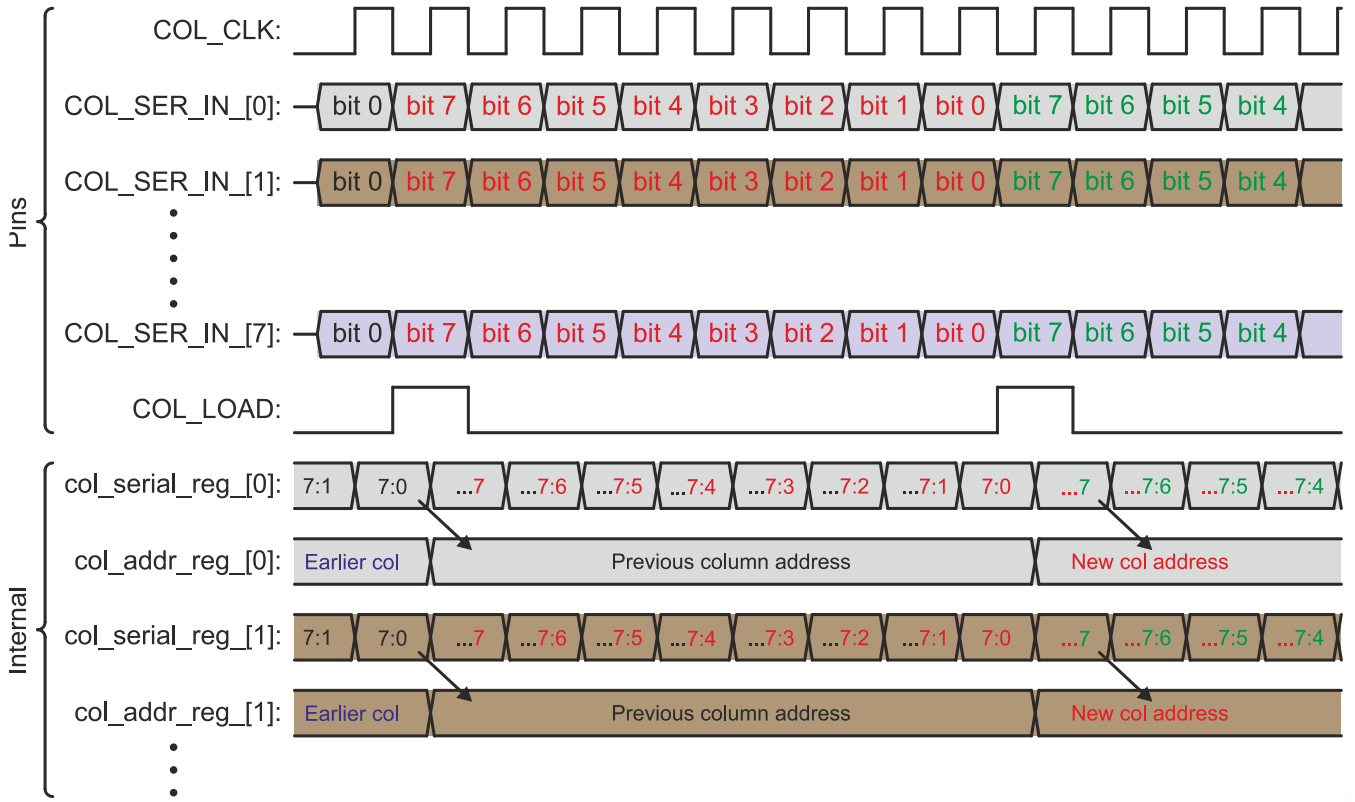

Figure 11: Column address loading.

Every rising edge on COL_CLK loads the data on each pin of COL_SER_IN_[7:0] into the corresponding shift register, one of col_serial_reg_[7:0] and moves the data already there one bit sideways. When a rising edge on COL_CLK occurs while COL_LOAD is high this edge will also copy the data from each col_serial_reg_[7:0] to the corresponding holding register, one of col_addr_reg_[7:0] to drive the address decoders.

Each column address only needs to select one signal to output, so it is normal to have the next address immediately after the previous, as in Figure 11.

Parameter	Min	Typical	Max	Units	Note
Period of COL_CLK		60		ns	
Setup time COL_SER_IN_[7:0] and COL_LOAD to COL_CLK rising edge		TBD		ns	
Hold time COL_CLK rising edge to COL_SER_IN_[7:0] and COL_LOAD		TBD		ns	

Table 5: Column address timing values.

Read timing

It is possible to operate this image sensor with many different pulse widths and spaces, but the sequence must be as in Figure 12. Durations and separations as in Table 6 were used for the measured performance.

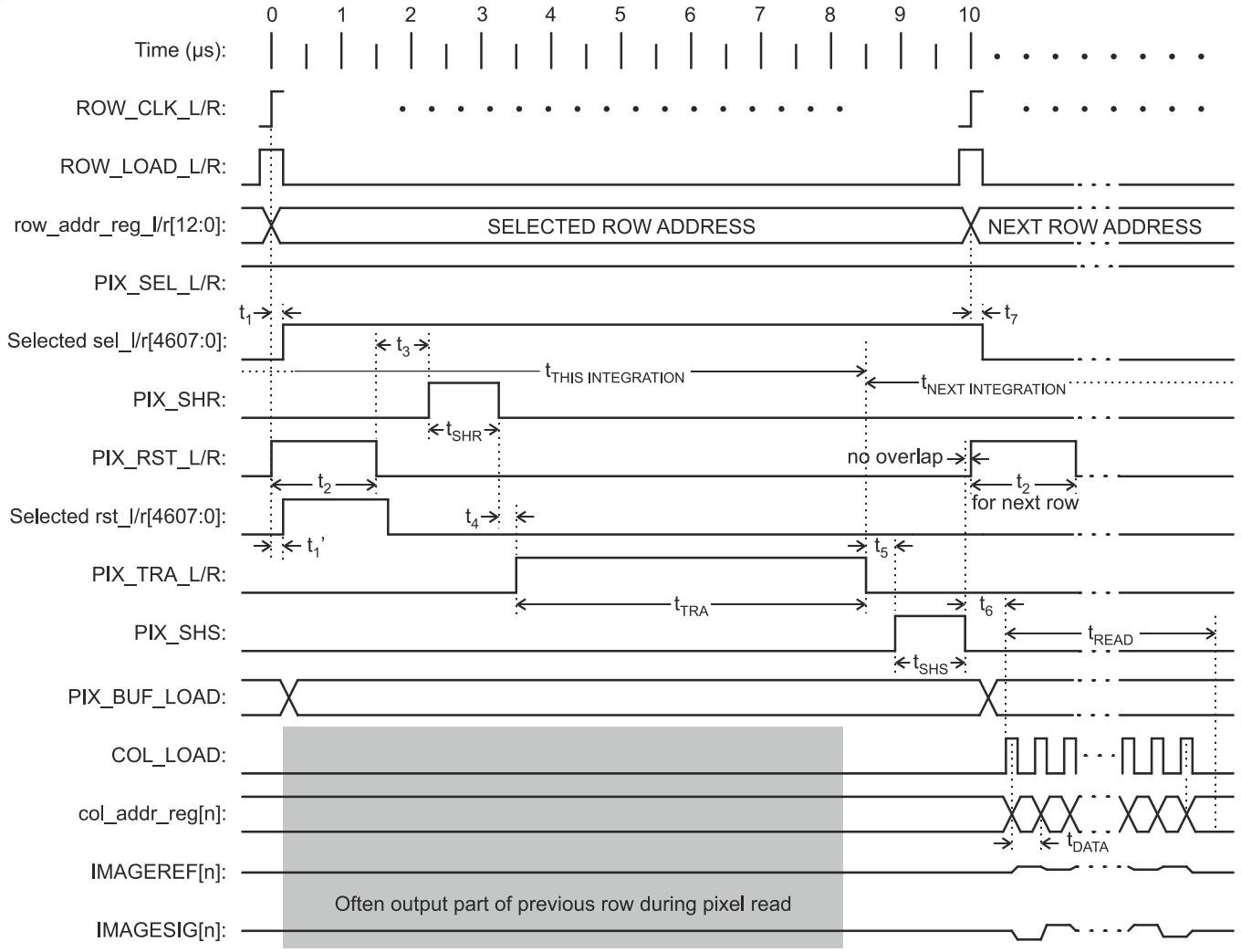

Figure 12: Typical rolling shutter timing diagram.

The row address is loaded first for left, right or both sides of the image sensor. This is shown in full in Figure 10, but only the ROW_LOAD_L/R pulse and one edge of ROW_CLK_L/R are included in Figure 12, as a reminder of their position. The new row address is loaded into row_addr_reg_l/r by the rising edge of ROW_CLK_L/R at close to the centre of the pulse on ROW_LOAD_L/R.

Pins PIX_SEL_L/R are often held at a logic “1” throughout the image capture process, with the row address selecting which sel[4607:0]_l/r to drive to a “1”. The selected sel[m]_l/r connects the selected row of pixels to the column tracks.

Pixel timing then continues, with PIX_RST_L/R pulsing high and low to reset the sense nodes in the selected half rows. PIX_SHR pulses to sample the reset levels on the columns, PIX_TRA_L/R is used to move the charge from the photodiodes to the sense nodes and then PIX_SHS samples the signal levels on the columns.

These sampled levels are then selected for output by the column address system as in Figure 11, but with only COL_LOAD included in Figure 12, again as a reminder of its position.

As shown in Figure 6 to Figure 9 and in Figure 12, the input PIX_BUF_LOAD must be toggled between the PIX_SHS pulse of each pixel row read and the start of the column selection to output levels.

This sequence may be repeated immediately to read another row provided the following PIX_RST_L/R pulse does not start to rise until the PIX_SHS pulse for the current row has returned to ground.

Any non-valid row address will not be decoded and so will not affect the integration of the required image, any non-valid column address will not be decoded, but may interrupt the readout of the image.

Note: IMAGEREF[7:0] will give the reset level of each pixel and so will show little change pixel to pixel. IMAGESIG[7:0] will give the result of the integration of light and so can show very large changes from pixel to pixel. The difference between these two signals gives the true value of the illumination, pixel by pixel.

Timing	Definition	Typical value	Unit
t_{SHR}	Pulse width to sample the reset level.	1.0	µs
t_{TRA}	Photodiode to sense node transfer pulse width. Includes time for the signal level to settle on the long column tracks.	5.0	µs
t_{SHS}	Pulse width to sample the signal after integration.	1.0	µs
t_{READ}	Time to read out 240 columns.	120	µs
t_{DATA}	Data time per pixel at 2 MP/s.	0.5	µs
$t_{THIS\ INTEGRATION}$ and $t_{NEXT\ INTEGRATION}$	Minimum integration time with full frame readout and pipelined operation.	553	ms
t_1	Propagation delay from ROW_CLK_L/R to new address loading to selected internal sel[m]_l/r rising edges.	TBD	ns
t_1'	Propagation delay from PIX_RST_L/R pin to selected internal rst[m]_l/r rising edges.	TBD	ns
t_2	Pulse width on PIX_RST_L/R to avoid a soft reset from SEL feed through.	1.5	µs
t_3	Delay time between PIX_RST_L/R falling edge and t_{SHR} to allow reset feedthrough to settle out on the long column tracks.	0.75	µs
t_4	Suggested time between t_{SHR} and t_{TRA}	0.25	µs
t_5	Suggested time between t_{TRA} and t_{SHS}	0.5	µs
t_6	Suggested time between t_{SHS} and start of column level outputs.	0.5	µs
t_7	Propagation delay from next address loading to selected internal sel[m]_l/r falling edge.	TBD	ns

Table 6: Typical timing values.

As suggested in Table 6, the timings used for measured results, both times t_3 and t_{TRA} are longer than for smaller image sensors, such as CIS115. This is due to the long column tracks of this large area sensor adding extra capacitance and so needing more time to fully settle at a typical ipix current.

Transfer pulse width t_{TRA} as given in Table 6 at 5.0 µs, will give a lag level as in Table 1 (typically 2 or 3 %). Other pulse widths may be used; shorter will give more lag especially at larger signal levels and longer will give less lag at all levels.

To achieve the highest frame rate in multiple region of interest mode, the number of columns to be output from each half row must be limited to less than 20, so each 10 µs row read can be immediately followed by another. This allows all rows to be read at 20 fps and will give at least 921 ROI per half array.

DEVICE OPERATION

As shown in Figure 12, the typical timing diagram, each row of pixels has its own integrate and read timing, giving the output of all rows in a sequence. If the row address is steadily incremented or decremented this gives a rolling effect and the mode is called a rolling shutter.

By processing the rows one at a time, it is simple to use external subtraction to have the lowest read noise by CDS.

A rolling shutter exposes and reads the pixels as in a traditional television raster scan – each row is read in turn, with its integration time between the reads in successive frames, giving a steady flow of signal, but the timing of each frame overlaps the preceding and following frames as in Figure 13.

By holding PIX_RST_GLOBAL at low all global reset transistors are held at “off” and give an anti-blooming effect.

With the CIS113 it is also possible to read the rows in any arbitrary order, so some rows may be read more often than others if the application requires this.

Although included as part of the global shutter circuit, PIX_RST_GLOBAL can also be used without PIX_GLB_SHUTTER at high to do a direct photodiode reset to the selected half rows of pixels.

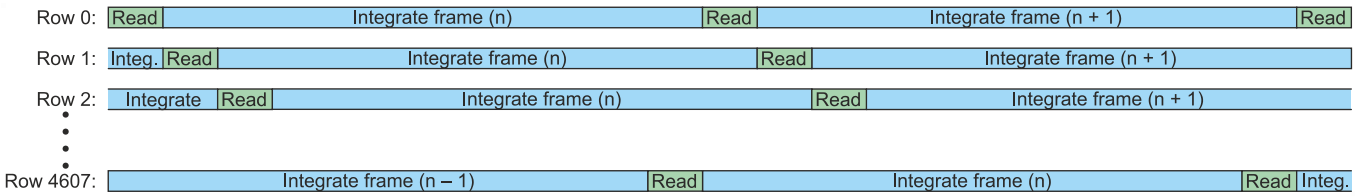

Figure 13: Normal rolling shutter.

Global shutter

As an alternative to the rolling shutter just described, the CIS113 can also offer a global shutter for when it is important to sample all pixels synchronously.

The individual selections of the half-row signals rst_global[4607:0]_l/r, rst[4607:0]_l/r and tra[4607:0]_l/r are replaced by a simultaneous selection of all half rows when PIX_GLB_SHUTTER is high.

In this mode PIX_RST_GLOBAL drives the direct photodiode reset rst_global[m]_l/r to every pixel (see Figure 4), PIX_RST_L/R drives all rst[m]_l/r and PIX_TRA_L/R drives all tra[m]_l/r signals without any gating with addresses.

A pulse on PIX_RST_L/R is needed just before the pulse on PIX_TRA_L/R to reset the sense nodes before the transfer. Light is integrated in all pixels from the end of PIX_RST_GLOBAL to the end of PIX_TRA_L/R, with the integrated charge then stored on the sense node in each pixel.

These charges can then be read out in a rolling sequence by using row addresses and PIX_SEL_L/R to select each row in turn to drive the columns in the pixel array. PIX_SHS then samples the levels on the columns into the output select block.

PIX_RST_L/R and PIX_TRA_L/R are held at low until the next frame has been integrated. In this mode PIX_SHR is not used at all as the reference levels were all deleted by the pulse on PIX_RST_L/R during the global image capture.

A typical timing diagram for global shutter operation is shown in Figure 14:

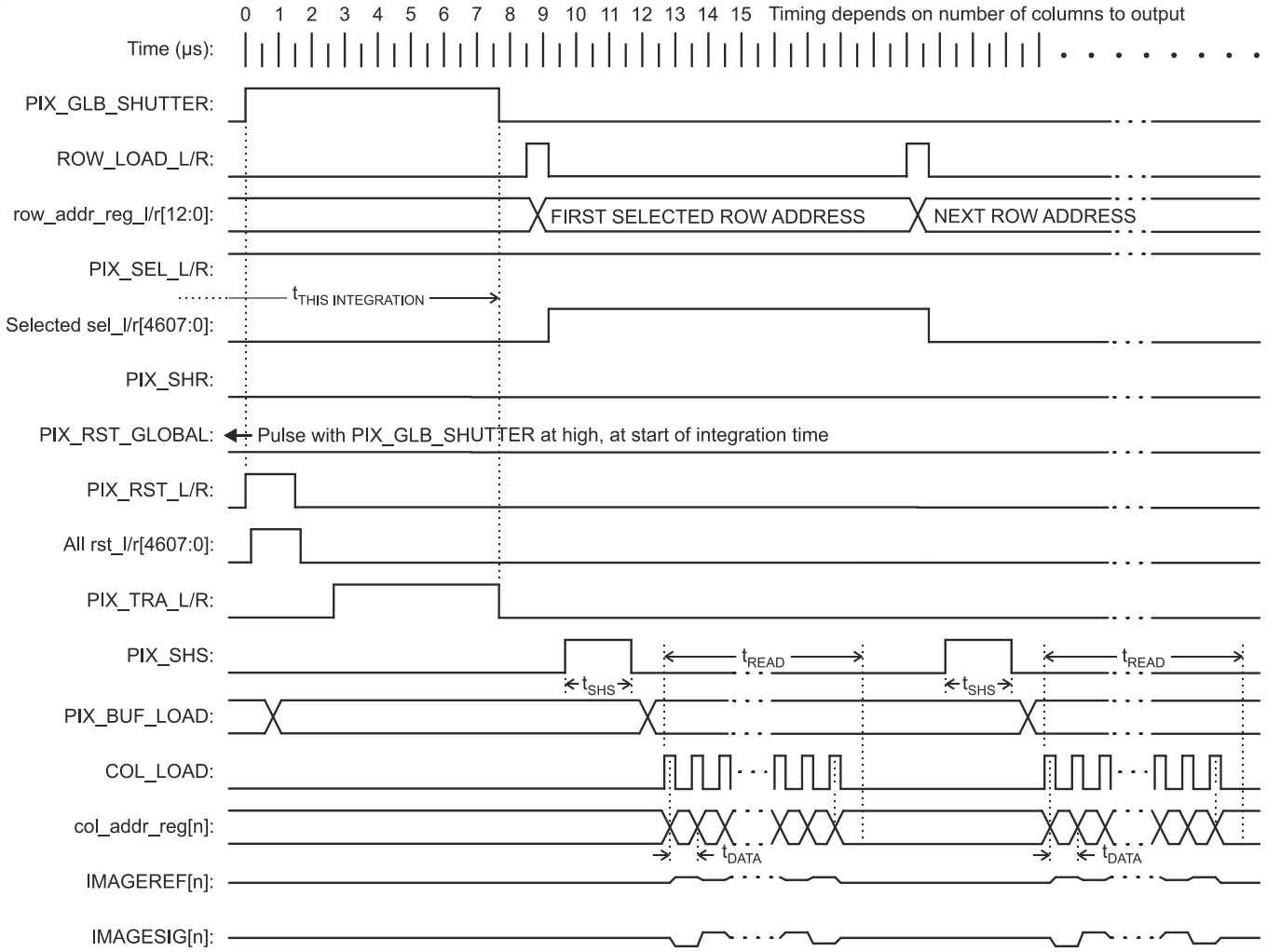

Figure 14: Typical global shutter timing diagram.

OPERATING CONDITIONS

The temperature ranges and power supplies to be used on the CIS113 are listed in Table 7:

Supply/Pin	Description	Value			Unit
		Min	Typical	Max	
T	Operating temperature – see note below	−100	20	60	°C
δT/δt	Maximum safe rate of heating or cooling			±5	K/min.
VDIG_L/R	Digital power supply to row and column select	1.65	1.8	1.98	V
VANA_L/R	Analogue power supply to read circuits	3.15	3.45	3.6	V
VANA_OUT_L/M/R	Analogue power supply to output buffers	3.15	3.45	3.6	V
VRESET	Select and reset driver supply to row drivers	2.0	3.45	3.6	V
VDDTRA	Supply used to drive the TG control gate	2.4	3.45	3.6	V
VREFR	Reset level power supply for all pixels	2.0	2.9	3.0	V
VPIX	Source follower power supply for pixels	2.0	2.9	3.0	V

Table 7: CIS113 operating temperature and supplies.

Notes: This image sensor will survive and operate at 60 °C, but the dark current will be very high, leading to very poor image quality. Recommended operating temperature is at or below 20 °C.

Performance parameters are measured with the device at a temperature of −25 °C and, as a result, full performance is only guaranteed at this nominal operating temperature.

Operation or storage in humid conditions may give rise to ice on the surface when the sensor is taken to low ambient temperatures, thereby causing irreversible damage.

Both of the two digital supply pins VDIG_L and VDIG_R should be used to minimise I.R voltage drops. These are connected together in the CIS113 and so must be driven by the same external supply. This is at a reduced typical level of 1.8 V to minimise noise generation.

Similarly, both of the two analogue supplies VANA_L and VANA_R should be used and are connected on-chip and so must be driven by the same external supply.

All three output buffer supplies VANA_OUT_L, VANA_OUT_M and VANA_OUT_R are connected together on-chip and for best performance all three must be driven to minimise I.R voltage drops. If VANA_L/R and VANA_OUT_L/M/R are to be driven from the same power source there must be significant filtering to prevent the output driver noise from degrading the analogue sampled signals.

VRESET sets the upper level of the drivers to the select and reset transistors in the pixels. To ensure a hard reset the level on the gate of the reset transistor is often higher than the main supplies, but in CIS113 the use of an "ultra-low V_T" reset transistor allows a normal supply level to be used.

VDDTRA sets the upper level of the drivers to the transfer transistors in the pixels, so to avoid lag the level should be controlled to a tighter tolerance than needed for other supplies.

VREFR drives the level on the drains of the reset transistors in the pixels and so needs to be at a lower potential than VRESET to ensure a hard reset.

VPIX drives the level on the drains of the source follower transistors in the pixels and so needs to be especially low noise. Provided the level is in the range in Table 7, the exact potential is often not critical.

End users are expected to adjust the supply levels to optimise performance in their application. This is particularly important for VRESET, VDDTRA, VREFR and VPIX. Levels lower than given in the Min. column in Table 7 can be preferred in some applications.

In addition to the power supplies there are also three current biases, IPIX, IREAD and IOUTPUT. These are input as currents to allow each application to use an appropriate accuracy. All three drive nmos current mirrors in the CIS113 and so take current from a positive supply, such as VANA and pass it to ground through the input part of the current mirror.

IPIX is used to set the pull-down current on each pixel column output track to IPIX × ⅓ by sizing the transistors in this path.

IREAD is used to set several pull-up and pull-down currents in the read path.

IOUTPUT is used to set the bias current in the output buffers.

All of IPIX, IREAD and IOUTPUT can be set at a low current to reduce power consumption or to a higher current for faster output settling time. Table 8 gives the expected ranges for these currents.

Active current sources are recommended for IPIX, IREAD and IOUTPUT to give good accuracy and repeatability.

Simple resistors to the appropriate VANA may be adequate in some applications.

Symbol	Description	Value (µA)		
		Min	Typical	Max
IPIX	Bias current for column pull-down.	1	80	100
IREAD	Bias current for read circuits (pull-up and pull-down)	8	40	100
IOUTPUT	Bias current for analogue output drivers.	8	24	150

Table 8: CIS113 bias currents.

Unlike some previous image sensors, such as CIS115, the row and column address decoders do not use a current source based decoder circuit, so there is no current to set and no voltage reference to monitor.

ROW AND COLUMN SELECT

Row addresses

Binary coded addresses are used for both row and column selection, all loaded serially.

As described in the section TIMING INFORMATION and shown in Figure 10, the 13 bit row addresses are loaded by signals ROW_CLK_L, ROW_SER_IN_L and ROW_LOAD_L for the left half and by ROW_CLK_R, ROW_SER_IN_R and ROW_LOAD_R for the right half.

In order to manufacture a large area image sensor like CIS113 a process called “stitching” is used. This uses exact repeats of a block of layout for the pixels, row decoders and row drivers, with a single copy of the layout for the top and bottom sections, see Figure 15.

Segment C is very narrow and just contains the top dummy pixel rows, seal ring and top/bottom saw lane.

Segment B has 1152 rows of real pixels, left and right columns of dummy pixels, row decoders, row drivers, parts of the seal ring and left/right saw lane. This segment is placed four times to make up the 4608 rows of pixels.

Segment A has everything else, including bottom dummy pixels, read circuits, column decoders, row and column serial to parallel registers and all bond pads.

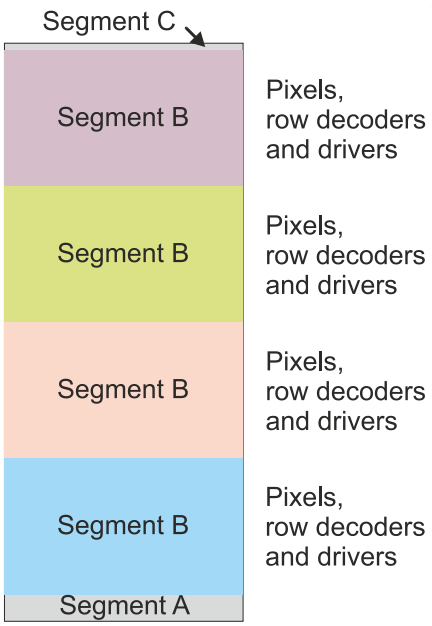

Figure 15: CIS113 stitching.

Within each segment B the row decoding is the same, so to address each copy separately the two MSB are bused with inverters and twists between each segment B. This gives an address range with jumps at each segment B boundary, see Table 9:

row_addr_reg_l/r[12]	row_addr_reg_l/r[11]	row_addr_reg_l/r[10:0]	Selection
1	0	10001111111	Row 4607 (top)
1	0	10001111110	Row 4606
1	0	10001111101	Row 4605
⋮	⋮	⋮	⋮
1	0	00000000010	Row 3458
1	0	00000000001	Row 3457
1	0	00000000000	Row 3456
Binary address jump			
1	1	10001111111	Row 3455
1	1	10001111110	Row 3454
1	1	10001111101	Row 3453
⋮	⋮	⋮	⋮
1	1	00000000010	Row 2306
1	1	00000000001	Row 2305
1	1	00000000000	Row 2304
Binary address jump			
0	1	10001111111	Row 2303
0	1	10001111110	Row 2302
0	1	10001111101	Row 2301
⋮	⋮	⋮	⋮
0	1	00000000010	Row 1154
0	1	00000000001	Row 1153
0	1	00000000000	Row 1152
Binary address jump			
0	0	10001111111	Row 1151
0	0	10001111110	Row 1150
0	0	10001111101	Row 1149
⋮	⋮	⋮	⋮
0	0	00000000011	Row 3
0	0	00000000010	Row 2
0	0	00000000001	Row 1
0	0	00000000000	Row 0 (bottom)

Table 9: Binary codes for pixel row addresses.

Row addresses with bits [10:0] at 10010000000 and above do not select any row of pixels or any other function.

At power-on or after a CHIP_RST pulse all row address registers will be set to 1111111111111. This does not select any row.

Using the column select circuit with a non-valid row address to output levels on IMAGEREF[7:0] and IMAGESIG[7:0] will give a level near the appropriate AGND_OUT_L/M/R.

Electrical transfer function test mode

As a means to check the operation of the support electronics, it is possible to plot the transfer function of the whole of the readout path from photodiodes to IMAGEREF[7:0] and IMAGESIG[7:0] pins, by using a test mode:

Set any one or two half-row addresses from the normal row address range in Table 9 and drive the corresponding PIX_TRA_L/R to low and PIX_SEL_L/R to high.

Then drive VREFR alternately to each of two levels, with pulses on corresponding PIX_RST_L/R and then PIX_SHR at one VREFR level and pulses on corresponding PIX_RST_L/R and then PIX_SHS at the other level to put the effect of both VREFR levels on vr_odd/even and vs_odd/even (see Figure 5).

These levels are then output on IMAGEREF[7:0] and IMAGESIG[7:0] when PIX_BUF_LOAD changes state and any column address is set.

By repeating this process for a range of values for the change on VREFR the transfer function can be plotted.

Column addresses

As described in the section TIMING INFORMATION and shown in Figure 11, the eight-bit column addresses are loaded by signals COL_CLK, COL_SER_IN_[7:0] and COL_LOAD for the eight blocks of columns or channels. Each channel is addressed separately, using one of the COL_SER_IN_[7:0] data bits as a serial stream.

As shown in Figure 16, the column numbering is from right to left, as is common for back thinned image sensors – in the design database the order is drawn left to right, then the back thinning results in a left – right flip.

Binary coded values are used, with each set of 240 column addresses as in Table 10.

Column addresses from 11110000 to 11111110 select no signal path, so each IMAGEREF[7:0] and IMAGESIG[7:0] will be driven to an internally set level around mid-way between VANA_OUT_L/M/R and AGND_OUT_L/M/R.

Column address 11111111 is used to pre-charge the outputs of the column selectors (see Figure 5) such that the first column to be output in any group of columns will have a similar starting point to the others in that group and so have a very similar settling characteristic. At power-on or after a CHIP_RST pulse all column address registers will be set to 11111111.

Any of the eight col_addr_reg_[7:0] serial words	**Selection**
00000000	Column 0 (right of block)
00000001	Column 1
00000010	Column 2
00000011	Column 3
⋮	⋮
11101110	Column 238
11101111	Column 239 (left of block)
11110000	None
⋮	⋮
11111110	None
11111111	Pre-charge mode

Table 10: Binary codes for BSI column addresses.

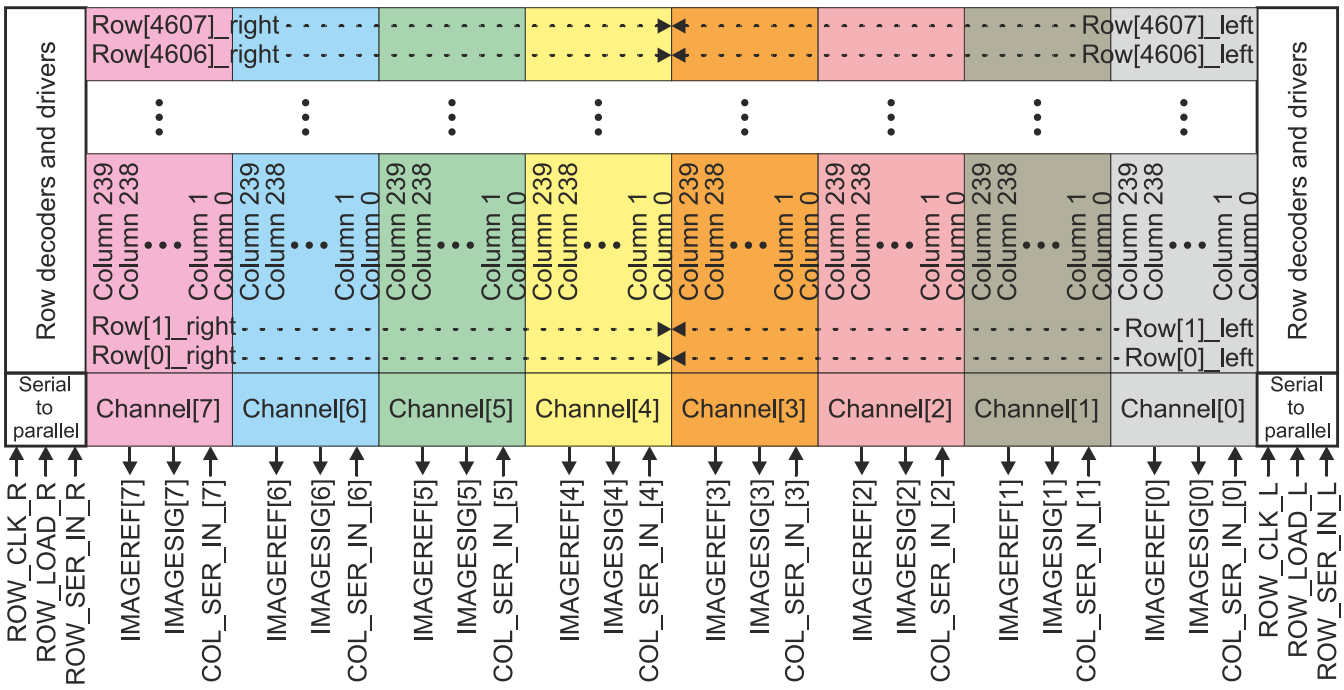

Figure 16: Numbering of BSI CIS113 rows and columns.

As can be seen in Figure 11 and Figure 16, the column number data COL_SER_IN_[7:0] is a set of serial data words, not a parallel bus. When outputs from only some of the blocks of columns, called Channels in Figure 16, are required, the other bits in COL_SER_IN_[7:0] will select a column for their channel. A suggested value for these channels is to load 11111111 in order to set the levels to a mid-point and be ready for when a column in that channel is required.

TEST MODES

There are several test features in CIS113 to improve test in the e2v factory. These are not intended for customer use and should be set to a safe state by holding the pins ATEST1, ATEST2, TEST_ENABLE, TEST_IN1, TEST_IN2 and TEST_IN3 at ground (0.0 V) and allowing TEST_DIGITAL_OUT to float.

ELECTRICAL and MECHANICAL INTERFACE

Package detail

To allow the construction of a mosaic of CIS113 image sensors to give a large focal plane, the package is specially designed for three-side butting with very little loss of pixel area at the joins. The package is a combination of a 76 pin ceramic PGA and an invar block with mounting and guide pins, as in Figure 17:

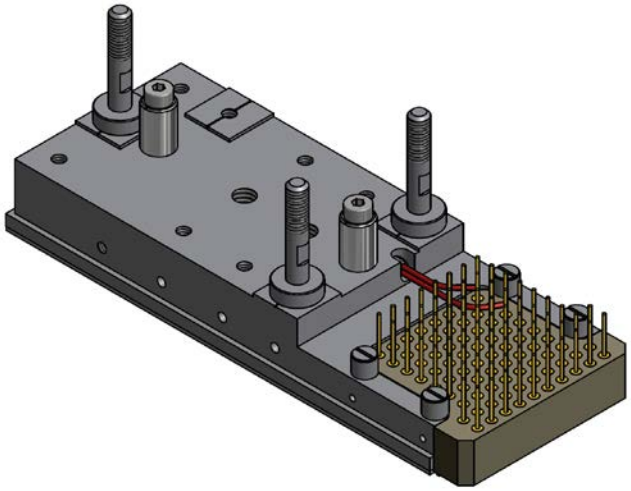

Figure 17: Underside of package.

Figure 17 shows the three M3 threaded studs for final attachment to the focal plane. These also have precision machined shims to set the height of the sensor surface to a known distance from the mounting plane.

Two precision circular pins are shown near each end of the thicker part of the invar block. One is used to set the X/Y position and the other to set the angular location when fitting the sensors into a mosaic.

Two M4 tapped holes can be seen; the one nearer the PGA and partly hidden by a threaded stud is for a handling rod to help pull the CIS113 into the focal plane, the other is to take a guide rod to help set the initial orientation.

Full mechanical drawings are available on request.

Mechanical details

Image area: 30.72 mm × 73.73 mm.

Die size: 31.6 mm × 76.5 mm.

Total package size: 31.70 mm × 82.34 mm.

Pixel height above mounting plane: 14.00 ± 0.02 mm.

Flatness and tilt: included in total pixel height tolerance.

Package dimensions

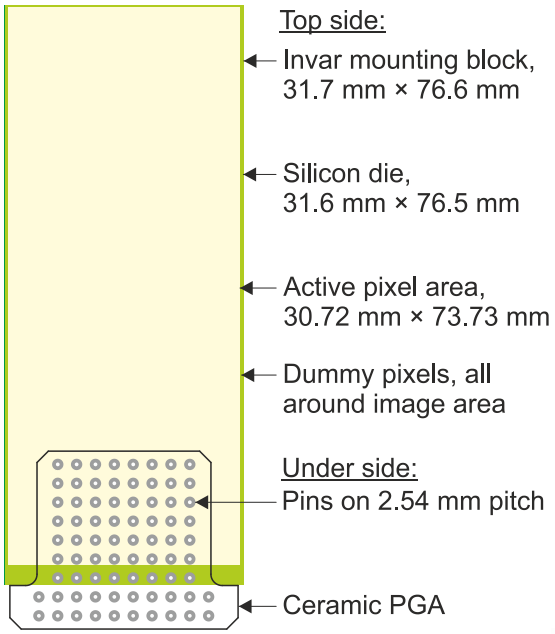

Figure 18: Nominal dimensions of package.

It can be seen from the dimensions in Figure 18 that on three sides the silicon die is inset from the invar block by only 50 µm (nominal). Great care must be exercised when handling this image sensor. Similarly, the wire bonds from the silicon die to the ceramic PGA are above the surface of the silicon and must not be touched.

Appropriate tools and procedures should be used when transferring this image sensor from the transport box and handling jig to the focal plane in the application – see the section HANDLING CIS113 near the end of this datasheet.

Positions of the pixels

To give the locations of the pixels there are two crosses on the front surface of the silicon with 200 µm square holes in the back side to allow them to be seen. These are at each end of the silicon edge with the wire bonds to the PGA. Coordinates of the pixel array relative to the centres of these crosses are given in Figure 19 in micrometres.

This uses the centre of the bottom edge of the pixel array as the reference point (0, 0) and then the positions from this point to the four corners of the pixel array and to the two aligment crosses.

The centre of the pixel array is at (0, 36864).

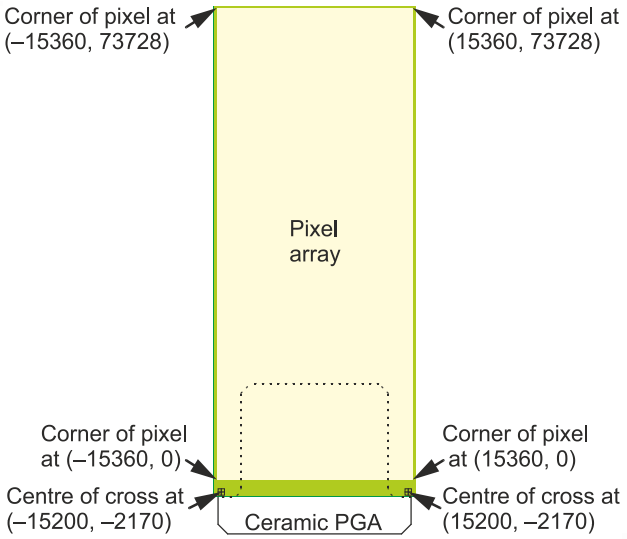

Figure 19: Coordinates of pixels (in µm).

Pin numbering on package

Pin numbering on a PGA is given as an alpha-numeric combination, for the CIS113 the rows and columns are labelled as in Figure 20:

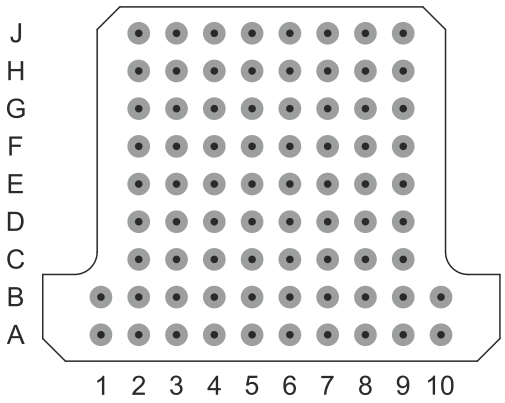

Figure 20: Package pin numbering (top view).

Figure 20 shows the pin numbering viewed from image input side, with pins behind. Each pin has the name and function as described in Table 11.

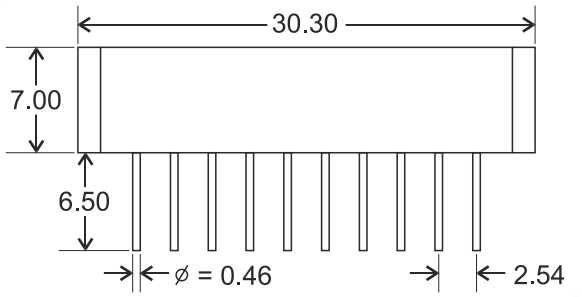

Figure 21: End view of ceramic (dimensions in mm).

Dimensions in Figure 21 are nominal. Fired ceramic changes its thickness during the process, so there is a ±10 % tolerance on the 7.00 mm height of the ceramic body. Note that the nominal width of the ceramic is less than that of the invar block to be certain of the three side butting.

Suitable sockets include the 10 × 10 pin 3M™ Textool™ type 200-6310-9UN-1900 (also listed as 3M5066) zero insertion force socket, ideally with only the required 76 contacts fitted. With the width of package used for CIS113 some users can prefer to adjust the angle of the socket clamping lever before assembly.

For delivery a dedicated transport box and handling jig is used to hold the CIS113 securely by its mounting holes. See the section HANDLING CIS113 near the end of this datasheet for a reference to a document with pictures of the transport box.

Pin list

Pin No.	Name	Description
A1	VDIG_R	Digital row and column decoder supply (left)
A2	ROW_CLK_R	Row address serial clock (left)
A3	ROW_LOAD_R	Row address load (left)
A4	PIX_SHR	Sample and hold reset level (left and right)
A5	COL_LOAD	Column address load (all segments)
A6	COL_CLK	Column address serial clock (all segments)
A7	PIX_SHS	Sample and hold signal level (left and right)
A8	ROW_LOAD_L	Row address load (right)
A9	ROW_CLK_L	Row address serial clock (right)
A10	VDIG_L	Digital row and column decoder supply (right)
B1	DGND_R	Digital row and column decoder ground (left)
B2	ROW_SER_IN_R	Row address serial data (left)
B3	PIX_TRA_R	Pixel charge transfer control (left)
B4	COL_SER_IN[4]	Column address serial data (channel 4)
B5	PIX_RST_R	Pixel sense node reset (left)
B6	PIX_RST_L	Pixel sense node reset (right)
B7	COL_SER_IN[3]	Column address serial data (channel 3)
B8	PIX_TRA_L	Pixel charge transfer control (right)
B9	ROW_SER_IN_L	Row address serial data (right)
B10	DGND_L	Digital row and column decoder ground (right)
C2	COL_SER_IN[7]	Column address serial data (channel 7)
C3	PIX_SEL_R	Pixel select (left)
C4	COL_SER_IN[5]	Column address serial data (channel 5)
C5	COL_SER_IN[6]	Column address serial data (channel 6)
C6	COL_SER_IN[1]	Column address serial data (channel 1)
C7	COL_SER_IN[2]	Column address serial data (channel 2)
C8	PIX_SEL_L	Pixel select (right)
C9	COL_SER_IN[0]	Column address serial data (channel 0)
D2	TEST_IN1	Only for test at e2v. Tie to ground
D3	IOUTPUT	Bias current to output drivers
D4	AGND_OUT_R	Analogue output driver ground (left)
D5	VANA_OUT_R	Analogue output driver supply (left)
D6	VANA_OUT_L	Analogue output driver supply (right)
D7	AGND_L	Analogue readout ground (right)
D8	PIX_RST_GLOBAL	Drive to global reset transistor in all pixels. Acts on selected half rows if PIX_GLB_SHUTTER is at low or on all half rows if PIX_GLB_SHUTTER is at high. Also used for anti-blooming if tied to ground.
D9	PIX_LOAD_BUF	Selects odd or even channels for sampling or output
E2	TEST_IN2	Only for test at e2v. Tie to ground
E3	VRESET	Supply to reset gate drivers (all)
E4	AGND_R	Analogue readout ground (left)
E5	VANA_R	Analogue readout supply (left)
E6	VANA_L	Analogue readout supply (right)
E7	AGND_OUT_L	Analogue output driver ground (right)
E8	VDDTRA	Supply to transfer gate drivers (all)

Pin No.	Name	Description
E9	CHIP_RST	Active low – sets all column addresses to 11111111 and both row addresses to 1111111111111. Tie to VDIG_L/R if not required.
F2	TEST_IN3	Only for test at e2v. Tie to ground
F3	AGND_OUT_M	Analogue output driver ground (middle)
F4	IMAGEREF[7]	Reference level output (channel 7)
F5	IMAGESIG[7]	Signal level output (channel 7)
F6	IMAGEREF[0]	Reference level output (channel 0)
F7	IMAGESIG[0]	Signal level output (channel 0)
F8	VANA_OUT_M	Analogue output driver supply (middle)
F9	PIX_GLB_SHUTTER	Active high – Bypasses row address selection for global reset, reset and transfer gate in every pixel to give synchronous global shutter. Tie to ground if not required.
G2	TEMP_1	PT100 temperature sensor
G3	VREFR	Supply to pixel reset transistors (all)
G4	IMAGEREF[6]	Reference level output (channel 6)
G5	IMAGESIG[6]	Signal level output (channel 6)
G6	IMAGEREF[1]	Reference level output (channel 1)
G7	IMAGESIG[1]	Signal level output (channel 1)
G8	VPIX	Supply to pixel amplifiers (all)
G9	CHIP_ENABLE	Enables bias current to all analogue sections.
H2	TEST_DIGITAL_OUT	Only for test at e2v. Leave open circuit.
H3	IPIX	Bias current to pixel columns
H4	IMAGEREF[5]	Reference level output (channel 5)
H5	IMAGESIG[5]	Signal level output (channel 5)
H6	IMAGEREF[2]	Reference level output (channel 2)
H7	IMAGESIG[2]	Signal level output (channel 2)
H8	ASUB	Analogue ground to substrate
H9	TEST_ENABLE	Only for test at e2v. Tie to ground
J2	TEMP_2	PT100 temperature sensor
J3	IREAD	Bias current to read circuits
J4	IMAGEREF[4]	Reference level output (channel 4)
J5	IMAGESIG[4]	Signal level output (channel 4)
J6	IMAGEREF[3]	Reference level output (channel 3)
J7	IMAGESIG[3]	Signal level output (channel 3)
J8	ATEST2	Only for test at e2v. Tie to ground
J9	ATEST1	Only for test at e2v. Tie to ground

Table 11: BSI pin list and functions.

TEMPERATURE SENSOR

To help achieve good control of temperature, a PT100 sensor is fixed in a cavity in the underside of the invar block in a position near the pins of the PGA. It is connected to pins G2 and J2.

Characteristics of this sensor are:

Resistance at 0 °C = 100 Ω ± 0.30 Ω.

Temperature coefficient (α) = +0.385 %/°C.

ELECTRICAL INTERFACE CHARACTERISTICS

In this table V_{DIG} refers to the level of VDIG_L and VDIG_R for row or column address selection. V_{ANA} refers to the level of VANA_L and VANA_R for the control signals for pixel and readout timing (CHIP_ENABLE, PIX_RST_GLOBAL, PIX_GLB_SHUTTER, PIX_RST_L/R, PIX_SEL_L/R, PIX_SHR, PIX_TRA_L/R, PIX_SHS, PIX_LOAD_BUF, CHIP_RST). Limits for current biases IPIX, IREAD and IOUTPUT are given in Table 8.

Symbol	Parameter	Value			Unit
		Min	Typical	Max	
V_{DIG_INL}	Address input voltage low level	−0.3	~ 0.0	0.3 × V_{DIG}	V
V_{DIG_INH}	Address input voltage high level	0.7 × V_{DIG}	~ V_{DIG}	V_{DIG} + 0.3	V
C_{DIG_IN}	Digital input pin capacitance			3	pF
I_{DIG_LEAK}	Digital input pin leakage current	−10		10	µA
V_{ANA_INL}	Control signal input voltage low level	−0.3	~ 0.0	0.3 × V_{ANA}	V
V_{ANA_INH}	Control signal input voltage high level	0.7 × V_{ANA}	~ V_{ANA}	V_{ANA} + 0.3	V
C_{ANA_IN}	Control input pin capacitance			3	pF
I_{ANA_LEAK}	Control input pin leakage current	−10		10	µA
C_{LOAD}	External capacitance on each of IMAGEREF[7:0] and IMAGESIG[7:0], for operation at 2 MP/s per channel			10	pF
V_{OUT_REF}	Output voltage on IMAGEREF[7:0]		~3.1		V
V_{SIG_DARK}	Output voltage on IMAGESIG[7:0] in darkness		~3.1		V
V_{SIG_SAT}	Output voltage on IMAGESIG[7:0] at saturation		~1.3		V
P	Power dissipation in whole frame mode and with all settings at typical, measured at 20 °C. See note below.		30		mW

Table 12: Electrical interface characteristics.

Note: The power dissipated within a CMOS image sensor is a combination of the static dissipation of the buffers and the dynamic dissipation from the parallel buses and decoders. With IPIX, IREAD and IOUTPUT as in the typical column of Table 8 and all power supplies as in the typical column of Table 7, the total power is expected to be as given in Table 12.

Output buffers

All sixteen video output buffers are standard five transistor operational amplifiers connected as voltage followers, as in Figure 22:

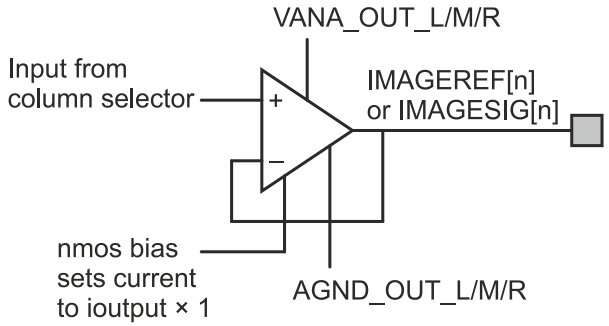

Figure 22: Output buffer structure.

These have the advantage over simple source follower output stages, as sometimes used for the analogue outputs on image sensors, of having an accurate unity voltage gain without significant extra noise, to give a better overall SNR.

Output buffer settling characteristics

To minimise the noise contribution due to the output buffers a low current design was chosen. This means the load capacitance must be kept very low if the typical or maximum pixel rate is required. Figure 23 shows the effect of adding a capacitor to the minimum load of CIS113 itself plus socket, PCB trace and 'scope probe to give total loads of 22 pF (dark blue), 37 pF (magenta), 69 pF (yellow) or 122 pF (cyan).

The settling time given in Table 1 applies with the minimum capacitance on the video outputs. If the external electronics must have a large input capacitance, a buffer between this image sensor and those electronics will help to maintain a high pixel readout rate.

When a low frame rate is adequate the high capacitance of some external electronics may be connected directly to the CIS113 to save adding a buffer.

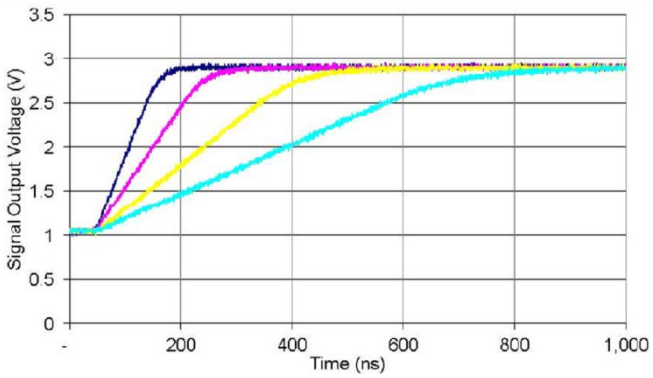

Figure 23: Typical settling characteristics.

ABSOLUTE MAXIMUM RATINGS

These are the limits which if exceeded are likely to cause permanent damage to the device. Operation at these limits is not expected. These limits apply with all ground pins (DGND_L, DGND_R, AGND_L, AGND_R, AGND_OUT_L, AGND_OUT_M, AGND_OUT_R and ASUB) at 0 V.

Symbol	Description or pins	Value			Unit
		Min	Typical	Max	
V_{DIG}	VDIG_L and VDIG_R	−0.5	1.8	2.2	V
V_{ANA}	VANA_L, VANA_R, VANA_OUT_L, VANA_OUT_M and VANA_OUT_R	−0.5	3.45	4.3	V
V_{PIX}	VPIX (source follower supply)	−0.5	2.9	4.3	V
V_{RESET}	VRESET (select and reset driver supply)	−0.5	3.45	4.3	V
V_{REFR}	VREFR (reset level supply)	−0.5	2.9	4.3	V
V_{TRA}	VTRA (transfer gate driver supply)	−0.5	3.45	4.3	V
V_{INH}, V_{INL}	Digital input signals	−0.5	0 to V_{DIG}	V_{DIG} + 0.5	V
V_{BIAS}	Voltage on IPIX, IREAD or IOUTPUT	0.0		3.6	V
T_{STORE}	Storage temperature	−120	–	+100	°C
T_{SOLDER}	Soldering temperature – see note below.	–	–	–	°C
	ESD protection, bare imager, all pins (HBM)	−2		+2	kV

Table 13: Absolute maximum ratings.

Note: Soldering temperature limits are not given as this device is expected to be used in a ZIF socket.

POWER UP or POWER DOWN

When powering the device up or down, it is critical that the absolute maximum ratings in Table 13 are met at all times, including the input signal to supply and ground limits. To ensure safe and consistent start-up a recommended sequence is:

(1) Hold all set-up and control signals (ROW_SER_IN_L/R, ROW_CLK_L/R, ROW_LOAD_L/R, COL_SER_IN[7:0], COL_CLK, COL_LOAD, CHIP_ENABLE, PIX_RST_GLOBAL, PIX_GLB_SHUTTER, PIX_RST_L/R, PIX_SEL_L/R, PIX_SHR, PIX_TRA_L/R, PIX_SHS, PIX_LOAD_BUF and CHIP_RST) at low (ground) and IPIX, IREAD and IOUTPUT at nil current (this is also at ground as the polarity is to source current into the imager).

(2) Drive all supplies (VDIG_L/R, VANA_L/R, VANA_OUT_L/M/R, VPIX, VREFR, VRESET and VDDTRA to their correct levels in any convenient order.

(3) Set IPIX, IREAD and IOUTPUT to the correct currents.

(4) Set CHIP_ENABLE high to pass bias currents to analogue blocks. A propagation delay of up to 200 µs is expected from CHIP_ENABLE going high to all circuits being active and ready to image.

(5) Set CHIP_RST to high and use ROW_SER_IN_L/R, ROW_CLK_L/R and ROW_LOAD_L/R to select two half rows.

(6) Use all of PIX_TRA_L/R and PIX_RST_L/R to clear any accumulated charge.

(7) Repeat (5) and (6) to reset whole imager.

To then capture images in rolling shutter mode:

Keep CHIP_ENABLE and CHIP_RST at high, PIX_RST_GLOBAL and PIX_GLB_SHUTTER at low and toggle PIX_LOAD_BUF between rows as in Figure 6 to Figure 9.

(8) Use ROW_SER_IN_L/R, ROW_CLK_L/R and ROW_LOAD_L/R to address two half rows.

(9) Use PIX_SEL_L/R, PIX_RST_L/R, PIX_TRA_L/R, PIX_SHR and PIX_SHS to read a row.

(10) Use COL_SER_IN[7:0], COL_CLK and COL_LOAD to select and output each required column in turn.

(11) Use external subtraction of IMAGESIG[7:0] from IMAGEREF[7:0] to remove kTC noise from the image. A differential amplifier is a convenient method for this subtraction.

(12) Repeat steps (8) to (11) to read a whole image or use reduced ranges of row and/or column addresses for one or more ROI.

To shut down cleanly:

After all required images have been captured:

(13) Set all set-up and control signals to low and then CHIP_ENABLE low to stop bias currents to analogue blocks.

(14) Set IPIX, IREAD and IOUTPUT to nil current.

(15) Drive all supplies to ground in any convenient order.

To shut down abruptly it is permitted to do (13), (14) and (15) simultaneously or in any order without damage, but the reset in lines (5) to (7) will be essential at next power-up.

HANDLING CMOS SENSORS

CMOS image sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases, a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full antistatic handling precautions should be taken whenever using a CMOS sensor or module. These include:

Working at a fully grounded workbench

Operator wearing a grounded wrist strap

Evidence of incorrect handling will invalidate the warranty. All devices are provided with internal protection circuits on input, output and power pins.

The devices are assembled in a clean room environment. e2v technologies recommend that similar precautions are taken to avoid contaminating the active surface.

HANDLING CIS113

In addition to the general CMOS handling instructions above, there are specific unpacking instructions for the CIS113 and its transport box and handling jigs. These are given in guidance note DAS778019ZQ, available on request.

HIGH ENERGY RADIATION

Performance parameters will begin to change if the device is subject to high energy radiation. Characterisation data is held at e2v technologies with whom it is recommended that contact be made if devices are to be operated in any high radiation environment.

PART REFERENCE

CIS113-40-g-M16

g = cosmetic grade

M16 = specific part number for option described

VARIANTS

The M16 version is made on high resistivity epitaxial silicon and thinned to give a good balance of NIR QE and visible MTF. A “Mid-Band” AR coating is standard to give a good QE curve over the visible range and into the NIR. Other coatings (single and multi-layer) could be available as custom variants – see Figure 1 for the example of Multi-2 AR coating.

The 4608 rows are stitched, so alternative sizes (1152, 2304 or 3456) are possible with minimal redesign cost. These can be read in full frame mode at increased frame rates – up to 8 fps with 1152 rows.

A version with 12 µm square pixels is also possible at less cost than for a full new design.

Consult e2v technologies for further information on these options.

RoHS COMPLIANCE

Early production CIS113 used a lead based solder to connect the two temperature sensor leads to their PGA pins. This has now been replaced by conductive adhesive, so current production CIS113 are RoHS compliant.