CCD42-10 Back Illuminated
High Performance AIMO CCD Sensor

FEATURES

- 2048 by 512 pixel format
- 13.5 μm square pixels
- Image area 27.6 x 6.9 mm
- Wide Dynamic Range
- Symmetrical anti-static gate protection
- Back Illuminated Format for Enhanced Quantum Efficiency
- 3 Standard Anti-Reflection Coatings
- Advance Inverted Mode Operation (AIMO)
- Dump gate on readout register
- Zero Light Emitting Output Amplifier

APPLICATIONS

- Spectroscopy
- Scientific Imaging
- TDI Operation

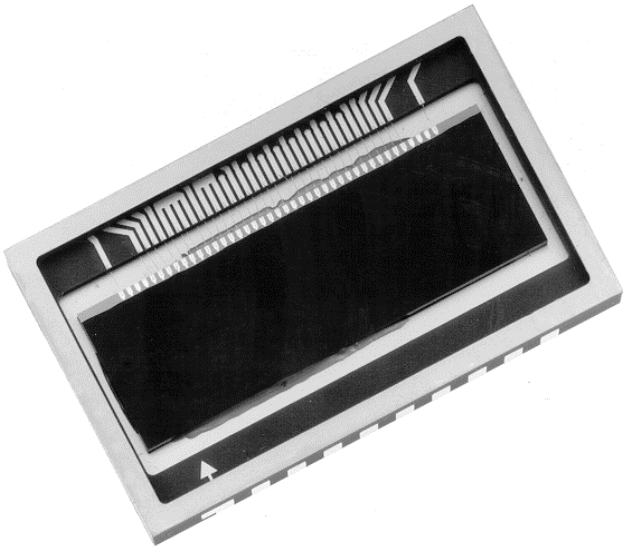
INTRODUCTION

This version of the CCD42 family of CCD sensors has full-frame architecture. Back illumination technology, in combination with an extremely low noise amplifier, make the device well suited to the most demanding applications, such as spectroscopy. To improve the sensitivity further, the CCD is manufactured without anti-blooming structures. This variant of the CCD42-10 operates in advanced inverted mode (AIMO) for use at Peltier temperatures. e2v technologies' AIMO structures give a 100 times reduction in dark current with minimum reduction in full-well capacity.

The output amplifier is designed to give excellent noise levels at low pixel rates, and can match the noise performance of most conventional scientific CCDs at pixel rates as high as 3 MHz.

The readout register has a gate controlled dump drain to allow fast dumping of unwanted data. The register is designed to accommodate four image pixels of charge, and a summing well capable of holding six image pixels is provided. The output amplifier has a feature enabling the responsivity to be reduced to allow the reading of such large charge packets.

Designers are advised to consult e2v should they be considering using CCD sensors in abnormal environments or if they require customised packaging.



TYPICAL PERFORMANCE

(Low noise mode)

Pixel readout frequency	20 – 3000 kHz
Output amplifier sensitivity	4.5 μV/e^-
Peak signal	100 ke^-/pixel
Dynamic range	33,333:1
Spectral range	200 – 1060 nm
Readout noise (at 233 K, 20 kHz)	3 e^- rms

GENERAL DATA

Format

Image area	27.6 x 6.9 mm
Active pixels	2048 (H) 515 (usable) (V)
Pixel size	13.5 x 13.5 μm

Package

Package size	32.89 x 20.07 mm
Number of pins	20
Inter-pin spacing	2.54 mm
Inter-row spacing	15.24 mm
Window material	Quartz or removable glass

e2v technologies (uk) limited, Waterhouse Lane, Chelmsford, Essex CM1 2QU United Kingdom Holding Company: e2v technologies plc
Telephone: +44 (0)1245 493493 Facsimile: +44 (0)1245 492492
Contact e2v by e-mail: enquiries@e2v.com or visit www.e2v.com for global sales and operations centres.

PERFORMANCE

			Min	Typical	Max	Units	Note
Peak charge storage				100k		e^-/pixel	1
Peak output voltage (unbinned)				450		mV	
Dark signal at 293 K				250	500	e^-/pixel/s	2
Charge transfer efficiency		Parallel	-	99.9999	-	%	1, 3
		Serial	-	99.9993	-	%	
Output amplifier sensitivity	Low noise mode		3.0	4.5	6.0	µV/e^-	
	High signal mode			1.5			1
Readout noise at 253 K	Low noise mode			3	4	rms e^-/pixel	4
	High signal mode			6			
Readout frequency				20	3000	kHz	5
Dark signal non-uniformity at 293 K (std. deviation)				60	-	e^-/pixel/s	1
Binned column dark signal non-uniformity at 293 K (std. deviation)				7	15	e^-/pixel/s	
Output node capacity relative to image section	Low noise mode			1.5			
	High signal mode			6.0			

SPECTRAL RESPONSE

Wavelength (nm)	Minimum Response (QE)						Response Non-uniformity (1σ)	
	Enhanced Process			Basic Process				
	Broadband Coated	Mid-band Coated	UV Coated	Broadband Coated	Mid-band Coated	Uncoated		
300	-	-	45	-	-	-	-	%
350	50	25	45	25	15	10	5	%
400	80	50	55	55	40	25	3	%
500	80	85	60	75	85	55	3	%
650	72	85	60	72	85	50	3	%
900	25	25	25	25	25	25	5	%

ELECTRICAL INTERFACE CHARACTERISTICS

Electrode Capacitances (Measured at mid-clock level)

	Min	Typical	Max	
I∅/I∅ interphase	-	5	-	nF
R∅/R∅ interphase	-	80	-	pF
I∅/SS	-	15	-	nF
R∅/SS	-	150	-	pF
Output impedance	-	350	-	Ω

NOTES

1. Not measured as production test.
2. The typical average (background) dark signal at any temperature T (kelvin) between 230 K and 300 K is given by:

   $$Q_d/Q_{d0} = 1.14 \times 10^6 T^3 e^{-9080/T}$$

   where Q_{d0} is the dark signal at 293 K. Note that this is typical performance and some variation may be seen between devices. Below 230 K additional dark current components with a weaker temperature dependence may become significant.
3. CCD characterisation measurements made using charge generated by X-ray photons of known energy.
4. Measured at OS with correlated double sampling at 20 kHz pixel rate in low noise mode.
5. Readout above 3000 kHz can be achieved but performance to the parameters given cannot be guaranteed.

BLEMISH SPECIFICATION

Traps Pixels where charge is temporarily held. Traps are counted if they have a capacity greater than 200 e^-.

Black spots Are counted when they have a signal level of less than 80% of the local mean signal.

White spots Are counted when they have a generation rate 100 times the specified maximum dark signal generation rate at 293 K (measured between 233 and 273 K). The typical temperature dependence of white spot blemishes is different from that of the average dark signal and is given by:

$$Q_d/Q_{d0} = 122T^3e^{-6400/T}$$

White column A column which contains at least 9 white defects.

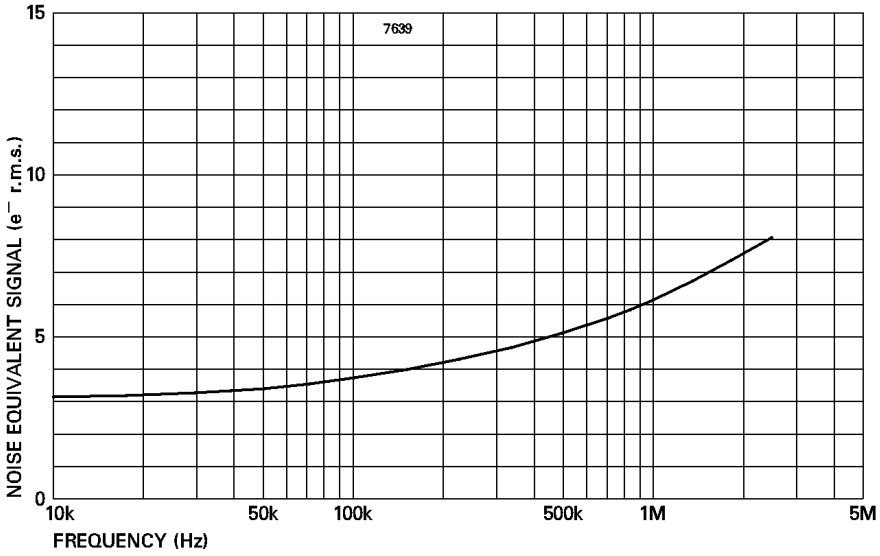
Black column A column which contains at least 9 black defects.

Spikes Are measured with the image fully binned into the register. Level 1 spikes are those above 50 k e^-/column. Level 2 spikes are those above 200 k e^-/column.

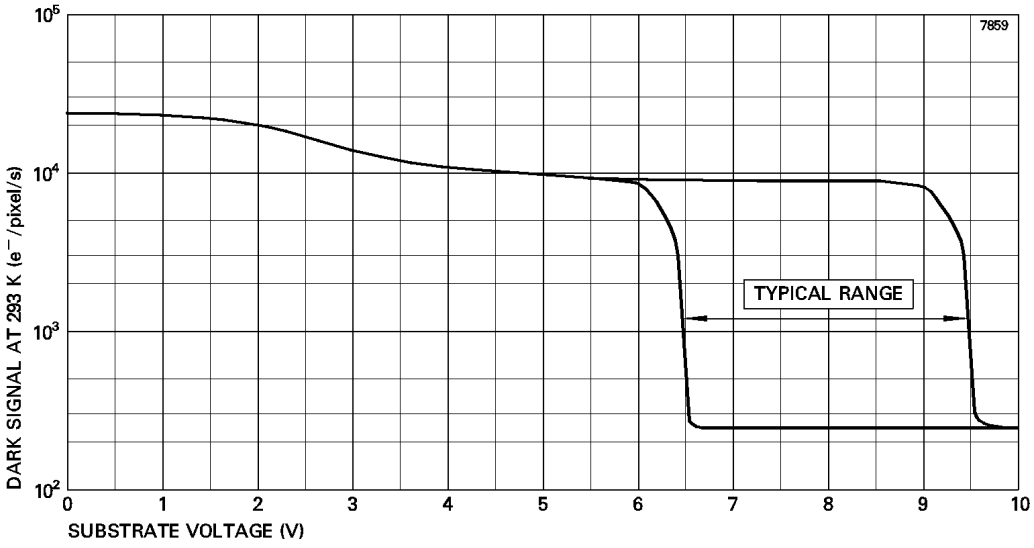
GRADE	0	1	2
Column defects: black white	 0 0	 1 0	 6 0
Black spots	40	80	200
Traps >200 e^-	1	2	5
White spots	20	30	50
Level 1 spikes	15	20	30
Level 2 spikes	3	4	6

Note: The effect of temperature on defects is that traps will be observed less at higher temperatures but more may appear below 233 K. The amplitude of white spots and columns will decrease rapidly with temperature.

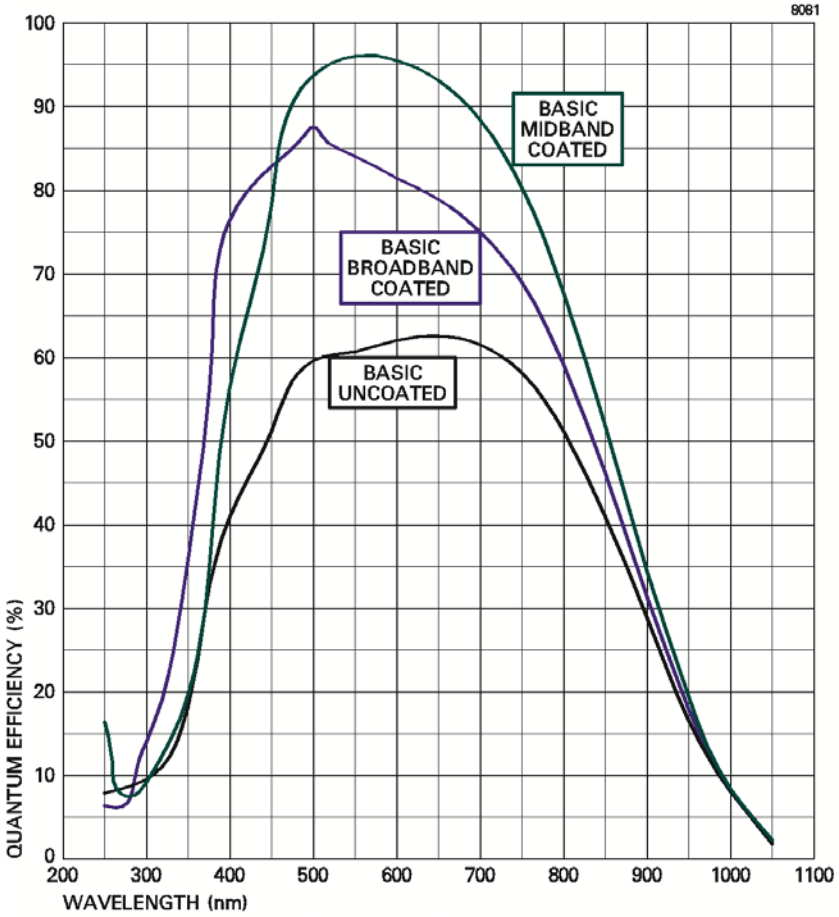
TYPICAL OUTPUT CIRCUIT NOISE (Measured using clamp and sample)

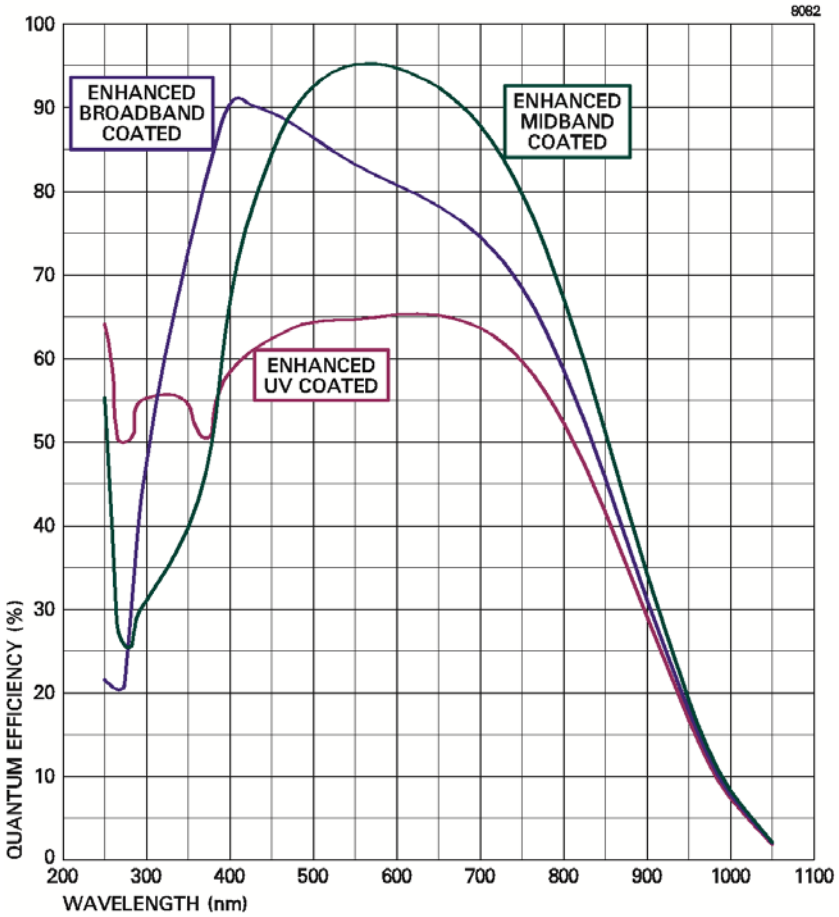


TYPICAL VARIATION OF DARK SIGNAL WITH SUBSTRATE VOLTAGE

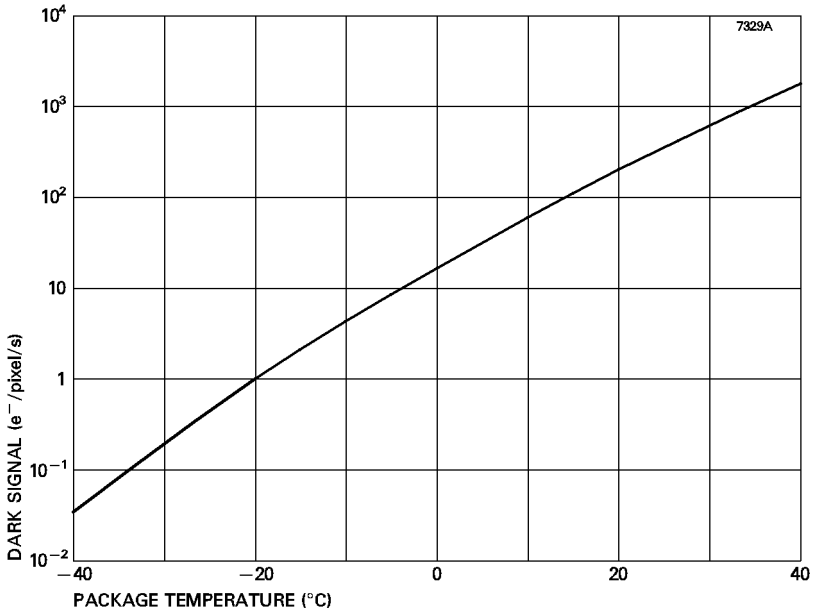


TYPICAL SPECTRAL RESPONSE (At –20 °C, no window)

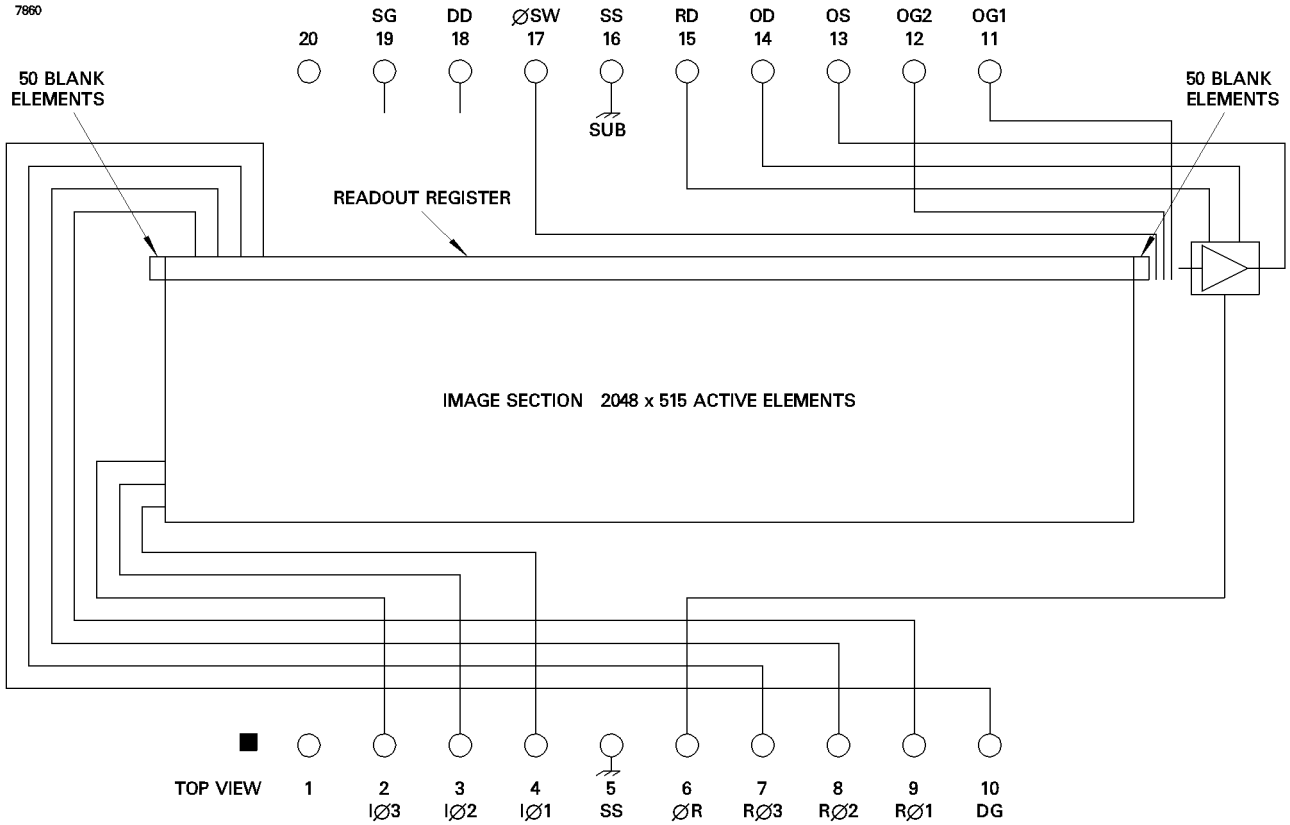




TYPICAL VARIATION OF DARK SIGNAL WITH TEMPERATURE



DEVICE SCHEMATIC



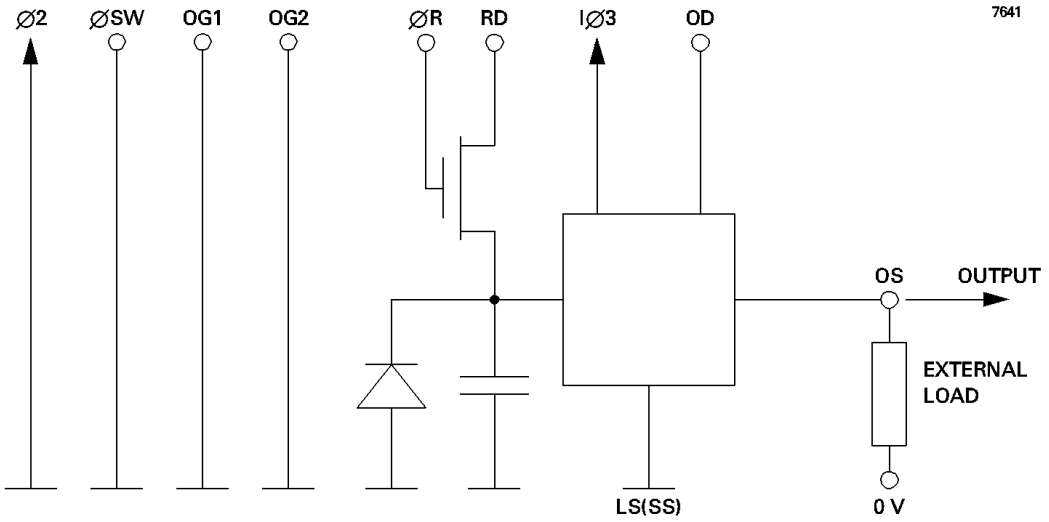
CONNECTIONS, TYPICAL VOLTAGES AND ABSOLUTE MAXIMUM RATINGS

PIN	REF	DESCRIPTION	PULSE AMPLITUDE OR DC LEVEL (V) (see note 6)			MAXIMUM RATINGS with respect to V_{SS}
			Min	Typical	Max	
1	-	No connection		-		-
2	I∅3	Image section, phase 3 (clock pulse)	8	12	15	±20 V
3	I∅2	Image section, phase 2 (clock pulse)	8	12	15	±20 V
4	I∅1	Image section, phase 1 (clock pulse)	8	12	15	±20 V
5	SS	Substrate	8	9.5	11	-
6	∅R	Output reset pulse	8	12	15	±20 V
7	R∅3	Readout register, phase 3 (clock pulse)	8	12	15	±20 V
8	R∅2	Readout register, phase 2 (clock pulse)	8	12	15	±20 V
9	R∅1	Readout register, phase 1 (clock pulse)	8	12	15	±20 V
10	DG	Dump gate (see note 7)	-	0	-	±20 V
11	OG1	Output gate 1	2	3	4	±20 V
12	OG2	Output gate 2 (see note 8)	-	OG1 + 1 V	-	±20 V
13	OS	Output transistor source		see note 9		–0.3 to +25 V
14	OD	Output drain	27	29	32	–0.3 to +25 V
15	RD	Reset transistor drain	15	17	19	–0.3 to +25 V
16	SS	Substrate	8	9.5	11	-
17	∅SW	Summing well (see note 10)	8	12	15	±20 V
18	DD	Diode drain	22	24	26	–0.3 to +25 V
19	SG	Spare gates	0	0	V_{SS} + 19	±20 V
20	-	No connection		-		-

If all voltages are set to the typical values, operation at or close to specification should be obtained. Some adjustment within the range specified may be required to optimise performance.

Maximum voltages between pairs of pins: OS to OD ± 15 V
Maximum current through any source or drain pin: 10 mA

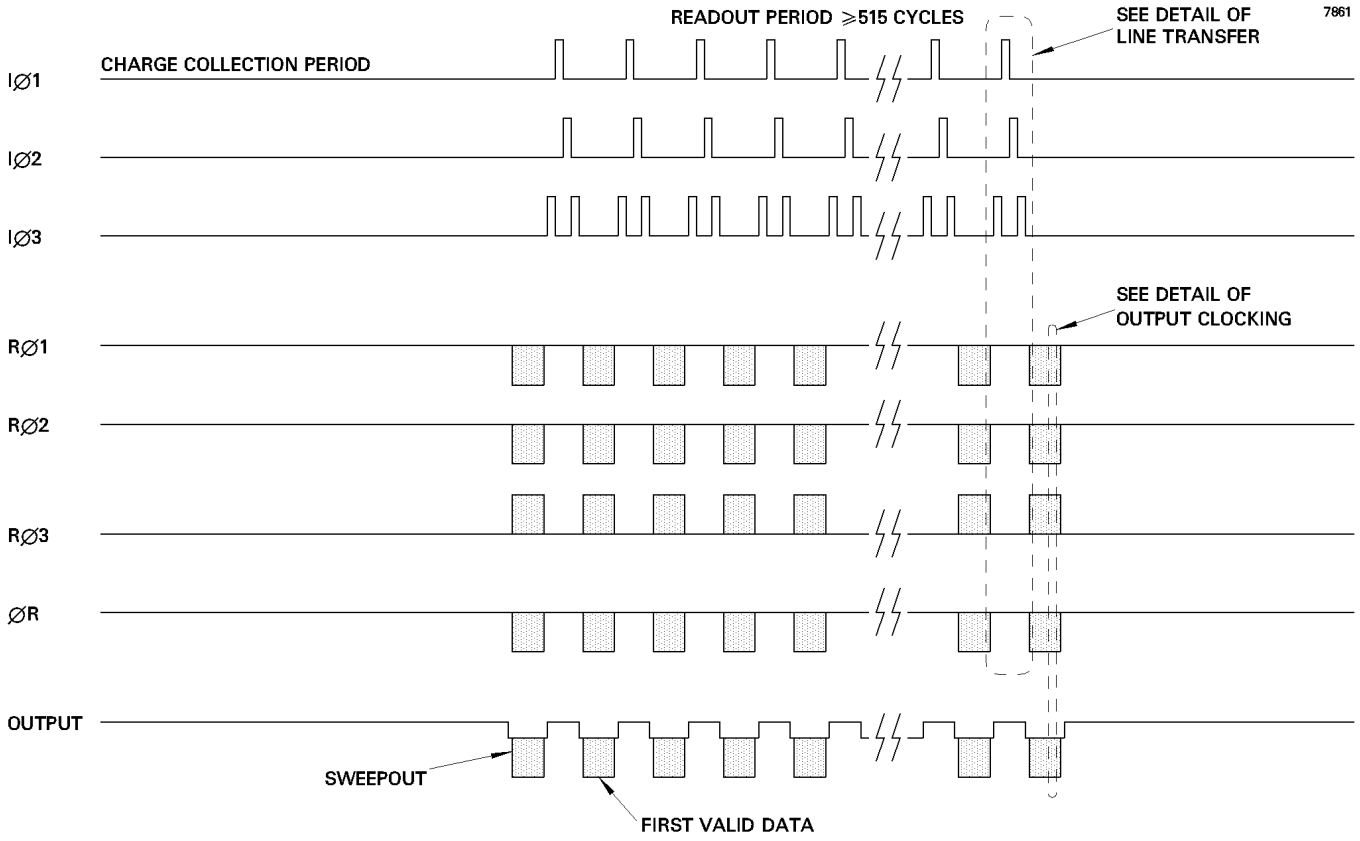
OUTPUT CIRCUIT



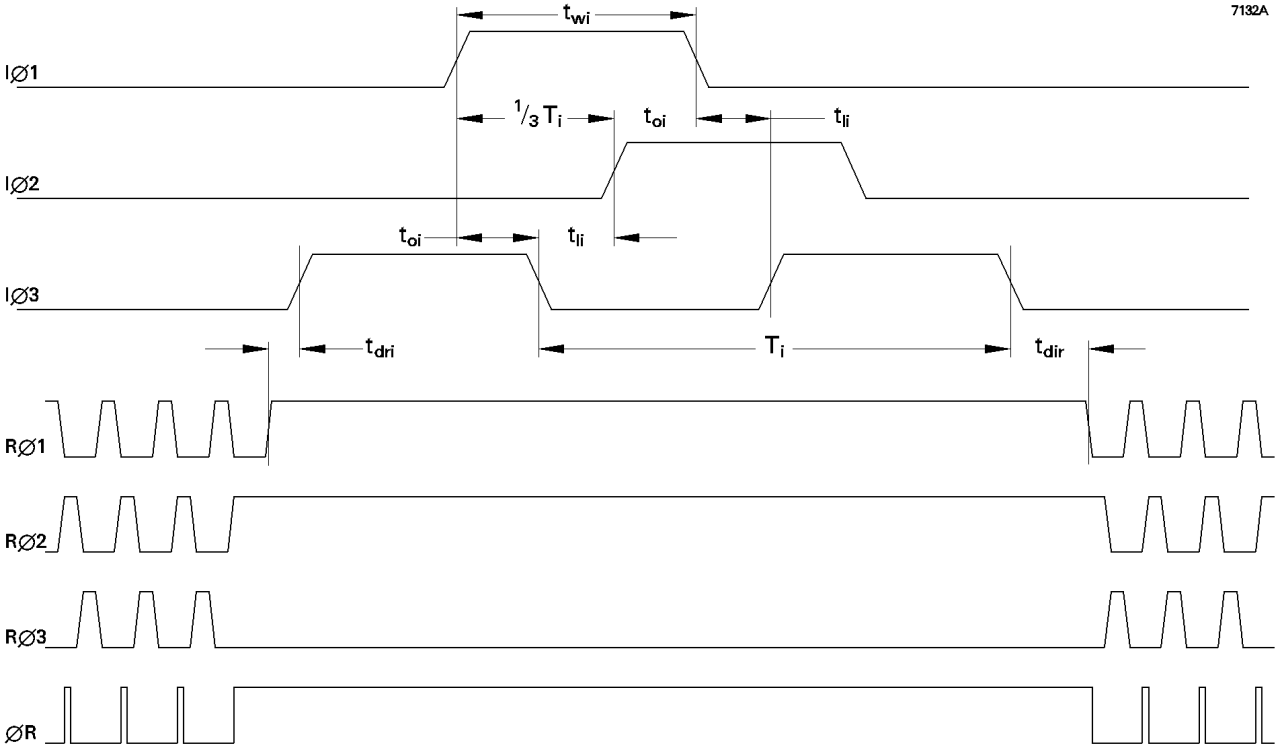
NOTES

6. Readout register clock pulse low levels + 1 V; other clock low levels 0 ± 0.5 V.
7. Non-charge dumping level shown. For charge dumping, DG should be pulsed to 12 ± 2 V.
8. Use OG2 = OG1 + 1 V for normal, low noise mode, or 20 V for low responsivity, high signal mode.
9. Not critical; can be a 1 -- 5 mA constant current source, or 5 -- 10 kΩ resistor.
10. For normal operation, the summing well should be clocked as R∅3.
11. The amplifier has a DC restoration circuit, which is activated internally whenever I∅3 is pulsed high

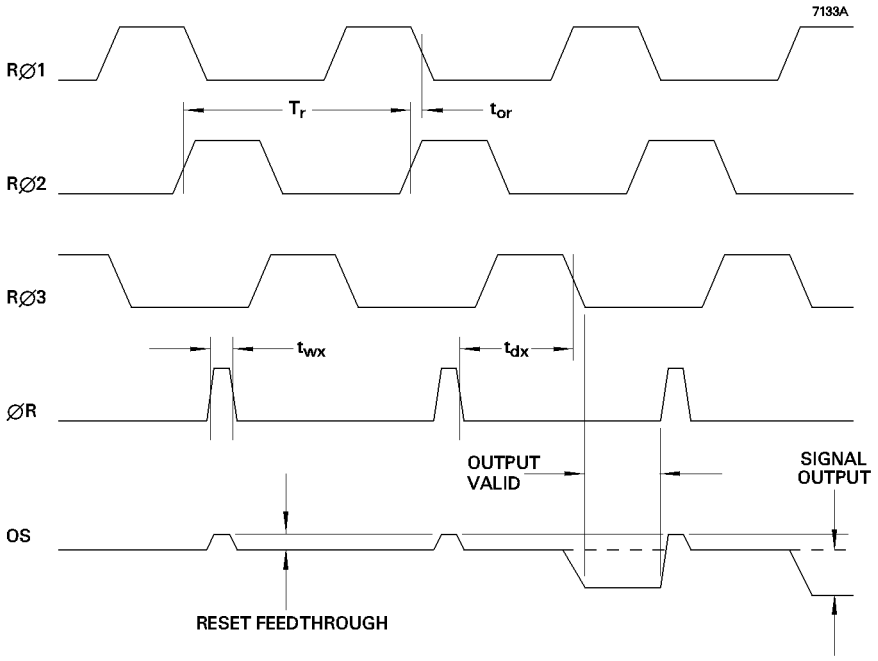
FRAME READOUT TIMING DIAGRAM



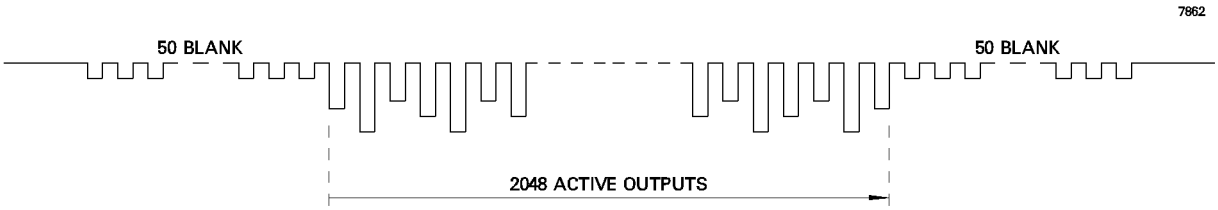
DETAIL OF LINE TRANSFER



DETAIL OF OUTPUT CLOCKING (Operation through both outputs)



LINE OUTPUT FORMAT (Split read-out operation)



CLOCK TIMING REQUIREMENTS

Symbol	Description	Min	Typical	Max	
T_i	Image clock period	15	30	see note 12	µs
t_{wi}	Image clock pulse width	7	15	see note 12	µs
t_{ri}	Image clock pulse rise time (10 to 90%)	0.5	2	$0.5t_{oi}$	µs
t_{fi}	Image clock pulse fall time (10 to 90%)	t_{ri}	2	$0.5t_{oi}$	µs
t_{oi}	Image clock pulse overlap	3	5	$0.2T_i$	µs
t_{li}	Image clock pulse, two phase low	3	5	$0.2T_i$	
t_{dir}	Delay time, I∅ stop to R∅ start	3	5	see note 12	µs
t_{dri}	Delay time, R∅ stop to I∅ start	1	2	see note 12	µs
T_r	Output register clock cycle period	333	see note 13	see note 12	ns
t_{rr}	Clock pulse rise time (10 to 90%)	50	$0.1T_r$	$0.3T_r$	ns
t_{fr}	Clock pulse fall time (10 to 90%)	t_{rr}	$0.1T_r$	$0.3T_r$	ns
t_{or}	Clock pulse overlap	20	$0.5t_{rr}$	$0.1T_r$	ns
t_{wx}	Reset pulse width	30	$0.1T_r$	$0.2T_r$	ns
t_{rx}, t_{fx}	Reset pulse rise and fall times	20	$0.5t_{rr}$	$0.2T_r$	ns
t_{dx}	Delay time, ∅R low to R∅3 low	30	$0.5T_r$	$0.8T_r$	ns

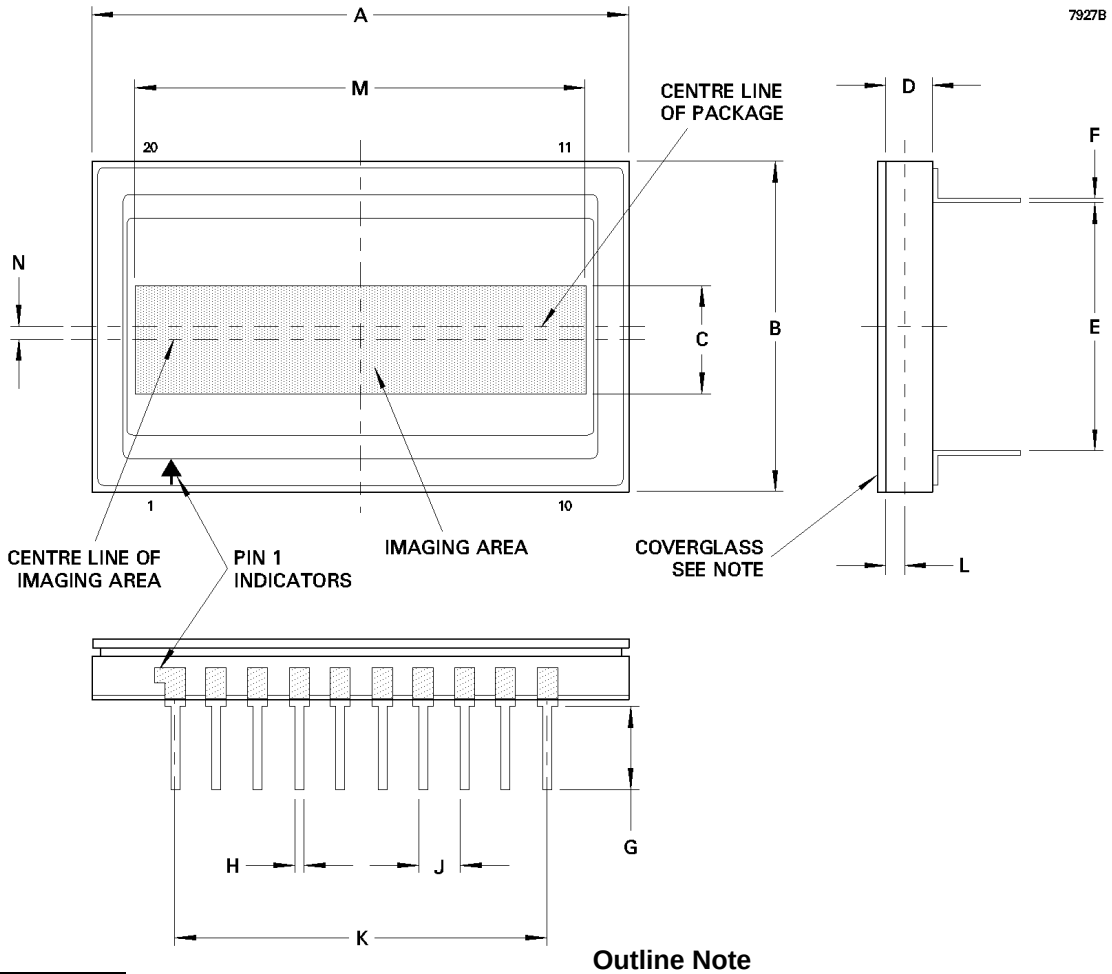
NOTES

12. No maximum other than that necessary to achieve an acceptable dark signal at the longer readout times.

13. As set by the readout period.

OUTLINES (All dimensions without limits are nominal)

Devices are not screened for compliance to the limits stated



Ref	Millimetres	
A	32.89 ± 0.38	
B	20.07 ± 0.25	
C	6.9	
D	2.79 ± 0.28	
E	15.24 ± 0.25	
F	0.254	+ 0.051
		− 0.025
G	5.2	
H	0.46 ± 0.05	
J	2.54 ± 0.13	
K	22.86 ± 0.13	
L	1.14 ± 0.25	
M	27.6	
N	0.8	

Outline Note

The device is normally supplied with a temporary glass window for protection purposes. It can also be supplied with a fixed, quartz or fibre-optic window where required.

ORDERING INFORMATION

Options include:

- Temporary quartz window
- Permanent quartz window
- Temporary glass window

For further information on the performance of these and other options, contact e2v.

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full antistatic handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving socket pins to be positively grounded
- Unattended CCDs should not be left out of their conducting foam or socket.

Evidence of incorrect handling will invalidate the warranty. All devices are provided with internal protection circuits to the gate electrodes (pins 2, 3, 4, 6, 7, 8, 9, 12, 19) but not to the other pins.

HIGH ENERGY RADIATION

Device parameters may begin to change if subject to ionising radiation.

Users planning to use CCDs in high radiation environments are advised to contact e2v.

TEMPERATURE LIMITS

	Min	Typical	Max	
Storage	153	-	373	K
Operating	153	233	323	K

Operation or storage in humid conditions may give rise to ice on the sensor surface on cooling, causing irreversible damage.

Maximum device heating/cooling .....5 K/min