e2v technologies

CCD39-01 Back Illuminated High Performance CCD Sensor

FEATURES

- 80 by 80 1:1 Image Format
- Image Area 1.92 x 1.92 mm
- Split-frame Transfer Operation
- 24 μm Square Pixels
- Symmetrical Anti-static Gate Protection
- Four High Performance Very Low Noise Output Amplifiers
- High Frame Rate Operation (up to 1000 fps)
- High Spectral Response
- 100% Active Area

APPLICATIONS

- Astronomy
- Scientific Imaging

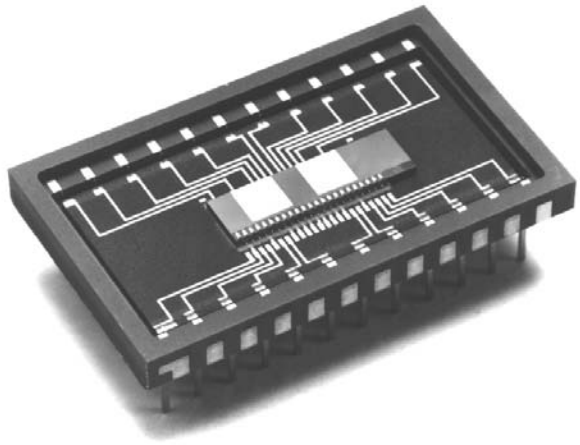
INTRODUCTION

The CCD39-01 is a small split-frame transfer device optimised for use at high frame rates which makes it particularly suited to the tracking of point source objects. To optimise the dynamic range, the sensitivity is maximised by combining back illumination technology with large pixels and non-antibloomed architecture. The noise floor of the chip is kept low by an advanced amplifier which permits operation at 1 MHz with noise levels typical of slow-scan operation. Dark signal noise is limited by cryogenic cooling or by an optional Peltier package which is sufficient for most applications when charge dithering effects are considered.

The device has split-frame transfer architecture with four amplifiers, each reading a block of 40 x 40 pixels.

The output circuit has a very small first-stage transistor to maximise the responsivity and minimise the noise, with only minimal loading from the much larger second-stage transistor, which provides a high level of drive capability. The connections to the circuit are identical to those of a single-stage type, the only difference being a standing current (1 mA) flowing in the substrate connection. There is no light emission to cause the generation of spurious charge.

Designers are advised to consult e2v technologies should they be considering using CCD sensors in abnormal environments or if they require customised packaging.



TYPICAL PERFORMANCE

Maximum readout frequency	>3	MHz
Output responsivity	4.5	$\mu V/e^-$
Peak signal	300	ke^-/pixel
Spectral range	200 - 1100	nm
Readout noise (at 20 kHz)	3	e^- rms
QE at 500 nm	90	%

GENERAL DATA

Format

Image area	1.92 x 1.92	mm
Active pixels (H)	80	
(V)	80 ± 4	
Pixel size	24 x 24	μm
Storage areas (x 2)	1.92 x 0.96 mm each	
Pixels (H)	80	
(V)	40	
Number of output amplifiers	4	

Package

Package size	32.89 x 20.07 mm
Number of pins	24
Inter-pin spacing	2.54 mm
Window material	quartz or removable glass
Type	ceramic DIL array

e2v technologies (uk) limited, Waterhouse Lane, Chelmsford, Essex CM1 2QU, UK Telephone: +44 (0)1245 493493 Facsimile: +44 (0)1245 492492
e-mail: enquiries@e2v.com Internet: www.e2v.com Holding Company: e2v technologies plc

e2v technologies inc. 4 Westchester Plaza, PO Box 1482, Elmsford, NY10523-1482 USA Telephone: (914) 592-6050 Facsimile: (914) 592-5148
e-mail: enquiries@e2vtechnologies-na.com

A1A-100036 Issue 6, March 2006

411/9572

PERFORMANCE

	Min	Typical	Max	
Peak charge storage (see note 1)	200k	300k	-	e^-/pixel
Peak output voltage (no binning)	-	1350	-	mV
Dark signal at 293 K (see notes 2 and 3)	-	75k	145k	e^-/pixel/s
Charge transfer efficiency (see note 4):				
parallel	-	99.9999	-	%
serial	-	99.9993	-	%
Output amplifier sensitivity (see note 3)	3	4.5	6	$\mu V/e^-$
Readout noise at 243 K (see notes 3 and 5)	-	3	4	rms e^-/pixel
Readout frequency	-	20	see note 6	kHz
Dark signal non-uniformity (std. deviation) (see notes 3 and 7)	-	7.5k	14.5k	e^-/pixel/s

Spectral Response (with standard AR coating)

Wavelength (nm)	Spectral Response Minimum	Typical	Maximum Response Non-uniformity (1σ)	
350	40	70	5	%
400	75	85	3	%
500	80	90	3	%
650	75	85	3	%
900	30	35	5	%

ELECTRICAL INTERFACE CHARACTERISTICS

Electrode capacitances (measured at mid-clock level):

	Min	Typical	Max	
I∅/I∅ interphase, S∅/S∅ interphase	-	50	-	pF
I∅/SS, S∅/SS	-	100	-	pF
R∅/R∅ interphase	-	7	-	pF
R∅/SS	-	20	-	pF
∅R/SS	-	10	-	pF
Output impedance (at typ. operating condition)	-	300	-	Ω

NOTES

1. Peak signal capacity is limited by the output circuit.
2. Measured between 233 and 253 K and V_{SS} +9.0 V. Dark signal at any temperature T (kelvin) is then estimated from:
   $$Q_d/Q_{d0} = 122T^3e^{-6400/T}$$
   where Q_{d0} is the dark signal at T = 293 K (20 °C).
3. Test carried out at e2v technologies on all sensors.
4. It is not practicable to measure charge transfer efficiency with so few pixels, but in general e2v technologies devices give the figures shown.
5. Measured using a dual-slope integrator technique (i.e. correlated double sampling) with a 10 μs integration period.
6. Readout at speeds in excess of 3 MHz can be achieved but performance to the parameters given cannot be guaranteed.
7. Measured between 233 and 253 K, excluding white defects.

BLEMISH SPECIFICATION

Traps Pixels where charge is temporarily held. Traps are counted if they have a capacity greater than 200 e^- at 243 K.

Slipped columns Are counted if they have an amplitude greater than 200 e^-.

Black spots Are counted when they have a signal level of less than 80% of the local mean at a signal level of approximately half full-well.

White spots Are counted when they have a generation rate 10 times the specified maximum dark signal generation rate (measured between 233 and 253 K). The amplitude of white spots will vary in the same manner as dark current, i.e.:

$$Q_d / Q_{d0} = 122T^3 e^{-6400/T}$$

White column A column which contains at least 9 white defects.

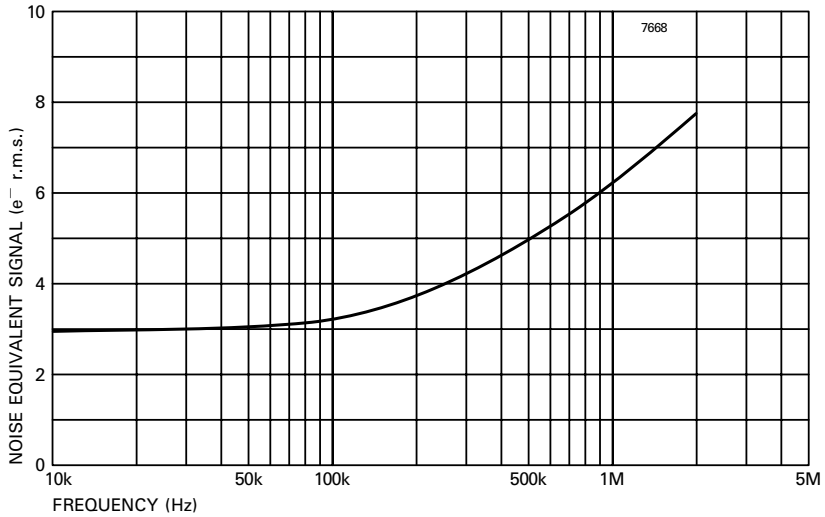
Black column A column which contains at least 9 black defects.

GRADE	0	1	5
Column defects:			
black or slipped	0	0	2
white	0	0	2
Black spots	2	4	130
Traps >200 e^-	0	0	2
White spots	0	2	20

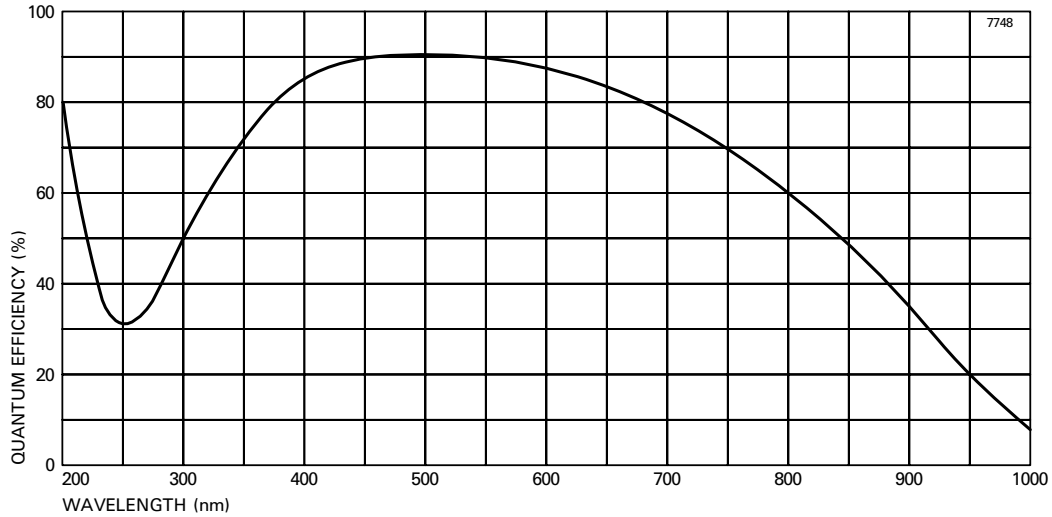
Note The effect of temperature on defects is that traps will be observed less at higher temperatures but more may appear below 243 K. The amplitude of white spots and columns will decrease rapidly with temperature.

TYPICAL OUTPUT CIRCUIT NOISE
(Measured using clamp and sample)

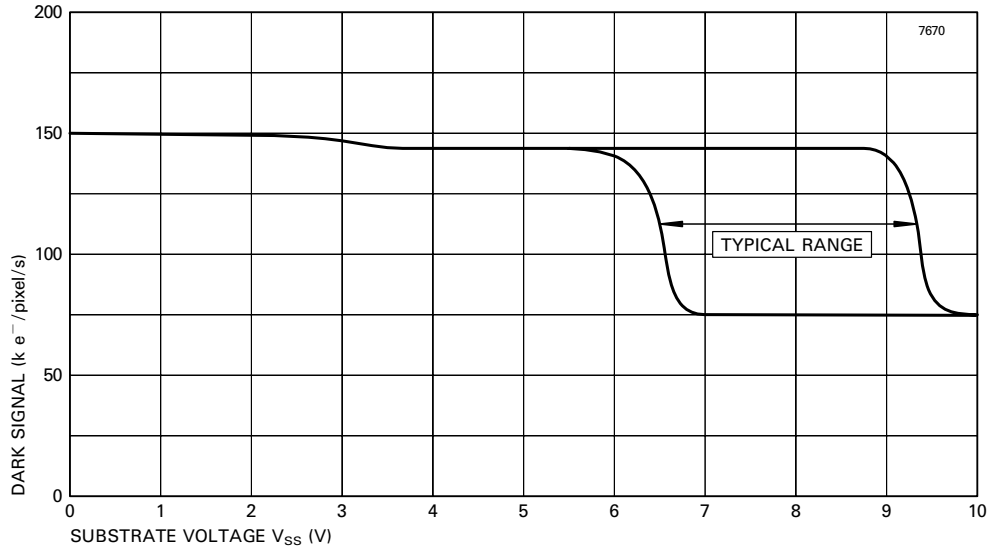
V_{SS} = 9.0 V V_{RD} = 17 V V_{OD} = 29 V



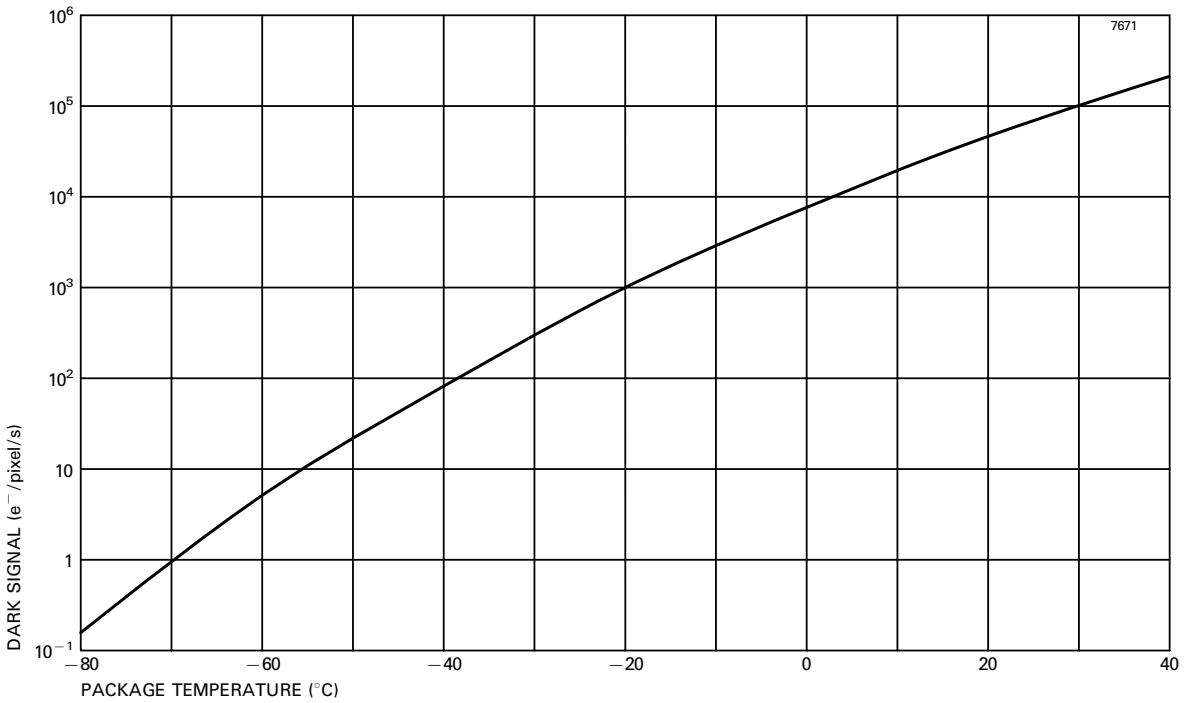
TYPICAL SPECTRAL RESPONSE (at −20 °C)
(No window, standard AR coating)



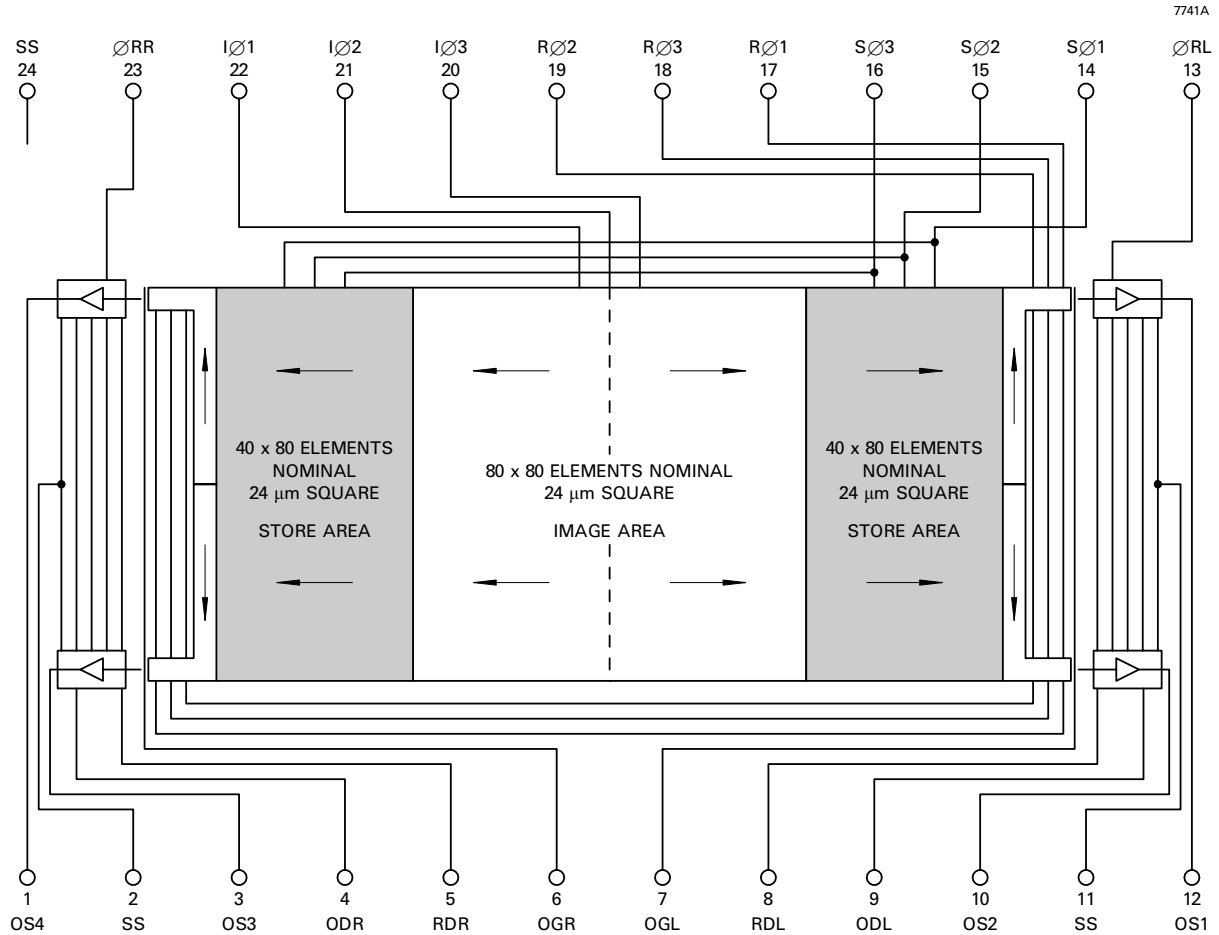
TYPICAL VARIATION OF DARK SIGNAL WITH SUBSTRATE VOLTAGE
(Two I∅ phases held high at +20 °C)



TYPICAL VARIATION OF DARK SIGNAL WITH TEMPERATURE (V_{ss} = +9.0 V)



DEVICE SCHEMATIC



Note: Alignment of the store shield may cause the number of image rows from each quadrant to vary by ±2 rows.

CONNECTIONS, TYPICAL VOLTAGES AND ABSOLUTE MAXIMUM RATINGS

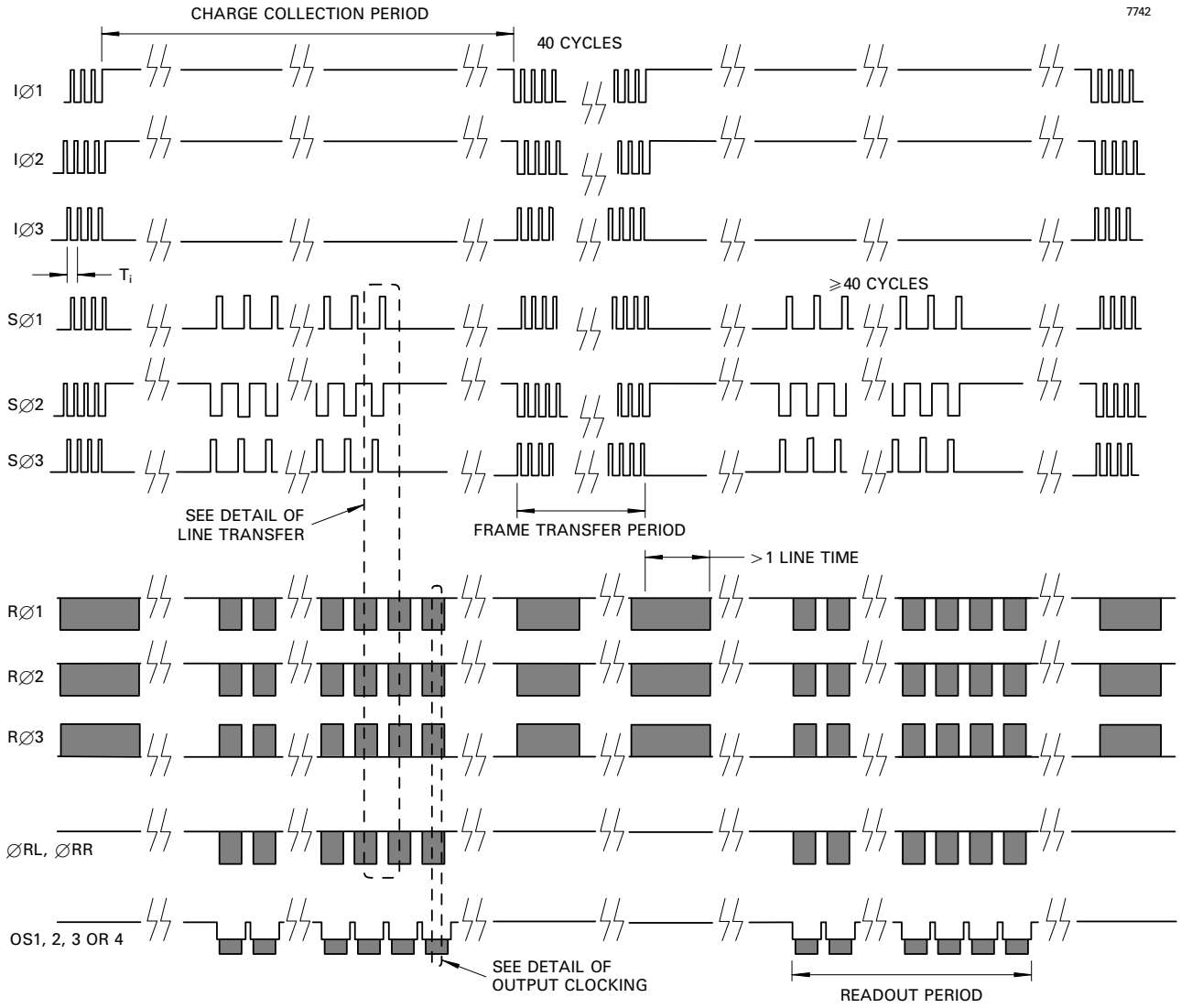
PIN	REF	DESCRIPTION	PULSE AMPLITUDE OR DC LEVEL (V) (See note 8)			MAXIMUM RATINGS with respect to V_{SS}
			Min	Typical	Max	
1	OS4	Output source: output circuit 4		see note 9		−0.3 to +25 V
2	SS	Substrate	0	9	10	-
3	OS3	Output source: output circuit 3		see note 9		−0.3 to +25 V
4	ODR	Output drain: output circuits 3 and 4	27	29	31	−0.3 to +35 V
5	RDR	Reset drain: output circuits 3 and 4	15	17	19	−0.3 to +25 V
6	OGR	Output gate: output circuits 3 and 4	1	3	5	±25 V
7	OGL	Output gate: output circuits 1 and 2	1	3	5	±25 V
8	RDL	Reset drain: output circuits 1 and 2	15	17	19	−0.3 to +25 V
9	ODL	Output drain: output circuits 1 and 2	27	29	31	−0.3 to +35 V
10	OS2	Output source: output circuit 2		see note 9		−0.3 to +25 V
11	SS	Substrate	0	9	10	-
12	OS1	Output source: output circuit 1		see note 9		−0.3 to +25 V
13	∅RL	Output reset pulse: output circuits 1 and 2	8	12	15	±25 V
14	S∅1	Store section, phase 1 (clock pulse)	8	12	15	±25 V
15	S∅2	Store section, phase 2 (clock pulse)	8	12	15	±25 V
16	S∅3	Store section, phase 3 (clock pulse)	8	12	15	±25 V
17	R∅1	Readout register, phase 1 (clock pulse)	8	11	15	±25 V
18	R∅3	Readout register, phase 3 (clock pulse)	8	11	15	±25 V
19	R∅2	Readout register, phase 2 (clock pulse)	8	11	15	±25 V
20	I∅3	Image section, phase 3 (clock pulse)	8	12	15	±25 V
21	I∅2	Image section, phase 2 (clock pulse)	8	12	15	±25 V
22	I∅1	Image section, phase 1 (clock pulse)	8	12	15	±25 V
23	∅RR	Output reset pulse: output circuits 3 and 4	8	12	15	±25 V
24	SS	Substrate	0	9	10	-

Maximum voltages between pairs of pins:
pin 4 (ODR) to pins 1, 3 (OS3, 4) . . . . . ±15 V
pin 9 (ODL) to pins 10, 12 (OS1, 2) . . . . . ±15 V
Maximum output transistor current . . . . . 10 mA

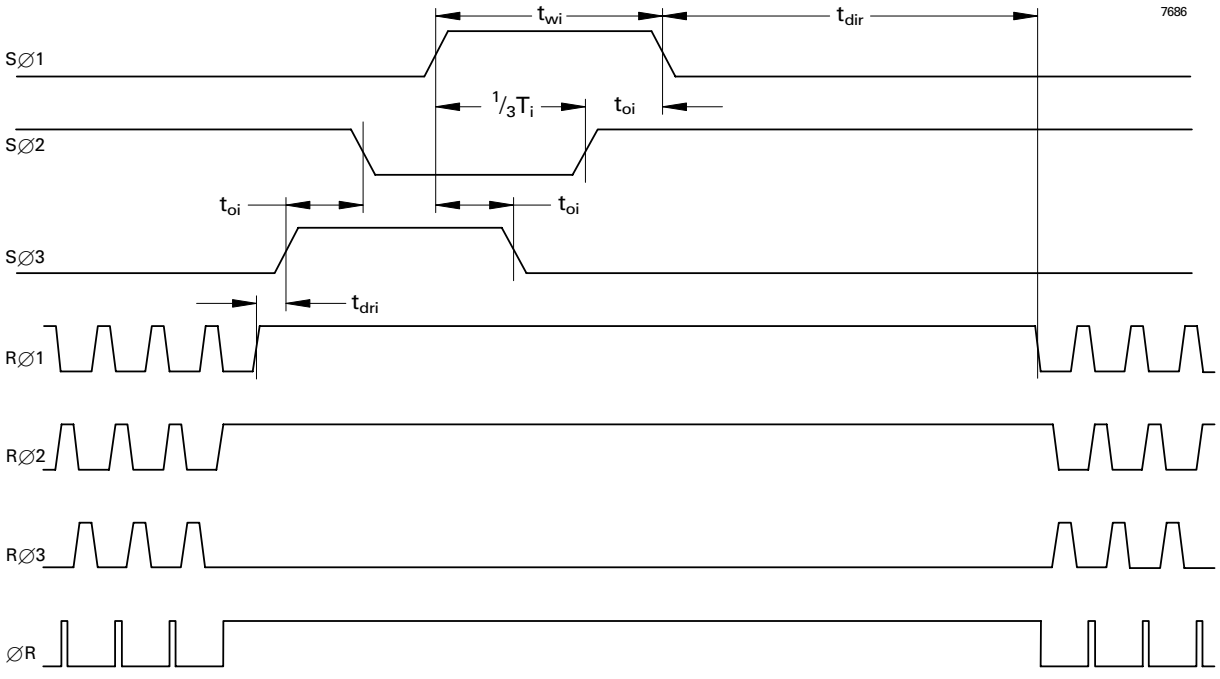
NOTES

8. Readout register clock pulse low levels +1 V; other clock low levels 0 ± 0.5 V.
9. Connect to ground via an external load (see note 16).
10. All devices will operate at the typical values given. However, some adjustment within the minimum to maximum range may be required to optimise performance for critical applications. It should be noted that conditions for optimum performance may differ from device to device.

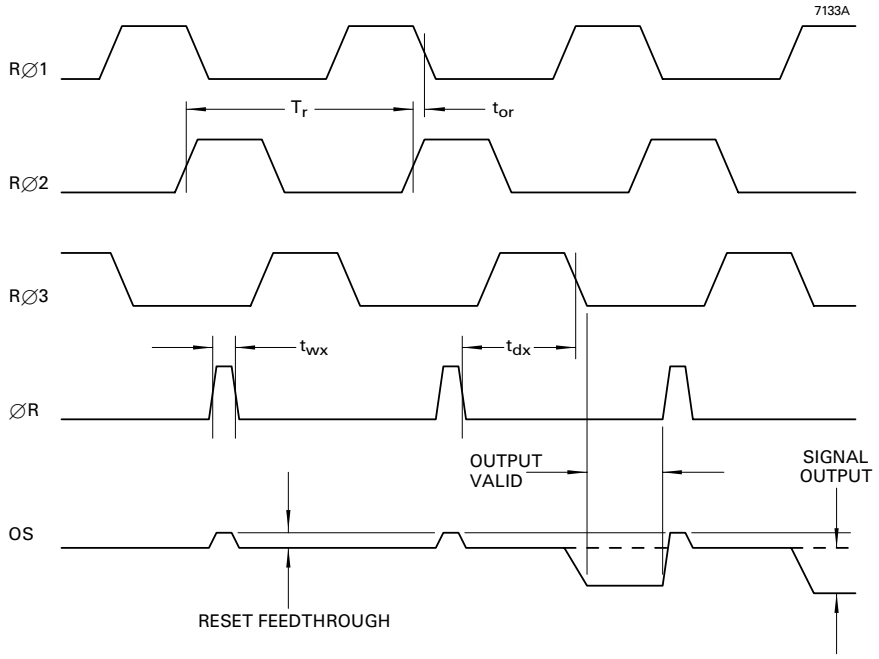
FRAME TRANSFER TIMING DIAGRAM



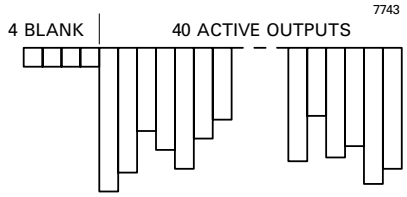
DETAIL OF LINE TRANSFER



DETAIL OF OUTPUT CLOCKING



LINE OUTPUT FORMAT



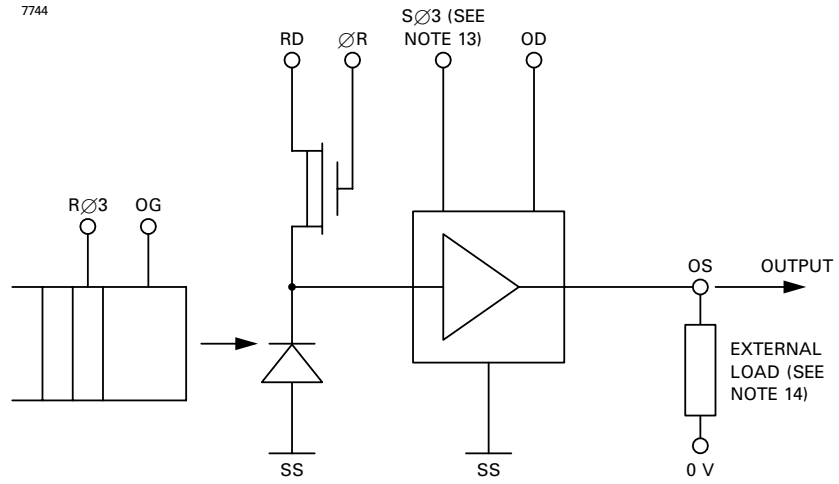
CLOCK TIMING REQUIREMENTS

Symbol	Description	Min	Typical	Max	
T_i	Image clock period	0.2	2.0	see note 11	µs
t_{wi}	Image clock pulse width	0.1	1.0	see note 11	µs
t_{ri}	Image clock pulse rise time (10 to 90%)	30	100	$0.2T_i$	ns
t_{fi}	Image clock pulse fall time (10 to 90%)	30	100	$0.2T_i$	ns
t_{oi}	Image clock pulse overlap	0	$0.5t_{ri}$	$0.2T_i$	µs
t_{dir}	Delay time, SØ stop to RØ start	1	2	see note 11	µs
t_{dri}	Delay time, RØ stop to SØ start	$T_r/3$	T_r	see note 11	µs
T_r	Output register clock cycle period	330	1000	see note 11	ns
t_{rr}	Clock pulse rise time (10 to 90%)	10	$0.1T_r$	$0.2T_r$	ns
t_{fr}	Clock pulse fall time (10 to 90%)	10	$0.1T_r$	$0.2T_r$	ns
t_{or}	Clock pulse overlap	0	$0.5t_{rr}$	$0.1T_r$	ns
t_{wx}	Reset pulse width	30	$0.1T_r$	$0.3T_r$	ns
t_{rx}, t_{fx}	Reset pulse rise and fall times	$0.2t_{wx}$	$0.5t_{rr}$	$0.1T_r$	ns
t_{dx}	Delay time, ØR low to RØ3 low	30	$0.5T_r$	$0.8T_r$	ns

NOTES

11. No maximum other than that necessary to achieve an acceptable dark signal at the longer readout times.
12. To minimise dark current, two of the IØ clocks should be held low during integration. IØ timing requirements are identical to SØ (as shown above).

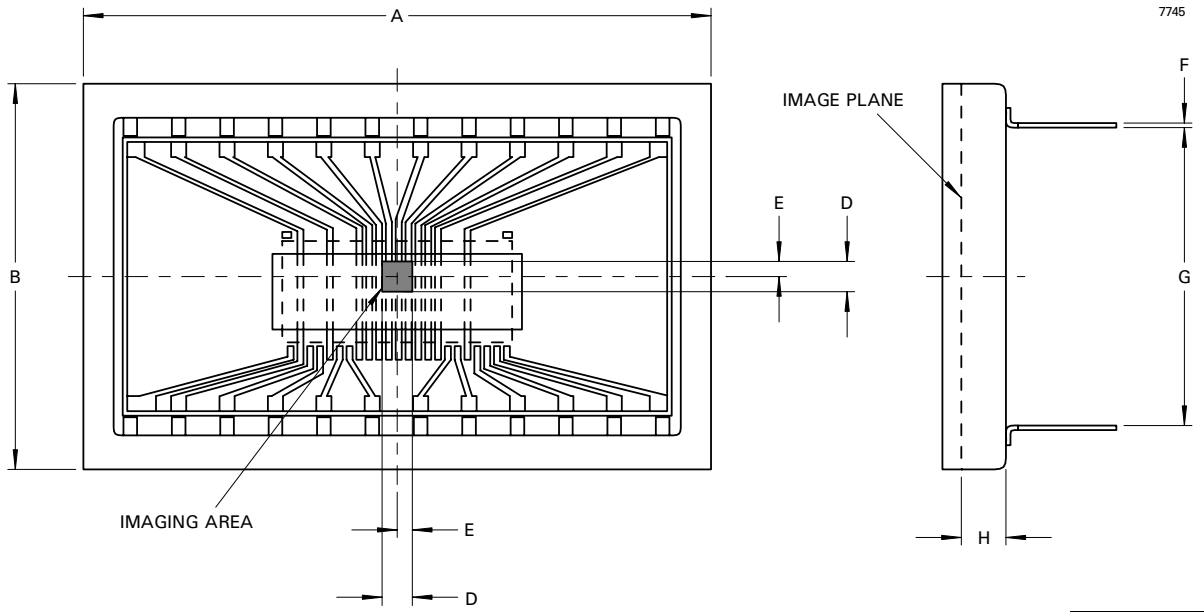
OUTPUT CIRCUIT

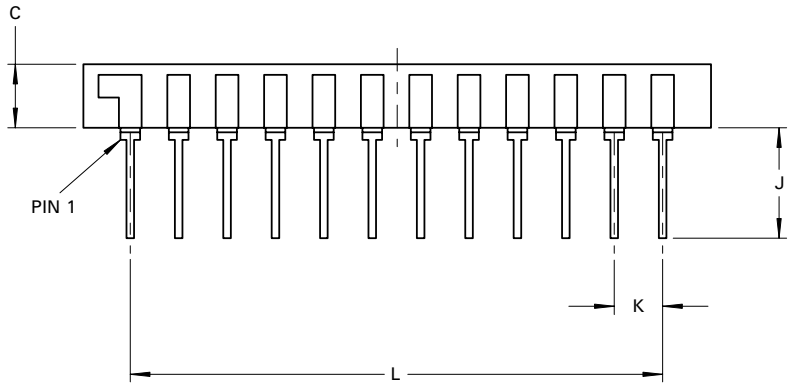


NOTES

13. The amplifier has a DC restoration circuit which is internally activated whenever S∅3 is high.
14. Not critical; can be a 2 to 5 mA constant current supply or an appropriate 3.3k - 10 kΩ load resistor. The quiescent voltage on OS is then approximately V_{OD} − 4 V.

OUTLINE
(All dimensions without limits are nominal)





Ref	Millimetres
A	32.89
B	20.07
C	3.3
D	1.92
E	0.96
F	$0.254^{+0.051}_{-0.025}$
G	15.24 ± 0.25
H	2.305 ± 0.600
J	4.85 min
K	2.54 ± 0.15
L	27.94 ± 0.15

ORDERING INFORMATION

Options include:

- Temporary Quartz Window
- Permanent Quartz Window
- Temporary Glass Window
- Permanent Glass Window
- Fibre-optic Coupling
- UV Coating
- X-ray Phosphor Coating

For further information on the performance of these and other options, please contact e2v technologies.

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full antistatic handling precautions should be taken whenever using a CCD sensor or module. These include:-

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving socket pins to be positively grounded
- Unattended CCDs should not be left out of their conducting foam or socket.

Evidence of incorrect handling will invalidate the warranty. All devices are provided with internal protection circuits to the gate electrodes (pins 6, 7, 13 to 23) but not to the other pins.

HIGH ENERGY RADIATION

Device characteristics will change when subject to ionising radiation.

Users planning to operate CCDs in high radiation environments are advised to contact e2v technologies.

TEMPERATURE LIMITS

	Min	Typical	Max	
Storage	73	–	373	K
Operating	73	243	323	K

Operation or storage in humid conditions may give rise to ice on the sensor surface on cooling, causing irreversible damage.

Maximum device heating/cooling . . 5 K/min