CCD30-11 NIMO Back Illuminated Deep Depleted High Performance CCD Sensor

FEATURES

- 1024 by 256 Pixel Format
- 26µm Square Pixels
- Image area 26.6 x 6.7mm
- Back Illuminated format for high quantum efficiency
- Deep Depletion for Enhanced Infrared Sensitivity
- Full-Frame Operation
- Symmetrical anti-static gate protection
- Unique Fringe Suppression Structure
- 100% Active Area
- Anti-bloomed Readout Register

APPLICATIONS

- Spectroscopy
- Scientific Imaging
- TDI Operation

INTRODUCTION

The CCD30-11 deep depletion sensor is a high performance CCD sensor designed as an alternative to the standard CCD30-11, for use in the scientific spectroscopy instrument market, where enhanced infrared spectral response is a critical performance parameter. With an array of 1024 x 256, 26 µm square pixels it has an imaging area to suit most spectrometer outputs of 26.6 x 6.7 mm (1.05 x 0.26 inch).

The readout register is organised along the long (1024 pixel) edge of the sensor and contains an anti-blooming drain to allow high speed binning operations of low level signals which may be adjacent to much stronger signals. The novel output amplifier design has no light emission.

The sensor is manufactured on thick epitaxial silicon, which gives much improved infrared responsivity. It is designed as a standard mode CCD as it is necessary to deplete far into the epitaxial silicon to avoid loss of resolution. The back illuminated structure, along with a NIR anti-reflection coating, further enhances the spectral response across the full spectral range.

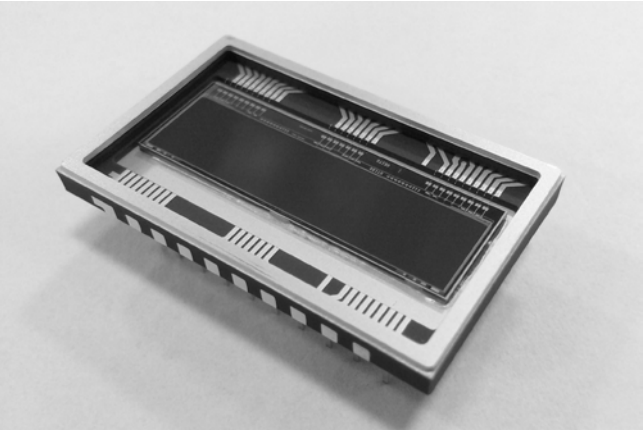
Back illuminated sensors can suffer etaloning effects at wavelengths typically longer than 700 nm, which are strongly dependent on the bandwidth of the illumination. This device variant reduces these etaloning effects by a factor of 10 typically, when compared with standard back illuminated devices.

Standard three phase clocking and isolated buried channel charge transfer are employed.

In common with all other e2v technologies CCD sensors, the CCD30-11 is available with either a quartz or fibre-optic window.

Designers are advised to consult e2v technologies should they be considering using CCD sensors in abnormal environments or if they require customised packaging or performance features.

Further information on deep depletion CCDs can be found in the technical paper on the e2v website titled Deep Depleted CCD sensors.



TYPICAL PERFORMANCE

(Low noise mode)

Pixel readout frequency	45 KHz
Output amplifier sensitivity	2.0 µV/e^-
Peak signal	700 ke^-/pixel
Spectral range	200–1100 nm
Readout noise @ 18 kHz	5.0 e^- rms

GENERAL DATA

Format

Image area	26.6 x 6.7 mm
Active pixels	1024 (H) x 256 (V)
Pixel size	26 x 26µm
Number of output amplifiers	1

Package

Package size	32.89 x 20.07 mm
Number of pins	20
Inter-pin spacing	2.54 mm
Window material	Quartz or Removable glass
Package type	Ceramic DIL array

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PERFORMANCE

		Min	Typical	Max	Units	Note
Peak charge storage		-	700,000	-	e^-/pixel	1,3
Peak output voltage (unbinned)		-	1.4	-	V	1,3
Dark signal at 293 K		-	170,000	340,000	e^-/pixel/s	2, 6
Charge transfer efficiency	Parallel	-	99.9999	-	%	3
	Serial	-	99.9993	-	%	
Output amplifier responsivity	Low noise mode	1.3	2.0	2.3	µV/e^-	
Readout noise	Low noise mode	-	5	8	rms e^-	4
Maximum readout frequency		-	45	5000	kHz	5
Binned Column Dark Signal Non-Uniformity at 293 K (std. deviation)		-	5,000	10,000	e^-/pixel/s	6

SPECTRAL RESPONSE AT 243 K (–30 °C)

Wavelength (nm)	Minimum Response (QE) (see note 7)		Maximum Response Non-uniformity (1σ)	
	Basic Process NIR Coated	Enhanced Process Multilayer 2 Coated		
350	15	30	-	%
400	30	75	3	%
500	50	75	-	%
650	75	80	3	%
900	65	65	5	%

NOTES

1) Signal level at which resolution begins to degrade. The typical values are those expected from design.
2) The typical average (background) dark signal at any temperature T (Kelvin) between 230 and 300 K is given by:

$$Q_d/Q_{d0} = 122T^3e^{-6400/T}$$

where Q_{d0} is the dark current at 293 K. Note that this is typical performance and some variation may be seen between devices. Below 230 K additional dark current components with a weaker temperature dependence may become significant.
3) Not measured on each sensor but expected to exceed the typical value.
4) Measured at a pixel readout frequency of 18 kHz using a dual-slope integrator technique (i.e. correlated double sampling). All other tests measured at 45 kHz.
5) Readout above 5000 kHz can be achieved but is not factory tested. Performance to the parameters given is not guaranteed by factory at frequencies other than the typical value.
6) Dark signal and DSNU values specified at 293 K are calculated from tests performed at 243 K with full parallel binning.
7) QE has a temperature dependence, with lower values as temperature decreases.

BLEMISH SPECIFICATION

Traps Pixels where charge is temporarily held. Traps are counted if they have a capacity greater than 200 e^- at 243 K.

Black spots Are counted when they have a signal level of less than 80% of the local mean at a signal level of approximately half full-well at 243K.

White spots Are counted when they have a generation rate 8 times the specified maximum dark signal generation rate (measured at 243 K). The typical temperature dependence of white spot blemishes is the same as that of the average dark signal i.e.:

$$Q_d/Q_{d0} = 122T^3e^{-6400/T}$$

Column defects A column which contains at least 9 white or 9 black defects.

Spikes Are measured with the image fully binned in to the register. Level 1 spikes are columns with 6.4 Me-/col or greater equivalent signal at +20 ^oC. Level 2 spikes are columns with 25.6 Me-/col or greater.

GRADE	**0**	**1**	**2**
Column defects; black or white	0	2	6
White	0	0	0
Black spots	12	25	120
Traps >200 e^-	1	2	5
White spots	20	30	50
Level 1 spikes	10	10	10
Level 2 spikes	2	2	2

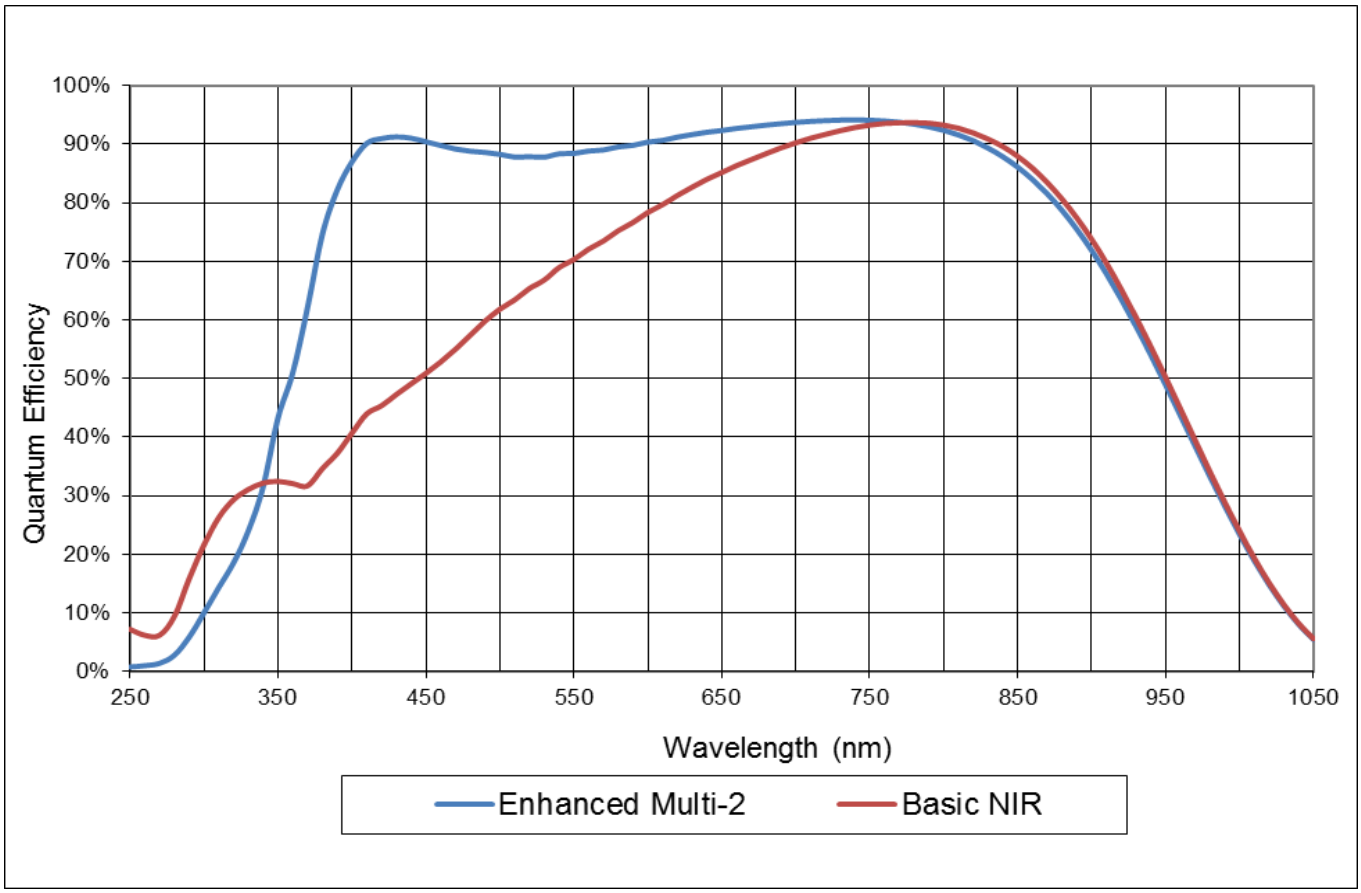
Minimum separation between adjacent black columns – 50 Pixels

Grade 5

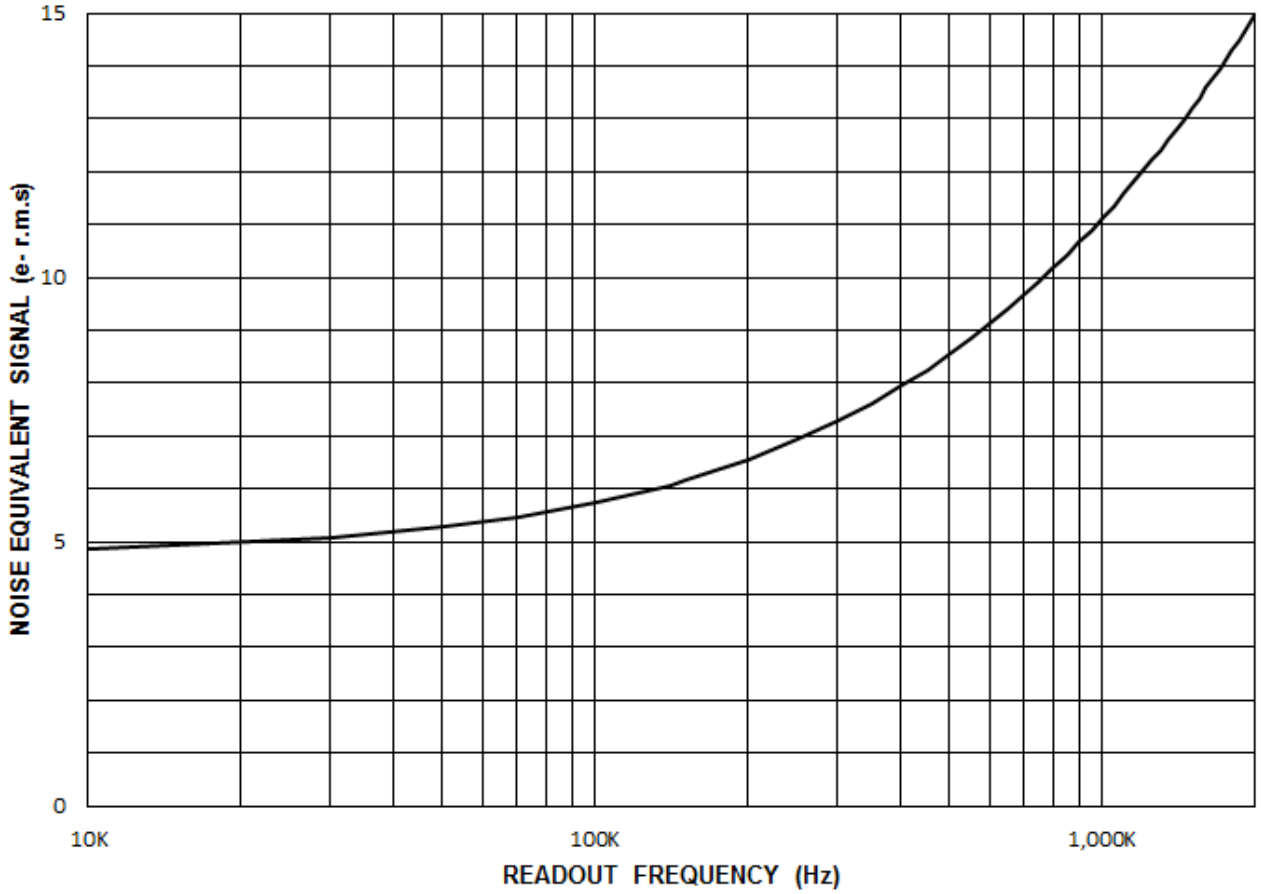
Devices which are fully functional, with image quality below that of grade 2, and which may not meet all other performance parameters.

Note: The effect of temperature on defects is that traps will be observed less at higher temperatures but more may appear below 233 K. The amplitude of white spots and columns will decrease rapidly with temperature.

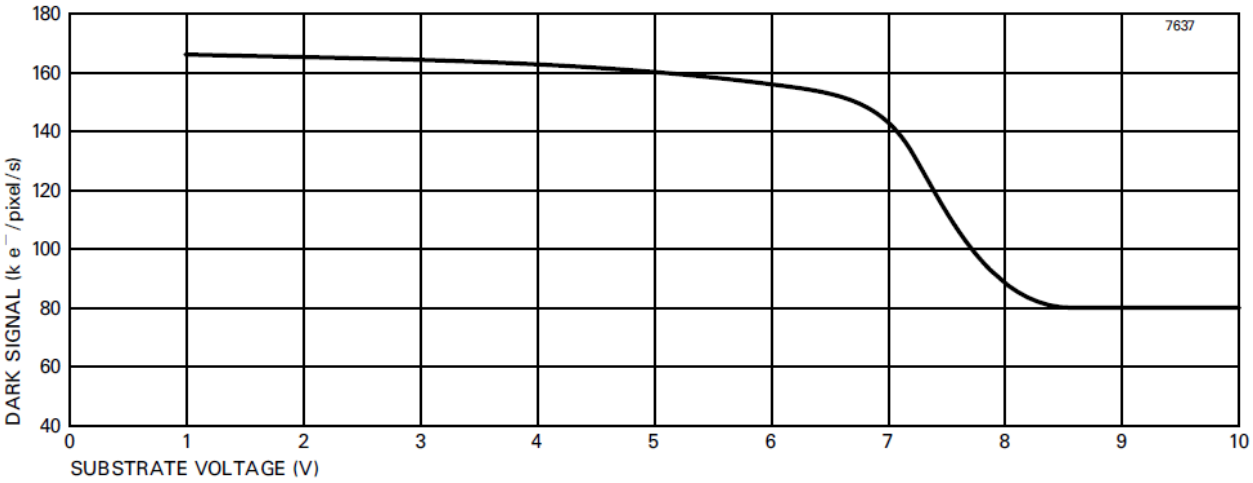
TYPICAL SPECTRAL RESPONSE (At –30 °C)



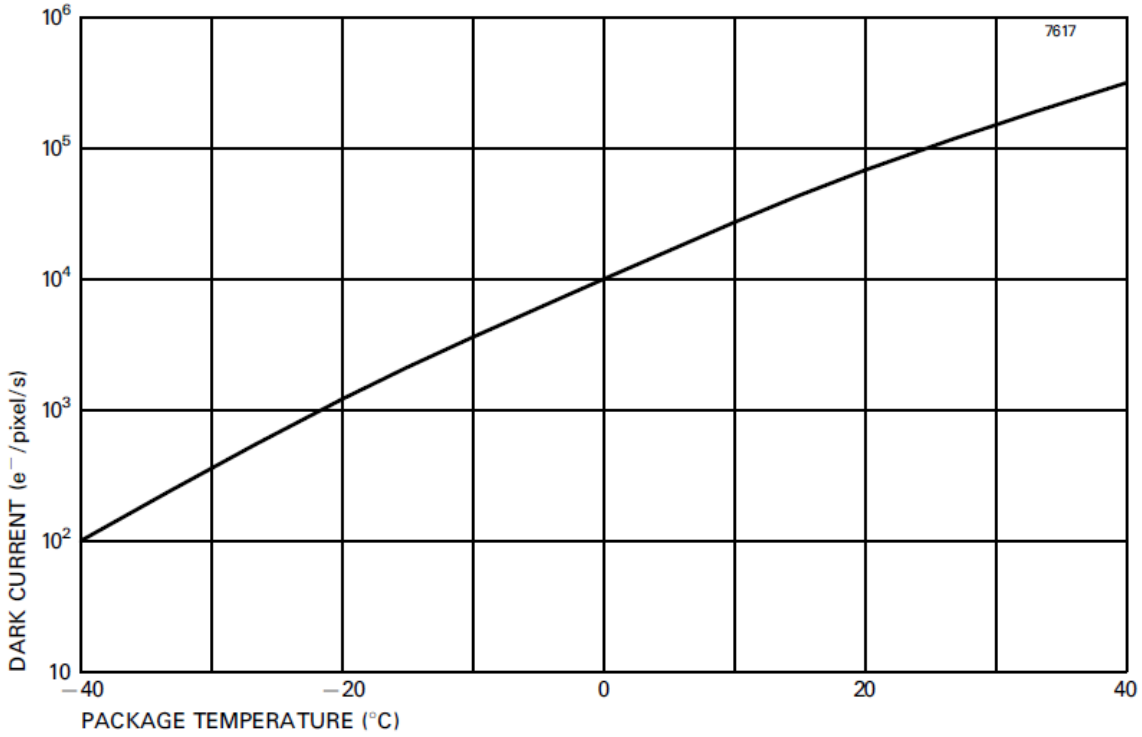
TYPICAL OUTPUT CIRCUIT NOISE



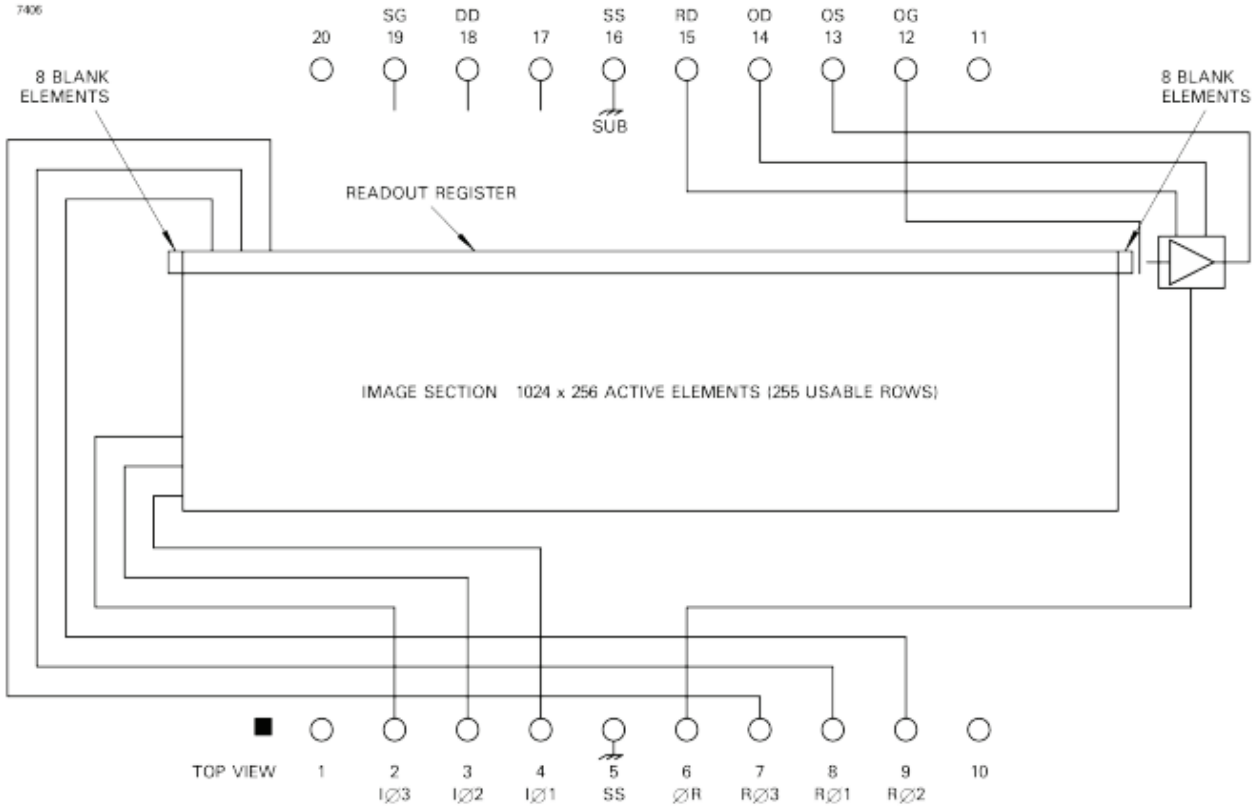
TYPICAL VARIATION OF DARK CURRENT WITH SUBSTRATE VOLTAGE (based on Front Faced Deep Depleted NIMO)



TYPICAL VARIATION OF DARK CURRENT WITH TEMPERATURE (based on Front Faced Deep Depleted NIMO)



DEVICE SCHEMATIC



CONNECTIONS, TYPICAL VOLTAGES AND ABSOLUTE MAXIMUM RATINGS

PIN	REF	DESCRIPTION	CLOCK AMPLITUDE OR DC LEVEL (V) (see note 12)			MAX RATINGS with respect to Substrate SS
			Min	Typical	Max	
1	-	No connection		-		-
2	IØ3	Image section, phase 3 (clock pulse)	8	12	15	±20V
3	IØ2	Image section, phase 2 (clock pulse)	8	12	15	±20V
4	IØ1	Image section, phase 1 (clock pulse)	8	12	15	±20V
5	SS	Substrate	0	3	10	-
6	ØR	Output reset pulse	8	12	15	±20V
7	RØ3	Reset register, phase 3 (clock pulse)	8	11	15	±20V
8	RØ1	Reset register, phase 2 (clock pulse)	8	11	15	±20V
9	RØ2	Reset register, phase 1 (clock pulse)	8	11	15	±20V
10	-	No connection				-
11	-	No connection				-
12	OG	Output gate	1	3	5	±20V
13	OS	Output transistor source		See note 8		-0.3 to +25V
14	OD	Output drain	27	29	32	-0.3 to +32V
15	RD	Reset transistor drain	15	17	19	-0.3 to +25V
16	SS	Substrate	0	3	10	-
17	-	No connection		-		-
18	DD	Dump drain	20	24	25	-0.3 to +25V
19	SG	Spare gate	0	0	VSS +19	±20V
20	-	No connection		-		-

NOTES

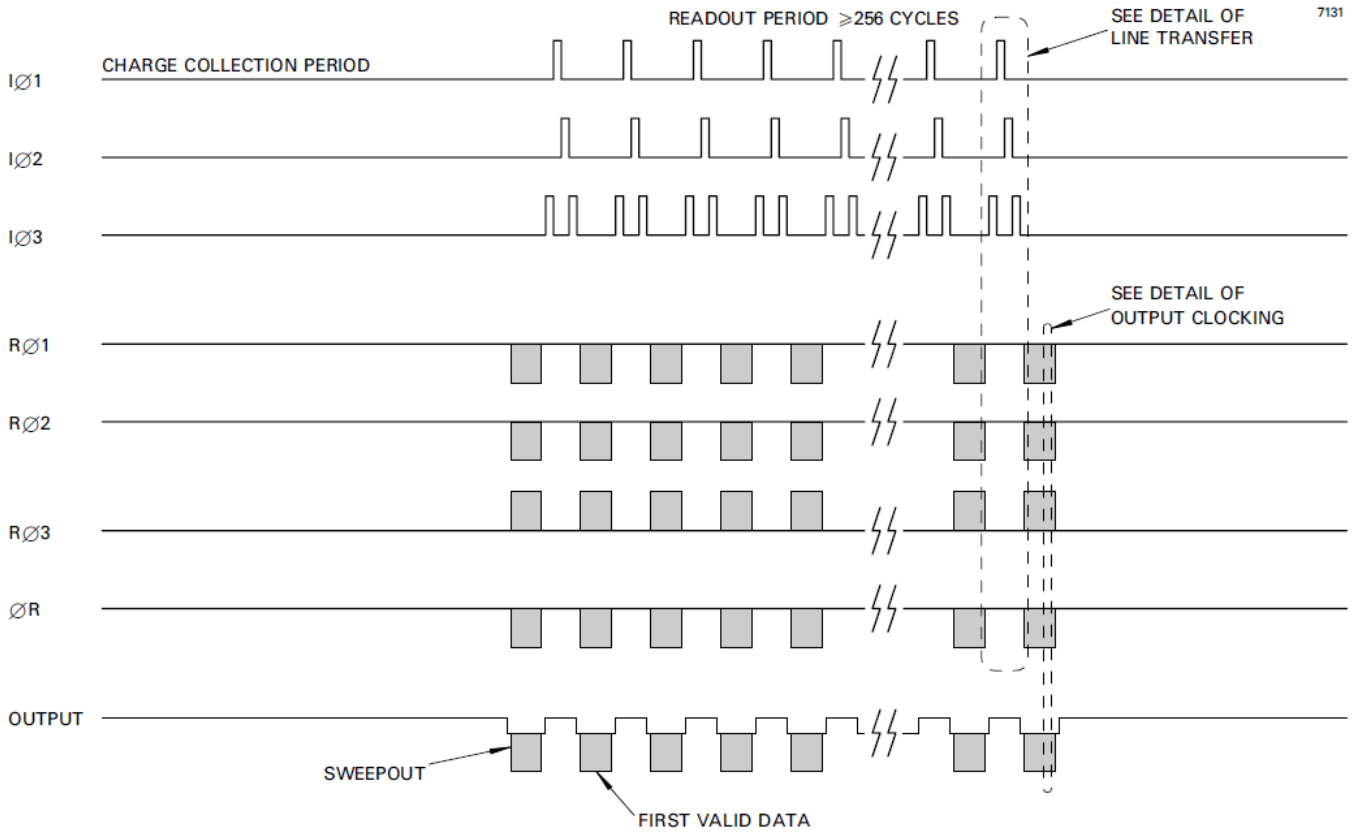
If all voltages are set to the 'typical' values, operation at or close to specification should be obtained. Some adjustment within the minimum – maximum range specified may be required to optimise performance.

Voltage between pairs of pins: OS to OD + 15 V. Maximum current through any source or drain pin: 10 mA.

SG needs to be grounded to prevent unwanted charge moving into the register.

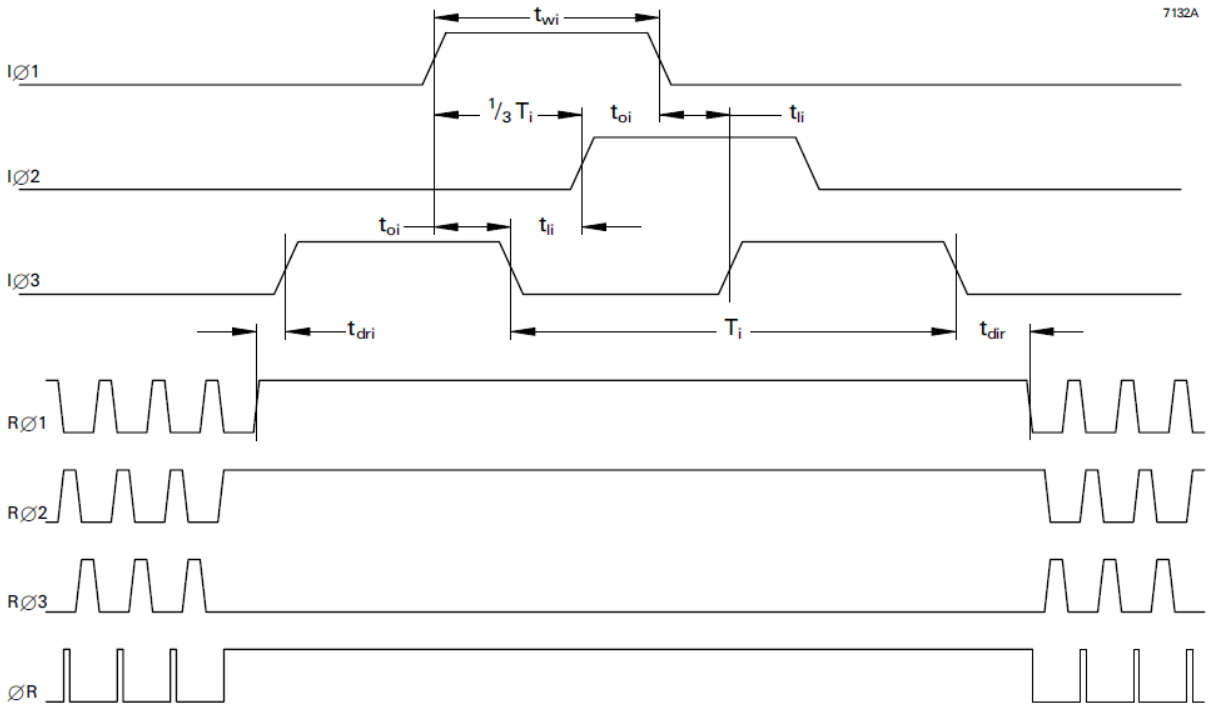
DD controls the anti-blooming function of the register and also biases the drains around the edge of the CCD, protecting the image and register from charge generated elsewhere spilling into these sensitive regions of the device.

FRAME READOUT TIMING DIAGRAM

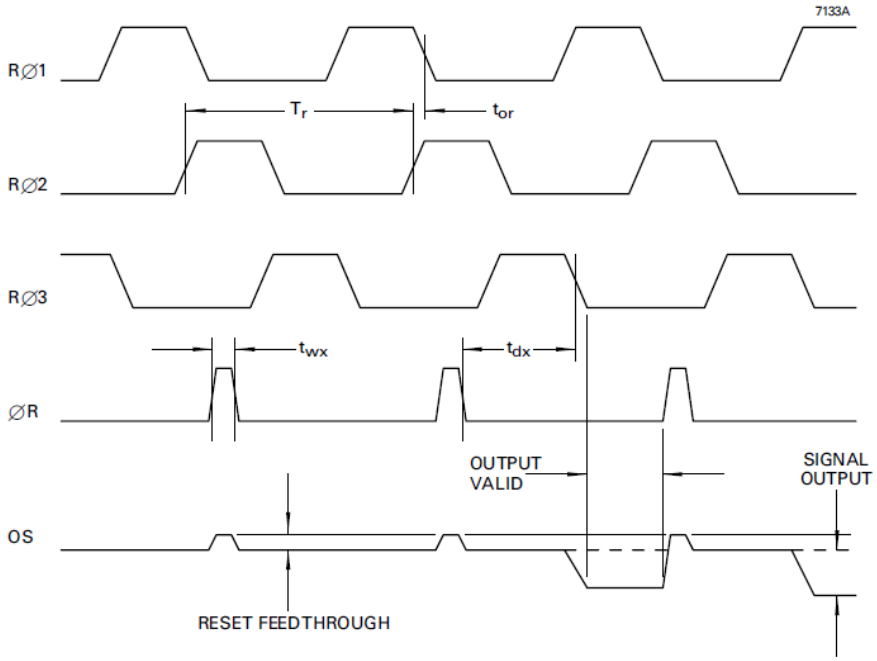


DETAIL OF LINE TRANSFER (Not to scale)

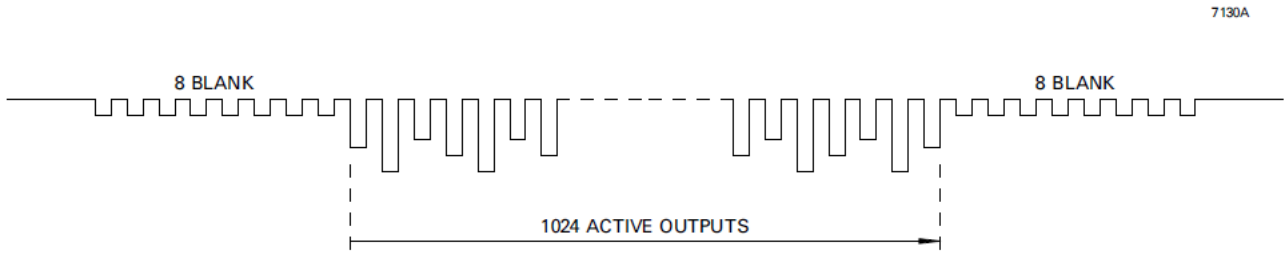
(For output from a single amplifier)



DETAIL OF OUTPUT CLOCKING



LINE OUTPUT FORMAT



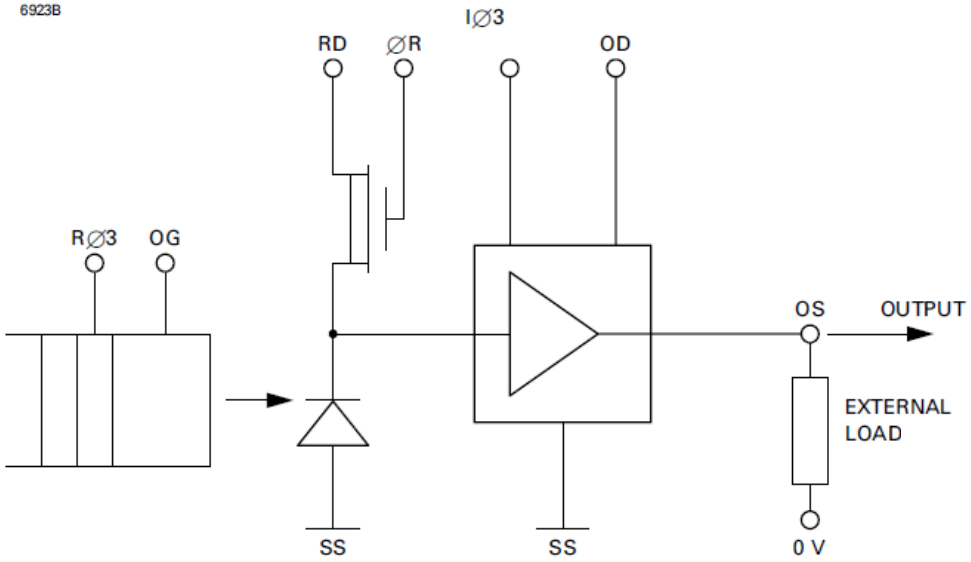
CLOCK TIMING REQUIREMENTS

Symbol	Description	Min	Typ	Max	Unit
T_i	Image clock period	10	20	See note 8	µs
t_{wi}	Image clock pulse width	5	10	See note 8	µs
t_{ri}	Image clock pulse rise time (10 to 90%)	0.5	1	$0.5t_{oi}$	µs
t_{fi}	Image clock pulse fall time (10 to 90%)	t_{ri}	1	$0.5t_{oi}$	µs
t_{oi}	Image clock pulse overlap	1	2	$0.2T_i$	µs
t_{li}	Image clock pulse, two phase low	1	5	$0.2T_i$	µs
t_{dir}	Delay time, IØ stop to RØ start	3	10	See note 8	µs
t_{dri}	Delay time, RØ stop to IØ start	1	2	See note 8	µs
T_r	Output register clock cycle period	200	See note 9	See note 8	ns
t_{rr}	Clock pulse rise time (10 to 90%)	50	$0.1T_r$	$0.3T_r$	ns
t_{fr}	Clock pulse fall time (10 to 90%)	t_{rr}	$0.1T_r$	$0.3T_r$	ns
t_{or}	Clock pulse overlap	20	$0.5t_{rr}$	$0.1T_r$	ns
t_{wx}	Reset pulse width	30	$0.1T_r$	$0.2T_r$	ns
t_{rx} , t_{fx}	Reset pulse rise and fall times	20	$0.5t_{rr}$	$0.2T_r$	ns
t_{dx}	Delay time, ØR low to RØ3 low	30	$0.5T_r$	$0.8T_r$	ns

NOTES

8) No maximum other than that necessary to achieve an acceptable dark signal at the longer readout times.
9) As set by the readout period. See note 4.

OUTPUT CIRCUIT

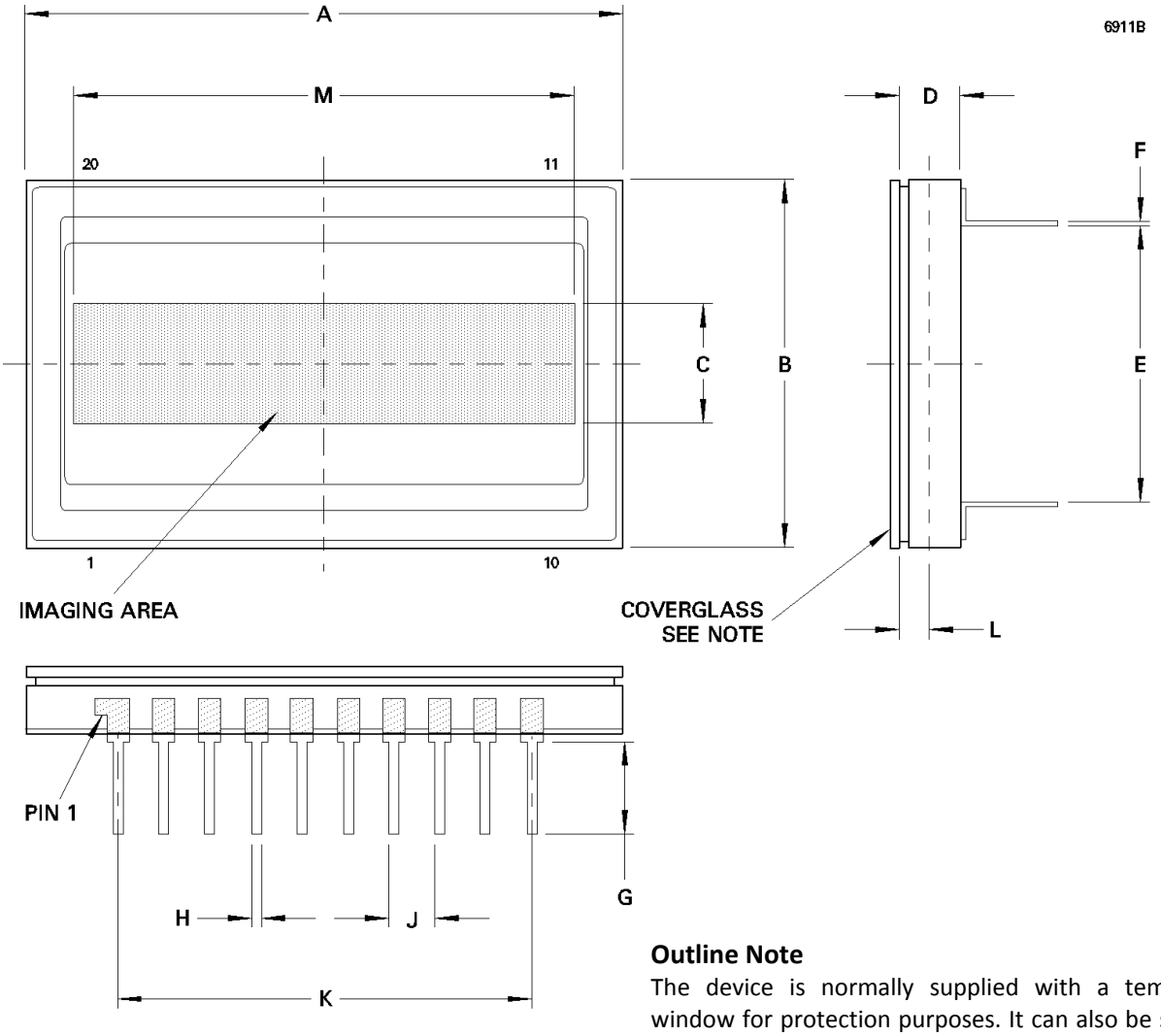


NOTES

10) Not critical; can be a 1 – 5 mA constant current source, or 5 – 10 kΩ resistor.
11) The amplifier has a DC restoration circuit, which is activated internally whenever IØ3 is pulsed high.
12) Image section pulse low levels 0 ± 0.5 V; other pulse low levels IØ low +1 V.
13) Output node capacity is typically 2 times that of the image section.

OUTLINE

(All dimensions are by design and not verified on each sensor. Those without limits are nominal)



Outline Note

The device is normally supplied with a temporary glass window for protection purposes. It can also be supplied with a fixed, quartz or fibre-optic window where required.

Ref	Millimetres	
A	32.89 ± 0.38	
B	20.07 ± 0.25	
C	6.7	
D	3.30 ± 0.33	
E	15.24 ± 0.25	
F	0.254	+ 0.051
		- 0.025
G	5.21	
H	0.46 ± 0.05	
J	2.54 ± 0.13	
K	22.86 ± 0.13	
L	1.65 ± 0.56	
M	26.6	

ORDERING INFORMATION

Options include:

- Temporary Quartz Window
- Permanent Quartz Window
- Temporary Glass Window

For further information on the performance of these and other options, please contact e2v technologies.

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full antistatic handling precautions should be taken whenever using a CCD sensor or module. These include:-

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving socket pins to be positively grounded
- Unattended CCDs should not be left out of their conducting foam or socket.

Evidence of incorrect handling will invalidate the warranty. All devices are provided with internal protection circuits to the gate electrodes (pins 2, 3, 4, 6, 7, 8, 9, 12, 19) but not to the other pins.

HIGH ENERGY RADIATION

Device characteristics will change when subject to ionising radiation.
Users planning to operate CCDs in high radiation environments are advised to contact e2v technologies.

TEMPERATURE LIMITS

	Min	Typical	Max	
Storage	73	-	373	K
Operating	73	233	323	K

Operation or storage in humid conditions may give rise to ice on the sensor surface on cooling, causing irreversible damage.

Maximum device heating/cooling ..... 5 K/min