EV12AS350B

12-bit 5.4Gsps Analog to Digital Converter

DATASHEET

Main Features

- Single Channel ADC with 12-bit resolution using four interleaved cores enabling 5.4 Gsps conversion rate
- Single 5.4 GHz Differential Symmetrical Input Clock
- 1000 mVpp Analog Input (Differential AC or DC Coupled)
- ADC Master Reset (LVDS)
- 2 conversion modes
  - 4 interleaved cores with staggered output data (equivalent to Mux 1:4)
  - Simultaneous sampling over 4 cores converting the same input signal with aligned outputs (can be used for real time averaging)
- LVDS Output format
- Digital Interface (SPI) with reset signal:
  - Standby Mode
  - Selection of data output swing
  - Test Modes
  - Chip configurations
- Power Supplies: single 4.8V, 3.2V and 2.0V
- Reduced clock induced transients on power supply pins due to BiCMOS Silicon technology
- Power Dissipation: 6.7 W
- EBGA380 Package 31x31mm (1.27 mm Pitch)

Performance

- Analog input bandwidth (-3 dB): 4.8 GHz
- Latency: 26 clock cycles
- Single tone dynamic performance:

Single Tone Conditions Fs	Fin	Pin	Performance	
5.4 GSPS	1.9 GHz	-3 dBFS	**ENOB** **SNR** **SFDR**	**8.6 bit** **54.5 dBFS** **64 dBFS**
5.4 GSPS	1.9 GHz	-6 dBFS	**ENOB** **SNR** **SFDR**	**8.9 bit** **55.7 dBFS** **68 dBFS**
5.4 GSPS	2.69 GHz	-3 dBFS	**ENOB** **SNR** **SFDR**	**8.1 bit** **53.0 dBFS** **56 dBFS**
5.4 GSPS	2.69 GHz	-6 dBFS	**ENOB** **SNR** **SFDR**	**8.5 bit** **54.5 dBFS** **64 dBFS**
5.4 GSPS	4.2 GHz	-3 dBFS	**ENOB** **SNR** **SFDR**	**6.9 bit** **49.5 dBFS** **45 dBFS**
5.4 GSPS	4.2 GHz	-6 dBFS	**ENOB** **SNR** **SFDR**	**7.8 bit** **52.1 dBFS** **54 dBFS**

- Dual tone dynamic performance:

Dual Tone Conditions			Performance	
Fs	Fin1/Fin2	Pin (on each tone)		
5.4 GSPS	2600 MHz 2610 MHz	-7 dBFS	**IMD**	**57 dBFS**
		-9 dBFS		**63 dBFS**
		-12 dBFS		**72 dBFS**

- NPR performance:

NPR Conditions			Performance At optimum loading factor	
Fs	Pattern start/stop frequency	Notch frequency / width		
5.4 GSPS	800 MHz / 2200 MHz	1300 MHz / 25 MHz	**NPR**	**48 dB**

Applications

- High Speed Data Acquisition
- Direct RF Down conversion
- Ultra Wideband Satellite Digital Receiver
- 16 Gbps pt-pt microwave receivers
- High energy Physics
- Automatic Test Equipment
- High Speed Test Instrumentation
- LiDAR (Light Detection And Ranging)
- Software Design Radio

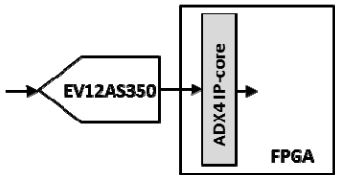
Performance improvement IP

ADX4 is an IP-core for time-interleaved ADC mismatch error correction. In time-interleaved operating mode, ADX4 increases SFDR by wideband suppression of time-interleaving aliasing spurs due to ADC mismatch beyond 70 dBFS.
ADX4 is available for evaluation on EV12AS350-ADX4-EVM evaluation board and can be licensed for production use. It is available for implementation on a wide range of FPGAs and with standard-cell design for ASICs.
ADX4 IP can be activated on all parts having the ADX4 suffix in their part number.

In addition, another IP designed specifically to improve the coding error rate of EV12AS350 is also available.

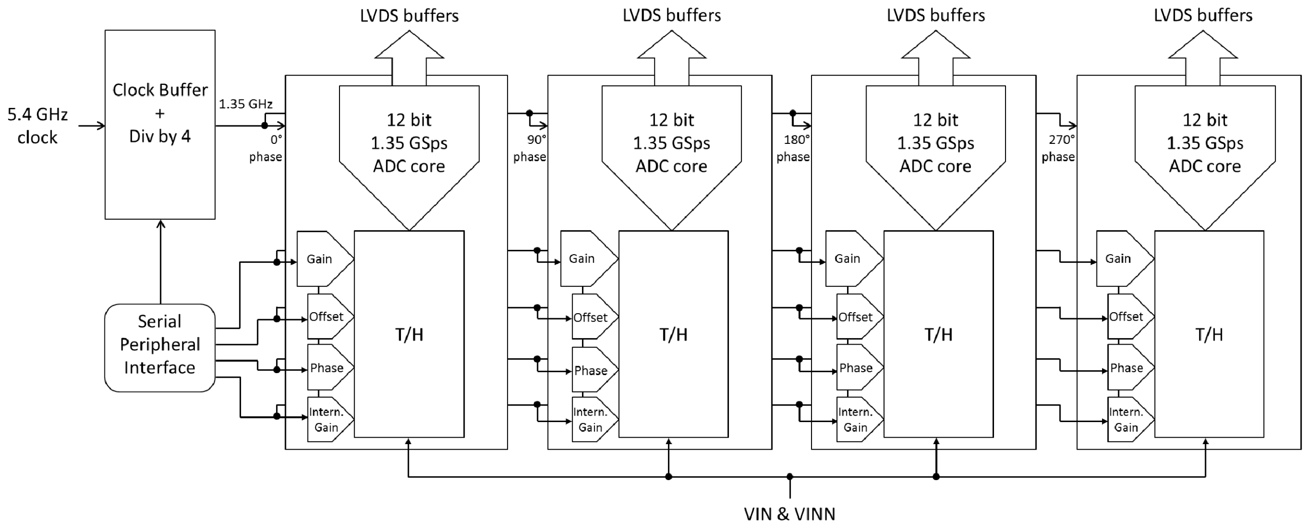
The EV12AS350-ADX4-EVM evaluation module pre-loaded with these IP-cores is available for fast performance evaluation.

Figure 1. ADX4 IP-core used with EV12AS350A



1 Block Diagram

Figure 2. Simplified Block Diagram

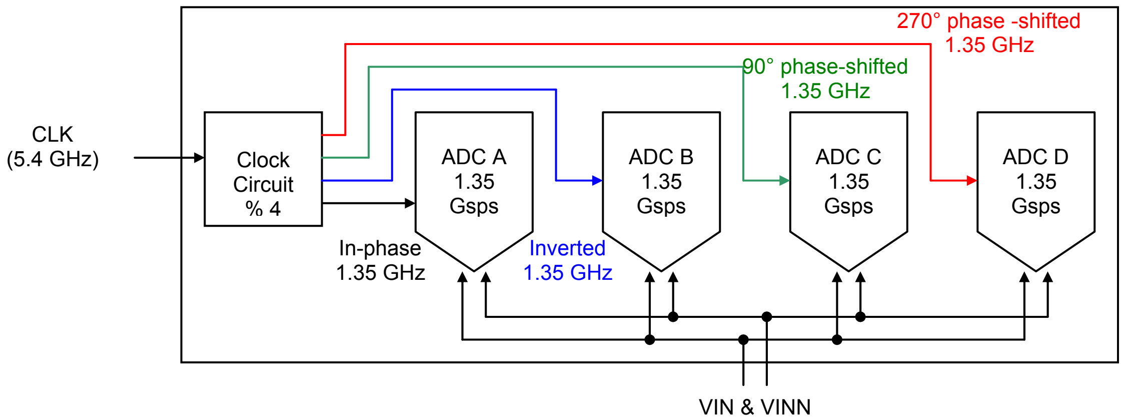


2 Description

The ADC is made up of four identical 12-bit ADC cores where all four ADCs are all interleaved together.
All four ADCs are clocked by the same external input clock signal delayed with the appropriate phase.
The Clock Circuit is common to all four ADCs. This block receives an external 5.4 GHz clock (maximum frequency) and preferably a low jitter sinewave signal. In this block, the external clock signal is then divided by FOUR in order to generate the internal sampling clocks:
The in-phase 1.35 GHz clock is sent to ADC A while the inverted 1.35 GHz clock is sent to ADC B, the in-phase 1.35 GHz clock is delayed by 90° to generate the clock for ADC C and the inverted 1.35 GHz clock is delayed by 90° to generate the clock for ADC D, resulting in an interleaved mode with an equivalent sampling frequency of 5.4 Gsps.

Note: This document and associated documentation are available on http://www.e2v.com/EV12AS350 or through technical support (hotline-bdc@e2v.com). Several adjustments for the sampling delay and the phase are tuned during initial manufacturing test in this clock circuit to ensure a proper phase relation between the different clocks generated internally from the 5.4 GHz clock. Further gain-, phase- and DC offset alignment is achieved with EV12AS350 variants including the ADX4 IP-core. For more information of ADX please contact www.spdevices.com.

Figure 3. Internal interleaving configuration



Notes: 1. For simplification purpose of the timer circuit, the temporary order of ports for sampling is A C B D, therefore sampling order at output port is as follows:

A:	N				N + 4,				N + 8, . .			
C:		N + 1,				N + 5,				N + 9…		
B:			N + 2,				N + 6,				N + 10…	
D:				N + 3,				N + 7,				…

The **T/H** (Track and Hold) is located after the internal 100 ohms impedance and before the ADC cores. This block is used to track the data when the internal sampling clock is low and to hold the data when the internal sampling clock is high.

The **ADC cores** are identical for the four ADCs and each can be powered ON or DOWN individually. Each one includes a quantifier block as well as a fast logic block composed of regenerating latches and the Binary decoding block.

The EV12AS350 ADC is pre-calibrated at factory. It can be used in **staggered mode** (2 or 4 ADC cores interleaved) or in **simultaneous sampling mode** (analog input converted simultaneously by the 1 to 4 ADC cores). In order to use EV12AS350 at its best performance in time-interleaved mode, the ADC cores need to be calibrated between each-others in terms of offset, gain and phase. Several calibration settings are programmed during manufacturing. Some of these settings can be modified by the user via Serial Peripheral Interface (SPI) for best performance according to the application-specific conditions. When using EV12AS350 with ADX4 IP-core, mismatches between the internal ADC cores will automatically be corrected.

The **junction temperature** can be monitored using a diode-mounted transistor but not connected to the die. The diode measures the junction temperature which is 7°C below the hot spot (but higher than die average temperature). Two sets of calibration are pre-programmed (one for cold temperature conditions and another one for ambient and hot temperature conditions) and can be selected via the SPI according to the temperature conditions of the application. However the user can fine tune the ADC calibration settings by changing the calibration values through the SPI.

The **SPI block** provides the digital interface for the digital controls of the ADCs. All the functions of the ADC are accessible and controlled via this SPI (standby mode, test modes, adjustment of different parameters…).

Possible **adjustments of parameters** via the SPI are:

- Selection of **swing on output data** (LVDS standard or reduced swing to save around 180mW)
- **Analog input resistance**
- **Common mode on analog input**
- **Duration of reset** (time during which data ready are set to zero)
- **Flash sequence length** (Test modes)
- **Interlacing gain** (to equalize gain of each ADC channel)
- **Interlacing offset** (to equalize offset of each ADC channel)
- **Interlacing phase** (to equalize phase of each ADC channel)

Two **Test modes** are available via the SPI and can be generated by the ADC: Flash and Ramp. The test modes are used for debug and testability. Flash mode is useful to align the interface between the ADC and the FPGA. In Ramp mode, the data output is a 12 bit ramp on the four ADC cores.
In addition a **PRBS** mode is available and can be used as a test mode or data scrambling.

Frequency of input clock can be divided by two internally. This mode is accessible via the SPI. It can be useful for debug.

It is possible to verify the integrity of OTP (One Time Programmable or fuses) in verifying the **CRC** (Cyclic Redundancy Check) status.

A **SYNC** synchronization signal (LVDS compatible) is mandatory to initialize and synchronize the four ADC cores.

Each ADC core has a **Parity Bit** and an **In Range Bit**

3 Specifications

3.1. Absolute Maximum Ratings

Table 1. Absolute Maximum ratings

Parameter	Symbol	Value		Unit
		Min	Max	
Positive supply voltage 4.8V	V_{CCA}	GND – 0.3	5.3	V
Positive Digital supply voltage 3.2V	V_{CCD}	GND – 0.3	3.6	V
Positive output supply voltage 2.0V	V_{CCO}	GND – 0.3	2.3	V
Analog input peak voltage	V_{IN} or V_{INN}	GND – 0.3	V_{CCA} + 0.3	V
Maximum difference between V_{IN} and V_{INN}	$\| V_{IN} - V_{INN} \|$	2.5		V
Clock input voltage	V_{CLK} or V_{CLKN}	GND – 0.3	V_{CCD} + 0.3	V
Maximum difference between V_{CLK} and V_{CLKN}	$\| V_{CLK} - V_{CLKN} \|$	4		V
SYNC input peak voltage	V_{SYNC} or V_{SYNCN}	GND – 0.3	V_{CCD} + 0.3	V
Maximum difference between V_{SYNC} and V_{SYNCN}	$\| V_{SYNC} - V_{SYNCN} \|$	2		V
SPI input voltage	CSN, SCLK, RSTN, MOSI	-0.3	V_{CCD} + 0.3	V
Junction Temperature	T_J		150	°C

Notes: T_J refers to the junction temperature at the hot spot (refer to Figure 28 for diode temperature measurement).

Parameter	Symbol	Value	Unit
Electrostatic discharge Human Body Model	ESD HBM	2000	V
Electrostatic discharge Charge Device Model	ESD CDM	250	
Latch up		JESD 78D Class I & Class II	
Moisture sensitivity level	MSL	3	
Storage temperature range	Tstg	-55 to +150	°C

Notes: Absolute maximum ratings are limiting values (referenced to GND = 0V), to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum rating may affect device reliability.
All integrated circuits have to be handled with appropriate care to avoid damages due to ESD. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.
Refer to section 7.2 for the power-up sequencing. The power supplies can be switched off in any order.
The power-up of the 3 power supplies has to be completed within a limited time. Long exposure to partial powered ON supplies may damage the device.

3.2. Recommended Conditions Of Use

Table 2. Recommended Conditions of Use

Parameter	Symbol	Comments	Recommended Value	Unit
Positive supply voltage	V_{CCA}	Analog Part	4.8	V
Positive digital supply voltage	V_{CCD}	Analog and Digital parts	3.2	V
Positive Output supply voltage	V_{CCO}	Output buffers and Digital Part	2.0	V
Differential analog input voltage (Full Scale)	V_{IN}, V_{INN} V_{IN} -V_{INN}		±500 1000	mV mVpp
Clock input power level	P_{CLK} P_{CLKN}		+7	dBm
Digital CMOS input	V_D	V_{IL} V_{IH}	0 Vcco	V
Clock frequency	Fc		0.5 ≤ Fc ≤ 5.4	GHz
Operating Temperature Range	T_C; T_J		-40°C < T_C ; T_J < 125°C	°C

Notes: T_J refers to the junction temperature at the hot spot (refer to Figure 28 for diode temperature measurement).

3.3. Explanation of test levels

Test level	Comment
1A	100% tested over specified temperature range and specified power supply range
1B	100% tested over specified temperature range at typical power supplies
1C	100% tested at +25°C over specified supply range
1D	100% tested at +25°C at typical power supplies
2	100% production tested at +25°C(1), and samples tested at specified temperatures.
3	Samples tested only at specified temperatures
4	Parameter value is guaranteed by characterization testing (thermal steady-state conditions at specified temperature).
5	Parameter value is only guaranteed by design

Only MIN and MAX values are guaranteed.

3.4. Electrical Characteristics for supplies, Inputs and Outputs

Unless otherwise specified:
Typical values are given for typical supplies V_{CCA}= 4.8V, V_{CCD} = 3.2V, V_{CCO} = 2.0V at ambient.
Values are given for default modes (4 ADC Cores interleaved with factory calibrations) with Fclk = 5.4 GHz, $P_{CLK,CLKN}$ = -3dBm.

Table 3. Electrical characteristics for Supplies, Inputs and Outputs

Parameter	Test Level	Symbol	Min	Typ	Max	Unit	Note
RESOLUTION				12		bit	
POWER REQUIREMENTS							
Power Supply voltage - Analog - Digital - Output (V_{CCO1} and V_{CCO2})	1A	V_{CCA} V_{CCD} V_{CCO}	4.7 3.1 1.9	4.8 3.2 2.0	4.9 3.3 2.1	V V V	
Power supply currents with reduced swing on output buffers (Reduced Swing Buffer = default mode)							(7)
Power Supply current with 4 ADC cores ON - Analog - Digital @5.4Gsps - Output @5.4Gsps	1A	I_{CCA_RSB} I_{CCD_RSB} I_{CCO_RSB}		265 1390 470	300 1500 550	mA mA mA	(1)
Power Supply current with only 1 ADC Core ON - Analog - Digital @5.4Gsps - Output @5.4Gsps	4	I_{CCA_RSB} I_{CCD_RSB} I_{CCO_RSB}		100 545 130		mA mA mA	(1)
Power Supply current : standby - Analog - Digital - Output	1A	I_{CCA_RSB} I_{CCD_RSB} I_{CCO_RSB}		40 250 13	50 300 70	mA mA mA	(1)
Power dissipation 4 cores ON @5.4Gsps Power dissipation 1 core ON @5.4Gsps Full Standby mode	1A 4 1A	P_{D_RSB}		6.7 2.5 1.1	7.3 1.25	W W W	(1)
Power supply currents with LVDS swing on output buffers							(7)
Power Supply current with 4 ADC cores ON - Analog - Digital @5.4Gsps - Output @5.4Gsps	1A	I_{CCA_LVDS} I_{CCD_LVDS} I_{CCO_LVDS}		265 1390 585	300 1500 620	mA mA mA	(1)
Power Supply current with only 1 ADC core ON - Analog - Digital @5.4Gsps - Output @5.4Gsps	4	I_{CCA_LVDS} I_{CCD_LVDS} I_{CCO_LVDS}		100 545 160		mA mA mA	(1)
Power dissipation 4 cores ON @5.4Gsps Power dissipation 1 core ON @5.4Gsps	1A 4	P_{D_LVDS}		6.9 2.6	7.5	W W	(1)
Maximum number of power-up		NbPWRup	1E6				(2)
ANALOG INPUTS							
Common mode compatibility for analog inputs				AC or DC			
Input Common Mode	1C	CM_{IN} or CMIRef	3.0	3.15	3.4	V	(3)
Full Scale Input Voltage range on each single ended input	4	V_{IN} V_{INN}		500 500		mVpp mVpp	

Parameter	Test Level	Symbol	Min	Typ	Max	Unit	Note
Analog Input power Level (in 100Ω differential termination)	4	$P_{IN, INN}$		+1		dBm	
Input leakage current	5	I_{IN}		40		µA	
Input Resistance (differential)	4	R_{IN}	98	100	102	Ω	(4) (5)
CLOCK INPUTS							
Source Type		Low Phase noise Differential Sinewave					
ADC intrinsic clock jitter	4			150		fs rms	
Clock input common mode voltage	4	CM_{CLK}		1.7		V	
Clock input power level in 100Ω	4	$P_{CLK, CLKN}$	-3	1	+7	dBm	
Clock input voltage on each single ended input (for sinewave clock with F > 4 GHz)	4	V_{CLK} or V_{CLKN}	±158	±250	±500	mV	
Clock input voltage into 100Ω differential clock input (for sinewave clock with F > 4 GHz)	4	$\|V_{CLK} - V_{CLKN}\|$	0.632	1	2	Vpp	
Clock input minimum slew rate (square or sinewave clock)	5	SR_{CLK}	8	12		GV/s	
Clock input capacitance (die + package)	5	C_{CLK}		1		pF	
Clock input resistance (differential)	4	R_{CLK}		100		Ω	
Clock Jitter (max. allowed on external clock source) For 5.4 GHz sinewave analog input	5	Jitter			70	fs rms	
Clock Duty Cycle	4	Duty Cycle	45	50	55	%	
SYNC, SYNCN Signal							
Input Voltages to be applied ▪ Swing ▪ Common Mode	1A	V_{IH}- V_{IL} CM_{SYNC}	100 1.125	350 1.25	450 1.8	mV V	
SYNC, SYNCN input capacitance	5	C_{SYNC}		1		pF	
SYNC, SYNCN input resistance	4	R_{SYNC}		100		Ω	
SPI (CSN, SCLK, RSTN, MOSI)							
CMOS low level of Schmitt trigger	1A	Vtminusc			0.25* V_{CCD}	V	
CMOS high level of Schmitt trigger	1A	Vtplusc	0.65*V_{CCD}			V	
CMOS Schmitt trigger hysteresis	1A	Vhystc	0.10*V_{CCD}			V	
CMOS low level input current (Vinc=0 V)	1A	Iilc			300	nA	
CMOS high level input current (Vinc=V_{CCD} max)	1A	Iihc			1000	nA	
SPI (MISO)							
CMOS low level output voltage (Iolc = 3 mA)	1A	Volc			0.20*V_{CCD}	V	
CMOS high level output voltage (Iohc = 3 mA)	1A	Vohc	0.8*V_{CCD}			V	
DIGITAL DATA and DATA READY OUTPUTS							
Logic Compatibility			LVDS				
Output levels with normal swing mode 50Ω transmission lines, 100Ω (2 x 50Ω) differential termination ▪ Logic low ▪ Logic high ▪ Differential output ▪ Common mode	1A	V_{OL} V_{OH} V_{OH}- V_{OL} V_{OCM}	 1.35 210 1.20	1.28 1.55 260 1.42	1.60 310 1.70	V V mV V	(6) (7)
Output levels with reduced swing mode = default mode 50Ω transmission lines, 100Ω (2 x 50Ω) differential termination ▪ Logic low ▪ Logic high ▪ Differential output ▪ Common mode	1A	V_{OL} V_{OH} V_{OH} - V_{OL} V_{OCM}	 1.3 170 1.20	1.32 1.54 220 1.43	1.65 270 1.70	V V mV V	(6)

Notes:

1. Maximum currents are obtained with maximum supplies and maximum temperature
2. Maximum number of power-up is limited by the maximum number of OTP reading.
3. The DC analog common mode voltage is provided by ADC.
   CMIRef can be adjusted thanks to SPI.

CMIRef= 0.656*V_{CCA}+(16-SPIcode)*12mV with SPIcode ranging between 0 and 31. See section 5.14
Min and Max values are given for SPIcode=16 (default value)

4. For optimal performance in term of VSWR, analog input transmission lines must be 100Ω differential and analog input resistance must be digitally trimmed to cope with process deviation.
5. The Analog input impedance is trimmed during manfucaturing. User can modify R_{IN} via the SPI. See section 5.13. Min and Max values are given for SPI default value.
6. Maximum single ended load capacitance has to be less than 5 pF
7. Swing can be adjusted via SPI. See section 5.12.

3.5. Converter Characteristics

Unless otherwise specified:
Typical values are given for typical supplies V_{CCA}= 4.8V, V_{CCD} = 3.2V, V_{CCO} = 2.0V at ambient.
-1 dBFS Analog input.
Clock input differentially driven; analog input differentially driven.
Values are given for default modes (4 ADC Cores interleaved with factory calibrations) with Fclk = 5.4 GHz, $P_{CLK,CLKN}$ = -3dBm..

Table 4. INL & Gain Characteristics

Parameter	Test Level	Symbol	Min	Typ	Max	Unit	Note
DC ACCURACY							
Gain dispersion from part to part	5	Go			+/- 1.5	dB	(1)
Gain variation versus temperature	4	G(T)			+/- 0.5	dB	
Typical Input offset voltage (4 ADC cores interleaved) at ambient with typical supplies	1B	OFFSET	2023	2048	2073	LSB	(2)
INL & DNL							
DNLrms	1D	DNLrms		0.3	0.45	LSB	(3)
Differential non linearity	1D	DNL+		1.0	1.8	LSB	
Differential non linearity	1D	DNL-	-0.9	-0.76		LSB	
INLrms	1D	INLrms		0.7	0.95	LSB	
Integral non linearity	1D	INL+		2.2	3.5	LSB	
Integral non linearity	1D	INL-	-3.5	-2.2		LSB	

Notes:

1. Gain central value is measured at Fin = 100 MHz. This value corresponds to the maximum deviation from part to part of different wafer batches.
2. Measured at 5.4 Gsps Fin = 1900MHz -1dBFS.During factory calibration all parts can not be calibrated to 2048. The min and max values represents the possible excursion of calibrated offset in typical conditions.
3. Measured at 5.4 Gsps Fin = 100MHz -1dBFS with 4 ADC Cores interleaved. DNL being better than -0.9LSB, no missing code is guaranteed.

Table 5. Dynamic Characteristics

Parameter	Test Level	Symbol	Min	Typ		Max	Unit	Note
AC ANALOG INPUTS								
Full Power Input Bandwidth	4	FPBW		4.8			GHz	
Gain Flatness (+/- 0.5 dB)	4	GF		1700			MHz	
Input Voltage Standing Wave Ratio up to 3.0 GHz up to 4.8 GHz	4	VSWR		 1.5:1 2.0:1				
DYNAMIC PERFORMANCE over first Nyquist zone (single tone at -1 dBFS) 4 cores interleaved (Staggered mode)								
Effective Number Of Bits 5.4 Gsps Fin = 100 MHz 5.4 Gsps Fin = 1900 MHz 5.4 Gsps Fin = 2690 MHz	 1D 1D 1D	ENOB	 8.1 7.9 7.1	**w/o ADX4** 8.9 8.3 7.4	**w/ ADX4** 9.1 8.3 7.4		Bit_FS	(3)
Spurious Free Dynamic Range (interleaving spurs included) 5.4 Gsps Fin = 100 MHz 5.4 Gsps Fin = 1900 MHz 5.4 Gsps Fin = 2690 MHz	 1D 1D 1D	|SFDR|	 57 53 46	**w/o ADX4** 64 58 50	**w/ ADX4** 76 58 50		dBFS	(3)

Parameter	Test Level	Symbol	Min	Typ		Max	Unit	Note
Signal to Noise Ratio								
5.4 Gsps Fin = 100 MHz	1D	|SNR|	54.5	57.5			dBFS	(1)
5.4 Gsps Fin = 1900 MHz	1D		52.5	53.2				
5.4 Gsps Fin = 2690 MHz	1D		50.5	51.1				
Signal to Noise and Distorsion				**w/o ADX4**	**w/ ADX4**			
5.4 Gsps Fin = 100 MHz	1D	|SINAD|	50	55	56		dBFS	(1) (3)
5.4 Gsps Fin = 1900 MHz	1D		48	51	51			
5.4 Gsps Fin = 2690 MHz	1D		43	46	46			
Total Harmonic Distorsion								
5.4 Gsps Fin = 100 MHz	1D	|THD|	64	68			dBFS	(1)
5.4 Gsps Fin = 1900 MHz	1D		54	56				
5.4 Gsps Fin = 2690 MHz	1D		45	48				
Total Interleaving Distorsion				**w/o ADX4**	**w/ ADX4**			
5.4 Gsps Fin = 100 MHz	1D	|TILD|	54	63	72		dBFS	(1) (3) (4)
5.4 Gsps Fin = 1900 MHz	1D		53	62	71			
5.4 Gsps Fin = 2690 MHz	1D		52	60	60			
DYNAMIC PERFORMANCE over first Nyquist zone (single tone at -3 dBFS) 4 cores interleaved (Staggered mode)								
Effective Number Of Bits				**w/o ADX4**	**w/ ADX4**			
5.4 Gsps Fin = 100 MHz	1D	ENOB	8.4	9.0	9.0		Bit_FS	(1) (3)
5.4 Gsps Fin = 1900 MHz	1D		8.1	8.6	8.6			
5.4 Gsps Fin = 2690 MHz	1D		7.6	8.1	8.1			
5.4 Gsps Fin = 4200 MHz	4			7.0	7.0			
Spurious Free Dynamic Range (interleaving spurs included)				**w/o ADX4**	**w/ ADX4**			
5.4 Gsps Fin = 100 MHz	1D	|SFDR|	58	67	77		dBFS	(1) (3)
5.4 Gsps Fin = 1900 MHz	1D		54	64	64			
5.4 Gsps Fin = 2690 MHz	1D		52	56	56			
5.4 Gsps Fin = 4200 MHz	4			46	46			
Signal to Noise Ratio								
5.4 Gsps Fin = 100 MHz	1D	|SNR|	54.5	57.1			dBFS	(1)
5.4 Gsps Fin = 1900 MHz	1D		53.5	54.5				
5.4 Gsps Fin = 2690 MHz	1D		51.5	52.9				
5.4 Gsps Fin = 4200 MHz	4			50.0				
Signal to Noise and Distorsion				**w/o ADX4**	**w/ ADX4**			
5.4 Gsps Fin = 100 MHz	1D	|SINAD|	53	56	56		dBFS	(1) (3)
5.4 Gsps Fin = 1900 MHz	1D		51	53	53			
5.4 Gsps Fin = 2690 MHz	1D		47	50	50			
5.4 Gsps Fin = 4200 MHz	4			44	44			
Total Harmonic Distorsion								
5.4 Gsps Fin = 100 MHz	1D	|THD|	64	71			dBFS	(1)
5.4 Gsps Fin = 1900 MHz	1D		59	63				
5.4 Gsps Fin = 2690 MHz	1D		51	54				
5.4 Gsps Fin = 4200 MHz	4			45				
Total Interleaving Distorsion				**w/o ADX4**	**w/ ADX4**			
5.4 Gsps Fin = 100 MHz	1D	|TILD|	55	65	73		dBFS	(1) (3) (4)
5.4 Gsps Fin = 1900 MHz	1D		56	64	73			
5.4 Gsps Fin = 2690 MHz	1D		53	62	62			
5.4 Gsps Fin = 4200 MHz	4			54	54			
DYNAMIC PERFORMANCE over first Nyquist zone (single tone at -6 dBFS) 4 cores interleaved (Staggered mode)								
Effective Number Of Bits				**w/o ADX4**	**w/ ADX4**			
5.4 Gsps Fin = 100 MHz	1D	ENOB	8.4	9.1	9.2		Bit_FS	(1) (3)
5.4 Gsps Fin = 1900 MHz	1D		8.3	8.9	8.9			
5.4 Gsps Fin = 2690 MHz	1D		8.1	8.5	8.5			
5.4 Gsps Fin = 4200 MHz	4			7.8	7.8			
Spurious Free Dynamic Range (interleaving spurs included)				**w/o ADX4**	**w/ ADX4**			
5.4 Gsps Fin = 100 MHz	1D	|SFDR|	59	69	80		dBFS	(1) (3)
5.4 Gsps Fin = 1900 MHz	1D		59	68	75			
5.4 Gsps Fin = 2690 MHz	1D		56	64	64			
5.4 Gsps Fin = 4200 MHz	4			55	55			
Signal to Noise Ratio								
5.4 Gsps Fin = 100 MHz	1D	|SNR|	54.5	57.5			dBFS	(1)
5.4 Gsps Fin = 1900 MHz	1D		54.5	55.7				
5.4 Gsps Fin = 2690 MHz	1D		53.5	54.5				
5.4 Gsps Fin = 4200 MHz	4			52.5				
Signal to Noise and Distorsion				**w/o ADX4**	**w/ ADX4**			
5.4 Gsps Fin = 100 MHz	1D	|SINAD|	53	56	56		dBFS	(1) (3)
5.4 Gsps Fin = 1900 MHz	1D		53	55	55			
5.4 Gsps Fin = 2690 MHz	1D		51	53	53			
5.4 Gsps Fin = 4200 MHz	4			49	49			

Parameter	Test Level	Symbol	Min	Typ		Max	Unit	Note
Total Harmonic Distorsion 5.4 Gsps Fin = 100 MHz 5.4 Gsps Fin = 1900 MHz 5.4 Gsps Fin = 2690 MHz 5.4 Gsps Fin = 4200 MHz	 1D 1D 1D 4	|THD|	 64 64 57	 71 69 62 53			dBFS	(1) (3)
Total Interleaving Distorsion 5.4 Gsps Fin = 100 MHz 5.4 Gsps Fin = 1900 MHz 5.4 Gsps Fin = 2690 MHz 5.4 Gsps Fin = 4200 MHz	 1D 1D 1D 4	|TILD|	 56 56 55	**w/o ADX4** 67 66 64 58	**w/ ADX4** 76 75 64 58		dBFS	(1) (3) (4)
DYNAMIC PERFORMANCE (dual tone at -7 dBFS each) **4 cores interleaved (Staggered mode)**								
IMD 5.4 Gsps Fin1 = 2600 MHz_Fin2 = 2610 MHz	4	IMD		57			dBFS	(1)
DYNAMIC PERFORMANCE (dual tone at -9 dBFS each) **4 cores interleaved (Staggered mode)**								
IMD 5.4 Gsps Fin1 = 2600 MHz_Fin2 = 2610 MHz	4	IMD		63			dBFS	(1)
DYNAMIC PERFORMANCE (dual tone at -12 dBFS each) **4 cores interleaved (Staggered mode)**								
IMD 5.4 Gsps Fin1 = 2600 MHz_Fin2 = 2610MHz 5.4 Gsps Fin1 = 4790 MHz_Fin2 = 4800MHz	 4 4	IMD		 72 52			dBFS	(1)
DYNAMIC PERFORMANCE (Noise Power Ratio) **4 cores interleaved**								
Noise Power Ratio 1st Nyquist Pattern from 800 MHz to 2200 MHz Notch frequency = 1300 MHz Notch width = 25 MHz	4	NPR		48			dB	(1)
DYNAMIC PERFORMANCE (single tone at -1 dBFS) **4 cores in parallel (Simultaneous mode)** 1st value is **without averaging /** 2nd value is **with real time averaging** of 4 cores 5.4 GHz external clock, each core running at 1.35 Gsps								
Effective Number Of Bits 5.4 GHz ➔ 1.35Gsps Fin = 100 MHz 5.4 GHz ➔ 1.35Gsps Fin = 1900 MHz 5.4 GHz ➔ 1.35Gsps Fin = 2690 MHz	1D	ENOB	 8.6 / 9.3 7.9 / 8.4 7.1 / 7.3	 9.1 / 9.8 8.3 / 8.7 7.4 / 7.6			Bit_FS	(1) (2)
Spurious Free Dynamic Range 5.4 GHz ➔ 1.35Gsps Fin = 100 MHz 5.4 GHz ➔ 1.35Gsps Fin = 1900 MHz 5.4 GHz ➔ 1.35Gsps Fin = 2690 MHz	1D	|SFDR|	 63 / 67 54 / 54 46 / 46	 72 / 73 58 / 58 49 / 49			dBFS	(1)
Signal to Noise Ratio 5.4 GHz ➔ 1.35Gsps Fin = 100 MHz 5.4 GHz ➔ 1.35Gsps Fin = 1900 MHz 5.4 GHz ➔ 1.35Gsps Fin = 2690 MHz	1D	|SNR|	 55.0 / 59.5 51.5 / 55.5 49.5 / 52.5	 57.1 / 61.9 52.2 / 56.8 50.9 / 54.1			dBFS	(1) (2)
Signal to Noise and Distorsion 5.4 GHz ➔ 1.35Gsps Fin = 100 MHz 5.4 GHz ➔ 1.35Gsps Fin = 1900 MHz 5.4 GHz ➔ 1.35Gsps Fin = 2690 MHz	1D	|SINAD|	 53 / 58 49 / 52 44 / 45	 56 / 60 51 / 54 46 / 47			dBFS	(1)
Total Harmonic Distorsion 5.4 GHz ➔ 1.35Gsps Fin = 100 MHz 5.4 GHz ➔ 1.35Gsps Fin = 1900 MHz 5.4 GHz ➔ 1.35Gsps Fin = 2690 MHz	1D	|THD|	 59 / 62 53 / 53 45 / 45	 66 / 68 57 / 57 48 / 48			dBFS	(1)
DYNAMIC PERFORMANCE (single tone at -3 dBFS) **4 cores in parallel (Simultaneous mode)** 1st value is **without averaging /** 2nd value is **with real time averaging** of 4 cores 5.4 GHz external clock, each core running at 1.35 Gsps								
Effective Number Of Bits 5.4 GHz ➔ 1.35Gsps Fin = 100 MHz 5.4 GHz ➔ 1.35Gsps Fin = 1900 MHz 5.4 GHz ➔ 1.35Gsps Fin = 2690 MHz 5.4 GHz ➔ 1.35Gsps Fin = 4200 MHz	 1D 1D 1D 4	ENOB	 8.8 / 9.6 8.3 / 8.9 7.8 / 8.1	 9.2 / 10.0 8.6 / 9.2 8.0 / 8.3 7.0 / 7.3			Bit_FS	(1) (2)
Spurious Free Dynamic Range 5.4 GHz ➔ 1.35Gsps Fin = 100 MHz 5.4 GHz ➔ 1.35Gsps Fin = 1900 MHz 5.4 GHz ➔ 1.35Gsps Fin = 2690 MHz 5.4 GHz ➔ 1.35Gsps Fin = 4200 MHz	 1D 1D 1D 4	|SFDR|	 64 / 69 59 / 61 52 / 52	 74 / 77 64 / 64 55 / 55 46 / 47			dBFS	(1)

Parameter	Test Level	Symbol	Min	Typ	Max	Unit	Note
Signal to Noise Ratio 5.4 GHz ➔ 1.35Gsps Fin = 100 MHz 5.4 GHz ➔ 1.35Gsps Fin = 1900 MHz 5.4 GHz ➔ 1.35Gsps Fin = 2690 MHz 5.4 GHz ➔ 1.35Gsps Fin = 4200 MHz	 1D 1D 1D 4	|SNR|	 55.5 / 60.5 52.5 / 56.5 51.5 / 55.5	 57.4 / 62.4 54.4 / 58.3 52.7 / 56.2 50.0 / 53.3		dBFS	(1) (2)
Signal to Noise and Distorsion 5.4 GHz ➔ 1.35Gsps Fin = 100 MHz 5.4 GHz ➔ 1.35Gsps Fin = 1900 MHz 5.4 GHz ➔ 1.35Gsps Fin = 2690 MHz 5.4 GHz ➔ 1.35Gsps Fin = 4200 MHz	 1D 1D 1D 4	|SINAD|	 54 / 59 51 / 55 48 / 50	 57 / 61 53 / 57 50 / 52 44 / 46		dBFS	(1)
Total Harmonic Distorsion 5.4 GHz ➔ 1.35Gsps Fin = 100 MHz 5.4 GHz ➔ 1.35Gsps Fin = 1900 MHz 5.4 GHz ➔ 1.35Gsps Fin = 2690 MHz 5.4 GHz ➔ 1.35Gsps Fin = 4200 MHz	 1D 1D 1D 4	|THD|	 61 / 64 58 / 59 51 / 51	 68 / 71 62 / 63 53 / 54 45 / 46		dBFS	(1)
DYNAMIC PERFORMANCE (single tone at -6 dBFS) **4 cores in parallel (Simultaneous mode)** 1st value is **without averaging /** 2nd value is **with real time averaging** of 4 cores 5.4 GHz external clock, each core running at 1.35 Gsps							
Effective Number Of Bits 5.4 GHz ➔ 1.35Gsps Fin = 100 MHz 5.4 GHz ➔ 1.35Gsps Fin = 1900 MHz 5.4 GHz ➔ 1.35Gsps Fin = 2690 MHz 5.4 GHz ➔ 1.35Gsps Fin = 4200 MHz	 1D 1D 1D 4	ENOB	 8.9 / 9.1 8.6 / 9.3 8.3 / 8.8	 9.2 / 10.0 8.9 / 9.6 8.6 / 9.1 7.9 / 8.3		Bit_FS	(1) (2)
Spurious Free Dynamic Range 5.4 GHz ➔ 1.35Gsps Fin = 100 MHz 5.4 GHz ➔ 1.35Gsps Fin = 1900 MHz 5.4 GHz ➔ 1.35Gsps Fin = 2690 MHz 5.4 GHz ➔ 1.35Gsps Fin = 4200 MHz	 1D 1D 1D 4	|SFDR|	 65 / 71 63 / 66 57 / 59	 75 / 78 72 / 73 64 / 64 54 / 55		dBFS	(1)
Signal to Noise Ratio 5.4 GHz ➔ 1.35Gsps Fin = 100 MHz 5.4 GHz ➔ 1.35Gsps Fin = 1900 MHz 5.4 GHz ➔ 1.35Gsps Fin = 2690 MHz 5.4 GHz ➔ 1.35Gsps Fin = 4200 MHz	 1D 1D 1D 4	|SNR|	 56.0 / 61.0 54.5 / 58.5 52.5 / 56.5	 57.7 / 62.7 55.9 / 60.1 54.4 / 58.2 52.7 / 55.9		dBFS	(1) (2)
Signal to Noise and Distorsion 5.4 GHz ➔ 1.35Gsps Fin = 100 MHz 5.4 GHz ➔ 1.35Gsps Fin = 1900 MHz 5.4 GHz ➔ 1.35Gsps Fin = 2690 MHz 5.4 GHz ➔ 1.35Gsps Fin = 4200 MHz	 1D 1D 1D 4	|SINAD|	 55 / 59 53 / 57 51 / 54	 57 / 61 55 / 59 53 / 56 50 / 52		dBFS	(1)
Total Harmonic Distorsion 5.4 GHz ➔ 1.35Gsps Fin = 100 MHz 5.4 GHz ➔ 1.35Gsps Fin = 1900 MHz 5.4 GHz ➔ 1.35Gsps Fin = 2690 MHz 5.4 GHz ➔ 1.35Gsps Fin = 4200 MHz	 1D 1D 1D 4	|THD|	 61 / 64 59 / 63 55 / 57	 68 / 71 66 / 68 61 / 61 53 / 54		dBFS	(1)

Notes:

1. See definition of terms in section 3.8.
2. Theoretical gain due to averaging is +1 bit on ENOB and +6dB on SNR. However, as 4 ADC cores are not perfectly matched, the actual gain is lower.
3. Performance enhancement of EV12AS350 with ADX4 is active from DC up to 2300 MHz.
4. TILD may be subject to variation over the ADC life time and environment conditions. It could potentially affect ENOB, SFDR and SINAD. To keep the same level of performance, the Offset, Gain and Phase adjustments of the ADC cores can be re-calibrated as described in section 5.8.5. An other option is to use ADX4 IP.

3.6. Timing and switching characteristics

Unless otherwise specified:
Typical values are given for typical supplies V_{CCA}= 4.8V, V_{CCD} = 3.2V, V_{CCO} = 2.0V at ambient.
-1 dBFS Analog input.
Clock input differentially driven; analog input differentially driven.
Values are given for default modes (4 ADC Cores interleaved with factory calibrations) with Fclk = 5.4 GHz, $P_{CLK,CLKN}$ = -3dBm..

Table 6. Transient and Switching Characteristics

Parameter	Test Level	Symbol	Value	Unit	Note
SWITCHING PERFORMANCE					
Maximum operating clock frequency with CLOCK_DIV2 = 0 with CLOCK_DIV2 = 1 (clock divided by 2)	1B	$F_{CLK\ MAX}$	5400 5400	MHz	(1) (2)
Minimum operating Clock frequency with CLOCK_DIV2 = 0 with CLOCK_DIV2 = 1 (clock divided by 2)	4	$F_{CLK\ MIN}$	100 200	MHz	(1)
CER	4	CER	10^{-12}		(3)

Notes

1. Functionality CLOCK_DIV2 enables to divide by 2 in the frequency of the clock signal applied to the ADC. See section 5.10.
2. For optimum dynamic performance, it is recommended to have a clock frequency higher than 500MHz
3. Output error amplitude > 128 LSB (3% of the full-scale). At 60°C, -10dBFS.

Table 7. Timing Characteristics

Parameter	Test Level	Symbol	Min	Typ	Max	Unit	Note
TIMING CHARACTERISTICS							
Aperture Delay	4	TA		140		ps	
ADC Aperture uncertainty	4	Jitter		150		fs rms	
Output rise time for DATA (20%-80%)	4	TR		250		ps	(1) (2)
Output fall time for DATA (20%-80%)	4	TF		250		ps	(1) (2)
Output rise time for DATA READY (20%-80%)	4	TR		250		ps	(1) (2)
Output fall time for DATA READY (20%-80%)	4	TF		250		ps	(1) (2)
Output Data Pipeline Delay = TPD+TOD	4	TPD	26 cc	26 cc	26 cc	external clock cycles	(1) (3)
	4	TOD		2.4		ns	(1)
Data Ready Reset delay ADC core A ADC core C ADC core B ADC core D	4	TPDRA TPDRC TPDRB TPDRD		33 cc 34 cc 35 cc 36 cc		external clock cycles	(1) (3)
		TRDR		2.7		ns	
Data to Data Ready delay	4	TD1	2 cc – 40ps				(1) (4) (5)
Data Ready to Data delay	4	TD2	2 cc – 90ps				(1) (4) (5)
Minimum SYNC pulse width	4	TSYNC_MIN	32 cc			external clock cycles	(3) (6)
Maximum SYNC pulse width	5	TSYNC_MAX		-	-	ns	(7)
SYNC slew rate	5	SR_{SYNC}	500			MV/s	
SYNC forbidden area lower bound SYNC forbidden area upper bound	4	T1 T2	 90	115 100	125	ps	(8)

Notes:

1. See definition of terms in section 3.8.
2. 50Ω // CLOAD = 2pF termination (for each single-ended output). Termination load parasitic capacitance derating value: 50ps/pF (ECL).
3. cc = external clock cycle at full speed
4. See section 3.6.2. for description of TD1/TD2
5. Measured with 3.6GHz < Fclk < 5.4 GHz
6. See timing diagram on section 5.6
7. There is no maximum SYNC pulse width. Only the SYNC rising edge is taken into account.
8. Refer to Figure 8 for T1 and T2 definition

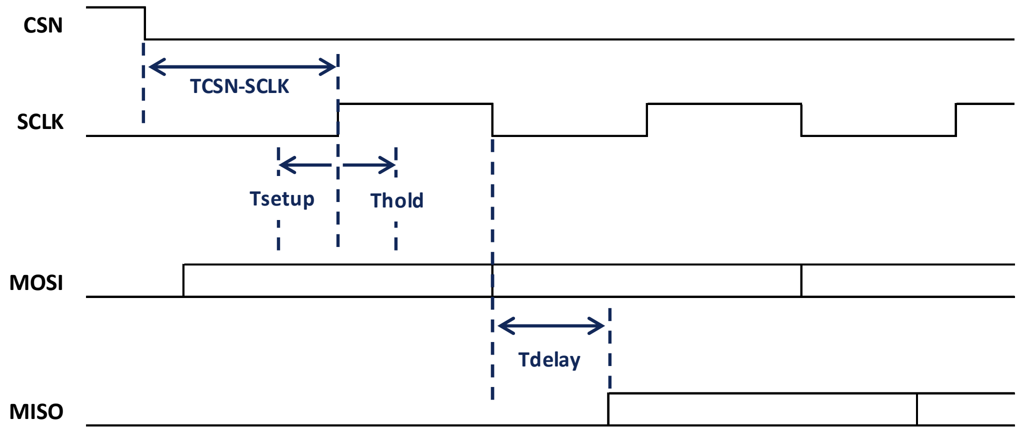
Table 8. SPI Timing Characteristics

Parameter	Test Level	Symbol	Value			Unit	Note
			Min	Typ	Max		
SPI new access availability after stand-by exit	1A	T_{STDBY}	100			µs	(1)
RSTN pulse duration	5	T_{RSTN}	10			µs	
SCLK frequency	1A	F_{SCLK}			50	MHz	
CSN to SCLK delay	5	$T_{CSN-SCLK}$	0.5			T_{SCLK}	
MISO setup time	5	T_{setup}	3			ns	
MISO hold time	5	T_{hold}	3			ns	
MOSI output delay With 5pF load With 50pF load	 5 5	T_{delay}			 6 9	ns	

Notes:

1. When exiting the stand-by mode, it is necessary to wait T_{STDBY} before doing a new SPI access

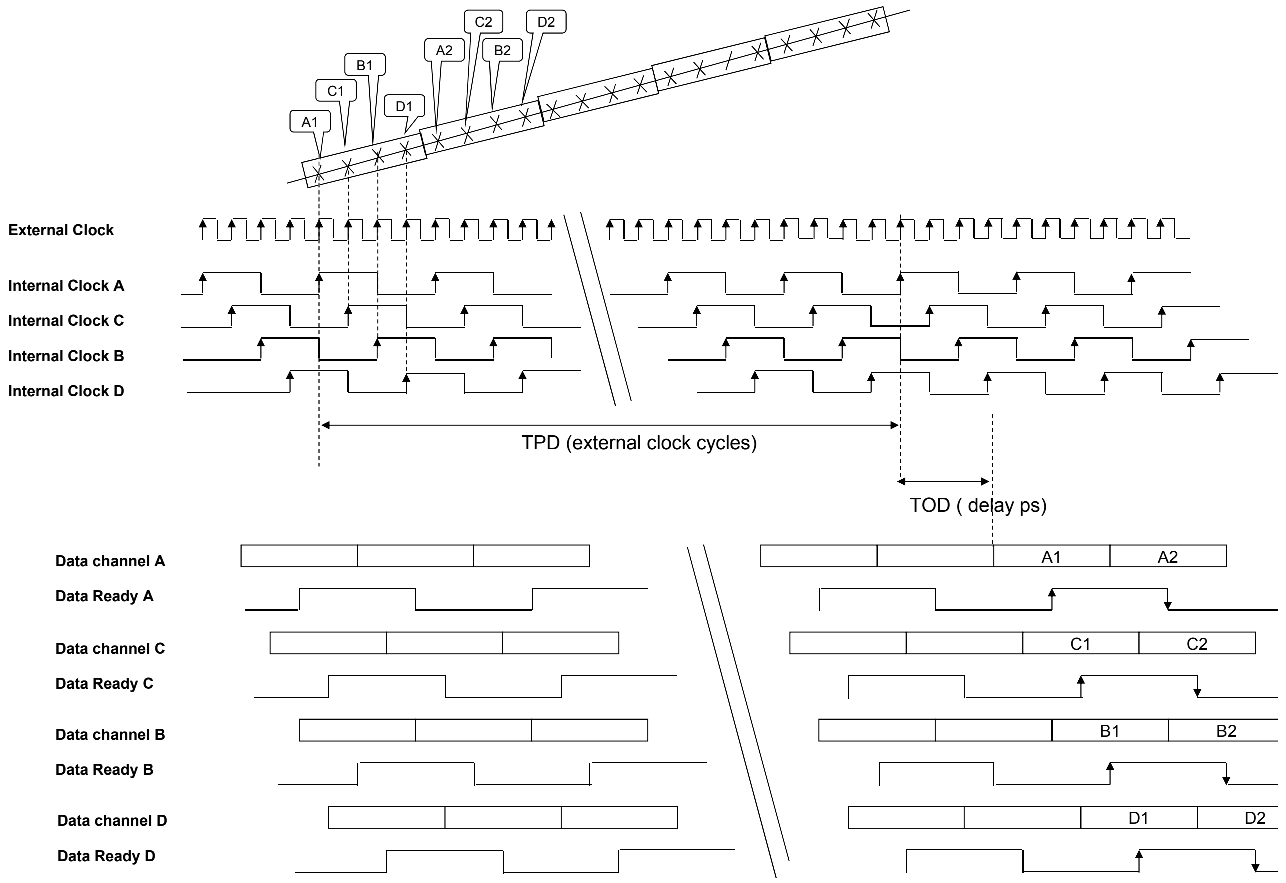
Figure 4. SPI Timing Diagram



3.6.1. Timing diagrams for functional mode

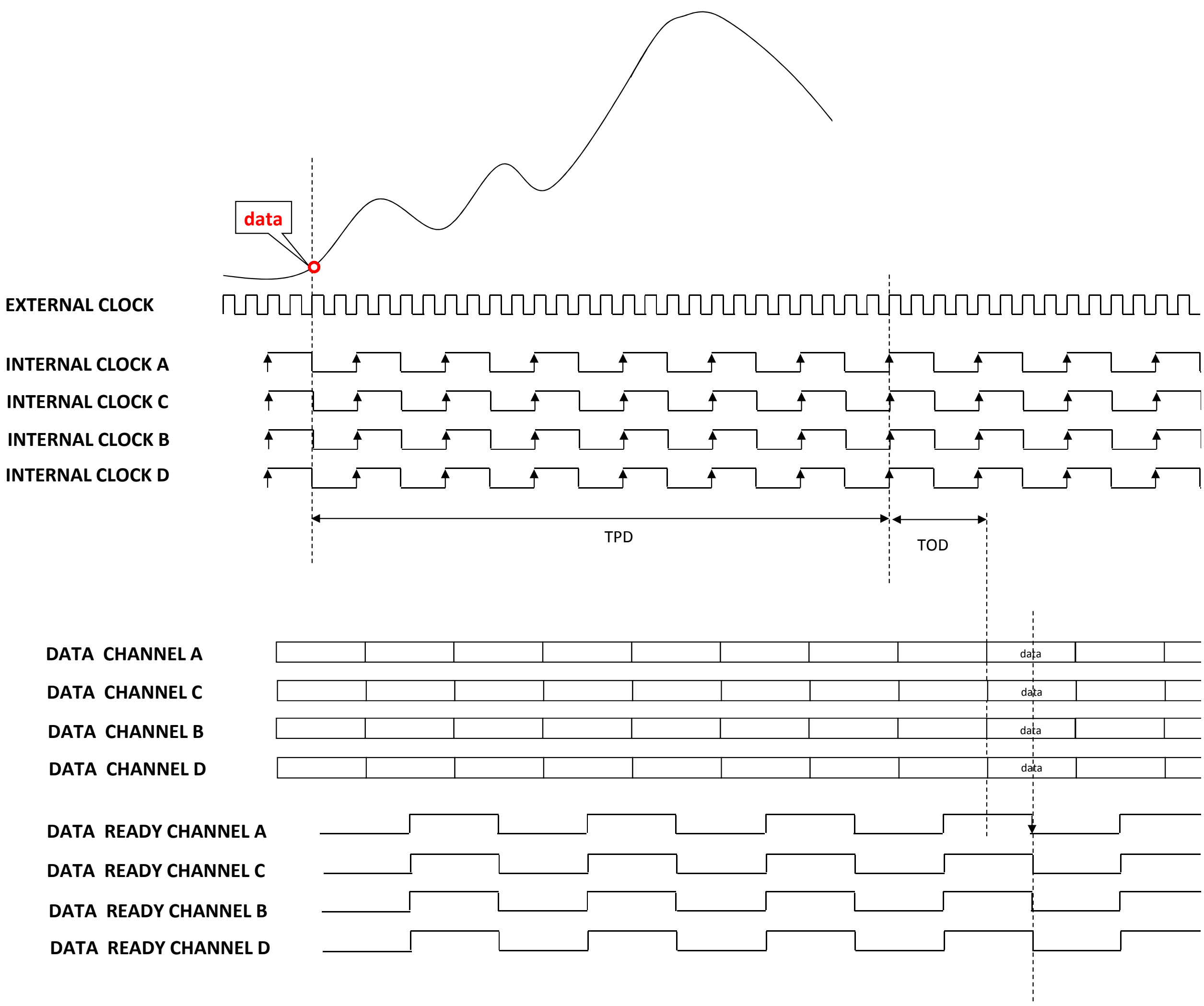
For the information on the reset sequence (using SYNC, SYNCN signals), please refer to section 5.6.
The functional mode is the default mode, no programming is needed.

Figure 5. ADC Timing in staggered mode (4 ADC cores interleaved)



TPD +TOD = OUTPUT DATA PIPELINE DELAY

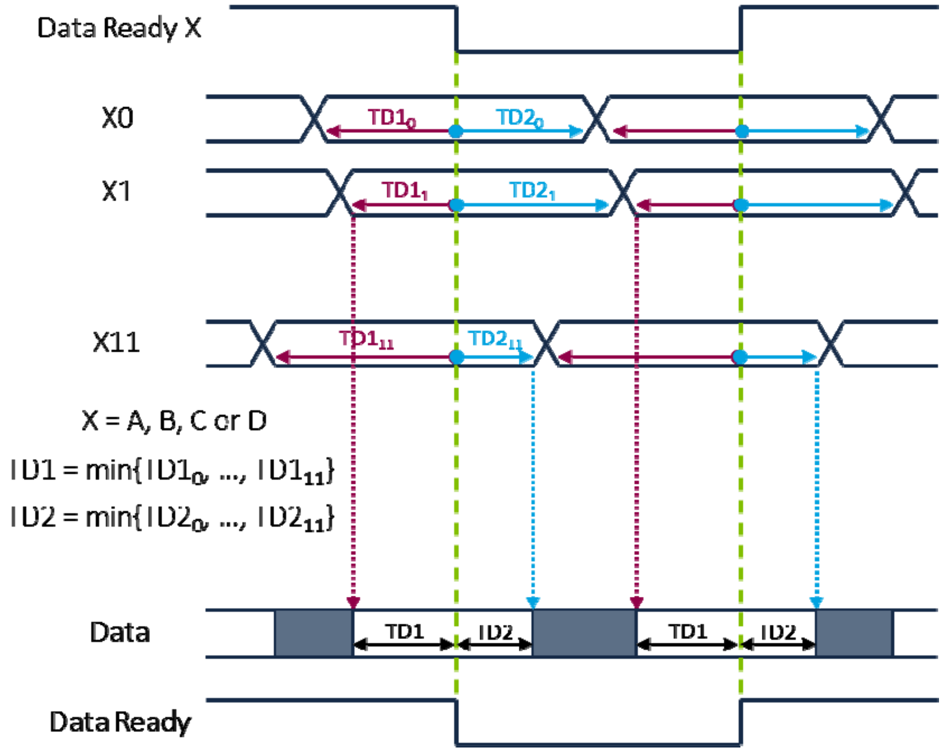
Figure 6. ADC Timing in simultaneous mode or simultaneous sampling (4 ADC cores sampling the same signal)



TPD +TOD = OUTPUT DATA PIPELINE DELAY

3.6.2. Centering of Data Ready on output data timing (TD1/TD2)

Figure 7. Centering of Data Ready signal on output data



3.6.3. SYNC edges forbidden zone (T1/T2)

Figure 8. SYNC edges forbidden zone

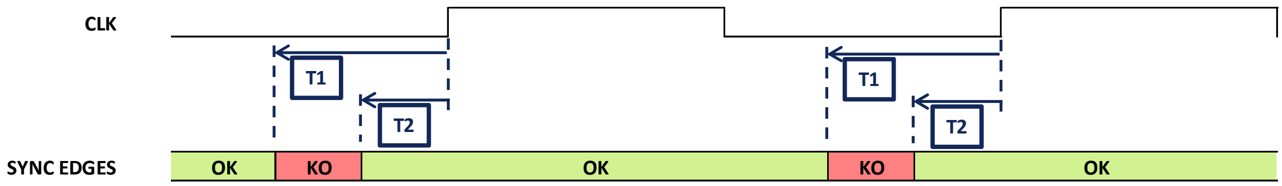
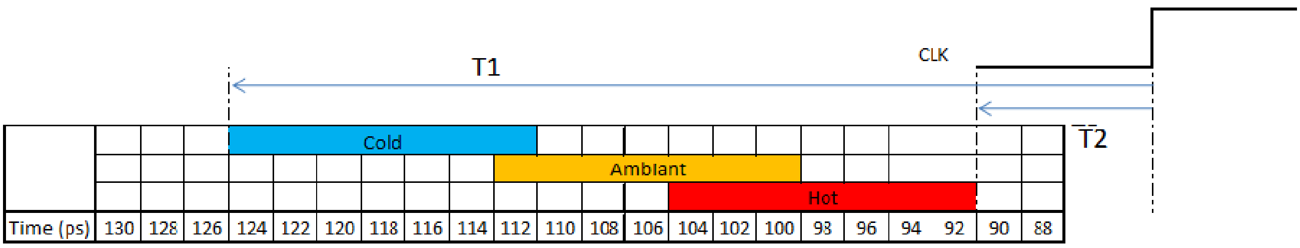


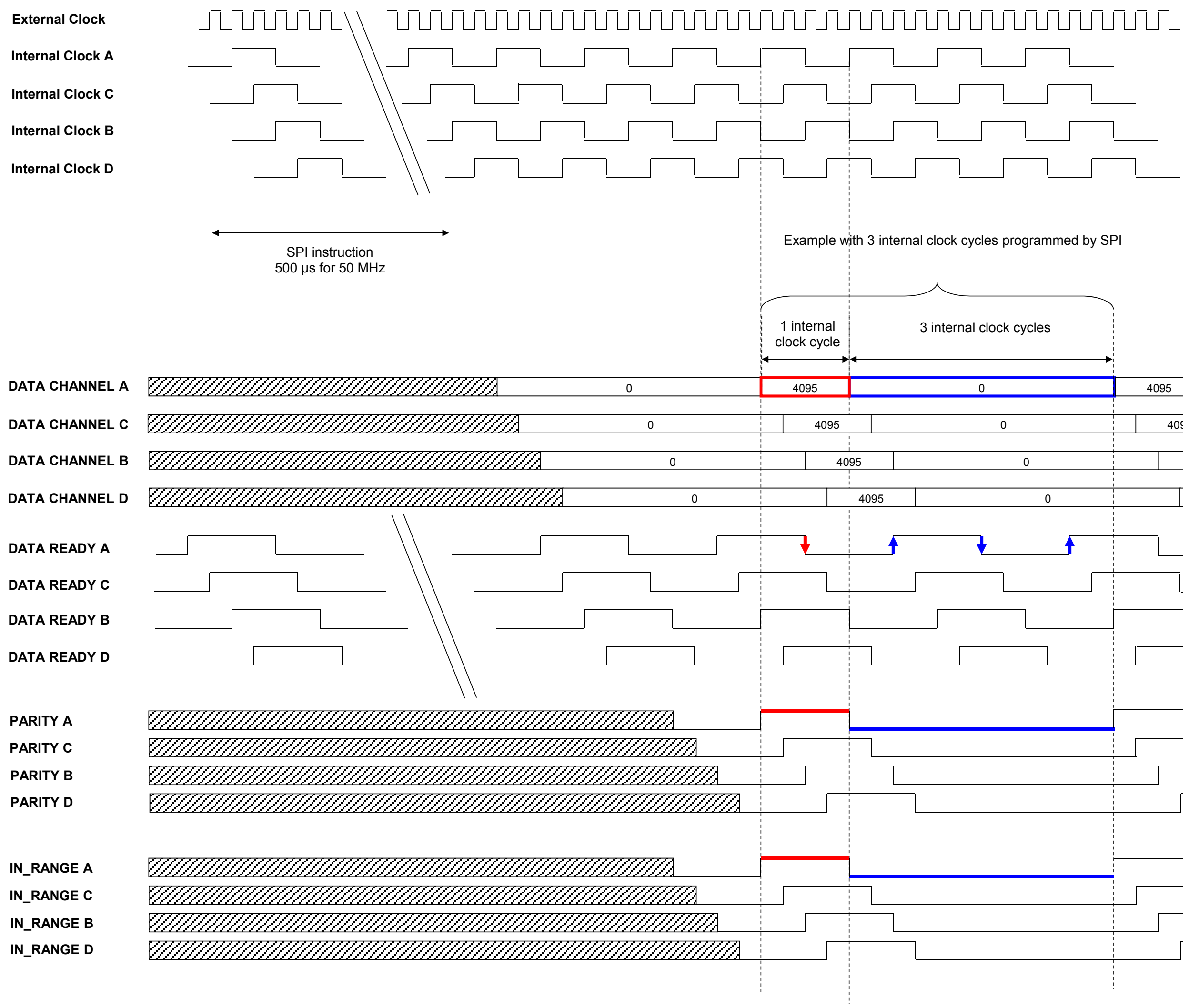
Figure 9. SYNC edges forbidden zone versus temperature



3.6.4. Timing diagram for Flash mode

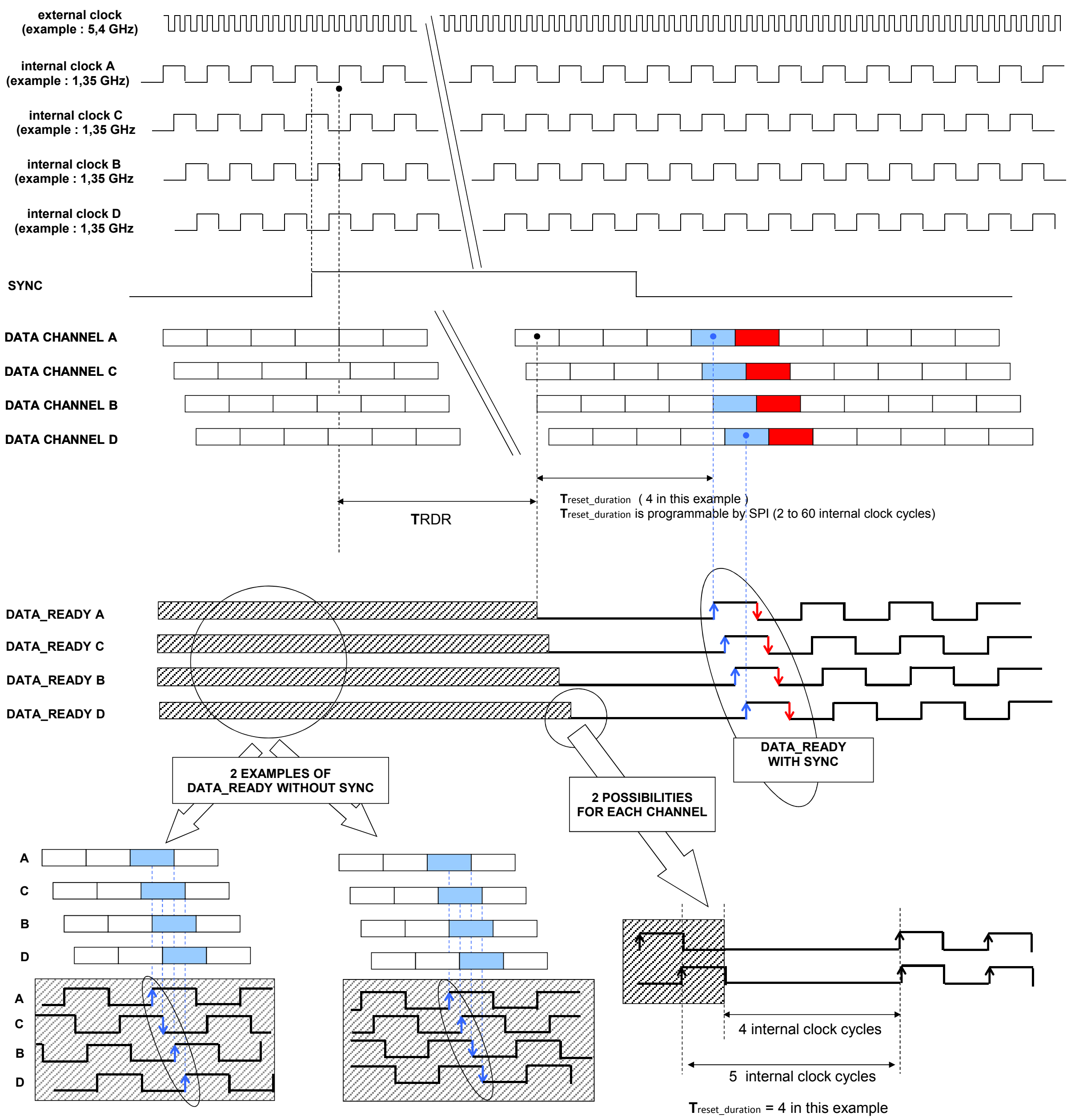
Flash mode can be used to synchronize ADC with a FPGA.
Flash mode starts immediately after the end of the SPI Writing.

Figure 10. ADC Timing in Flash mode with 4 ADC cores interleaved



Example with FLASH_LENGTH = 3
1 internal clock cycle = 4 external clock cycles

Figure 11. ADC Timing in flash mode with 4 ADC cores sampling the same signal



Example with FLASH_LENGTH=3
1 internal clock cycle = 4 external clock cycles

3.6.5. Timing diagram for Ramp mode

The Ramp mode can be used in order to have a visual way to debug.

Figure 12. ADC Timing in ramp mode with 4 ADC cores interleaved

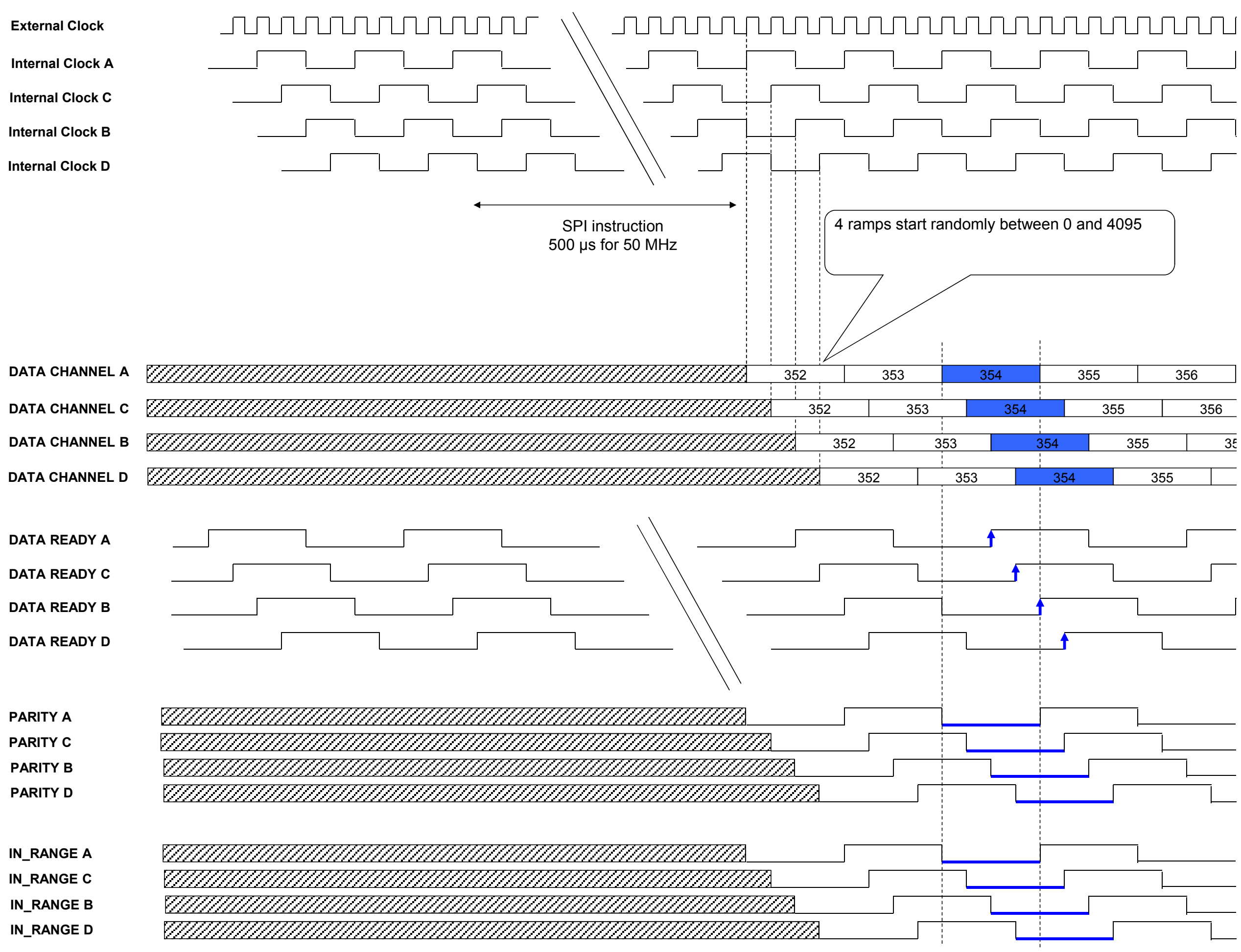
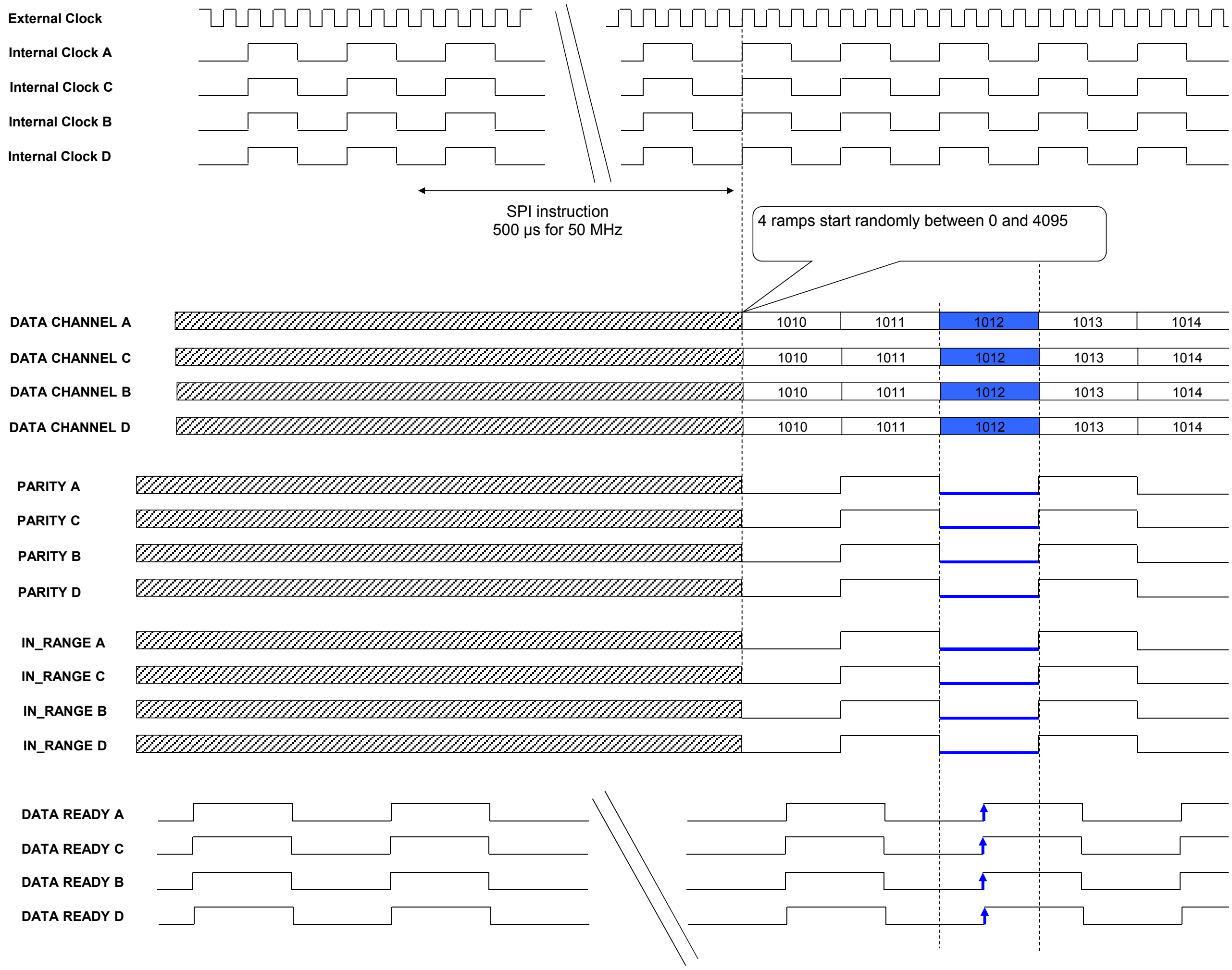


Figure 13. ADC Timing in ramp mode with 4 ADC cores sampling the same signal



3.7. Digital Output Coding

Table 9. ADC Digital output coding table

Differential analog input	Voltage level	Binary MSB (bit 11).........LSB(bit 0)	In-Range
> + 500.125 mV	>Top end of full scale + ½ LSB	1 1 1 1 1 1 1 1 1 1 1 1	0
+ 500.125 mV + 500 mV	Top end of full scale + ½ LSB Top end of full scale - ½ LSB	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0	1 1
+ 0.125 mV - 0.125 mV	Mid scale + ½ LSB Mid scale - ½ LSB	1 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1	1 1
- 500 mV -500.125 mV	Bottom end of full scale + ½ LSB Bottom end of full scale - ½ LSB	0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0	1 1
< - 500.125 mV	< Bottom end of full scale - ½ LSB	0 0 0 0 0 0 0 0 0 0 0 0	0

In-Range output bit is flagged to level 0 when the analog input exceeds the ADC Full-Scale. In that condition, output code is clamped to code 0 or 4095.

3.8. Definition of Terms

Abbreviation	Term	Definition
(CER)	*Code Error Rate*	Probability to exceed a specified error threshold for a sample at maximum specified sampling rate.
(DNL)	*Differential non linearity*	The Differential Non Linearity for an output code i is the difference between the measured step size of code i and the ideal LSB step size. DNL (i) is expressed in LSBs. DNL is the maximum value of all DNL (i). DNL error specification of less than 1 LSB guarantees that there are no missing output codes and that the transfer function is monotonic.
(ENOB)	*Effective Number Of Bits*	$ENOB = \frac{SINAD - 1.76 + 20 \log (A / FS/2)}{6.02}$ Where A is the actual input amplitude and FS is the full scale range of the ADC under test
(FPBW)	*Full power input bandwidth*	Analog input frequency at which the fundamental component in the digitally reconstructed output waveform has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis) for input at Full Scale –1 dB (- 1 dBFS).
(Fs max)	*Maximum Sampling Frequency*	Value for which functionality and performance are no more guaranteed above this frequency.
(Fs min)	*Minimum Sampling frequency*	Sampling frequency for which the ADC begins to have loss in distortion. Performances are not guaranteed below this frequency.
(IMD)	*InterModulation Distortion*	The two tones intermodulation distortion (IMD) rejection is the ratio of either input tone to the worst third order intermodulation products.
(INL)	*Integral non linearity*	The Integral Non Linearity for an output code i is the difference between the measured input voltage at which the transition occurs and the ideal value of this transition. INL (i) is expressed in LSBs, and is the maximum value of all |INL (i)|.
(JITTER)	*Aperture uncertainty*	Sample to sample variation in aperture delay. The voltage error due to jitter depends on the slew rate of the signal at the sampling point.
(NPR)	*Noise Power Ratio*	The NPR is measured to characterize the ADC performance in response to broad bandwidth signals. When applying a notch-filtered broadband white-noise signal as the input to the ADC under test, the Noise Power Ratio is defined as the ratio of the average out-of-notch to the average in-notch power spectral density magnitudes for the FFT spectrum of the ADC output sample test.
(ORT)	*Overvoltage Recovery Time*	Time to recover 0.2 % accuracy at the output, after a 150 % full scale step applied on the input is reduced to midscale
(OTP)	*One Time Programmable*	OTP are fuses used to set circuit default configuration and calibrations
(SFDR)	*Spurious free dynamic range*	Ratio expressed in dBFS of the RMS signal amplitude to the RMS value of the highest spectral component (peak spurious spectral component). The peak spurious component may or may not be a harmonic.
(SINAD)	*Signal to noise and distortion ratio*	Ratio expressed in dBFS of the RMS signal amplitude to the RMS sum of all other spectral components, including the harmonics and interleaving spurs except DC.
(SNR)	*Signal to noise ratio*	Ratio expressed in dBFS of the RMS signal amplitude to the RMS sum of all other spectral components excluding the twenty five first harmonics and interleaving spurs.
(T1, T2)	*SYNC forbidden zone*	T1 and T2 represents setup and hold time on the SYNC input brought back to the input of the package
(TA)	*Aperture delay*	Delay between the rising edge of the differential clock inputs (CLK, CLKN) (zero crossing point), and the time at which (XAI, XAIN where X = A, B C or D) is sampled.
(TC)	*Encoding clock period*	TC1 = Minimum clock pulse width (high) TC = TC1 + TC2 TC2 = Minimum clock pulse width (low)
(TD)	*Total Distortion*	TD expressed in dBFS is the root square quadratic sum of THD and TILD expressed in dBFS
(TD1)	*Time delay from Data transition to Data Ready*	General expression is TD1 = TC1 + TDR – TOD with TC = TC1 + TC2 = 1 encoding clock period.
(TD2)	*Time delay from Data*	General expression is TD2 = TC2 + TDR – TOD with TC = TC1 + TC2 = 1 encoding

	Ready to Data	clock period.
(TDR)	*Data ready output delay*	Delay from the rising edge of the differential clock inputs (CLK, CLKN) (zero crossing point) to the next point of change in the differential output data (zero crossing) with specified load.
(THD)	*Total harmonic distortion*	Ratio expressed in dBFS of the RMS sum of the first twenty five harmonic components, to the RMS input signal amplitude.
(TF)	*Fall time*	Time delay for the output DATA signals to fall from 20% to 80% of delta between low level and high level.
(TILD)	*Total Interleaving Distortion*	Ratio expressed in dBFS of the RMS sum of all interleaving spurs (Fc/4±Fin, Fc/2-Fin, Fc/4), to the RMS input signal amplitude.
(TOD)	*Digital data Output delay*	Delay from the rising edge of the differential clock inputs (CLK, CLKN) (zero crossing point) to the next point of change in the differential output data (zero crossing) with specified load (not taking into account TPD delay).
(TPD)	*Pipeline delay/latency*	Number of clock cycles between the sampling edge of an input data and the associated output data being made available (not taking into account TOD delay)
(TPDR)	*Pipeline Delay*	Pipeline Delay between the falling edge of the external clock after reset (SYNC, SYNCN) and the reset to digital zero transition of the Data Ready output signal (XDR, where X = A, B, C or D).
(TR)	*Rise time*	Time delay for the output DATA signals to rise from 20% to 80% of delta between low level and high level.
(TRDR)	*Data Ready reset delay*	Delay between the falling edge of the external clock after reset (SYNC, SYNCN) and the reset to digital zero transition of the Data Ready output signal (XDR, where X = A, B, C or D) not taking into account the TPDR pipeline delay.
(TSYNC)	*SYNC duration*	External SYNC pulse width needed for SYNC function
(VSWR)	*Voltage Standing Wave Ratio*	The VSWR corresponds to the ADC input reflection loss due to input power reflection. For example a VSWR of 1.2:1 (or 1.2) corresponds to a 20dB return loss (ie. 99% power transmitted and 1% reflected).

4 Pin Description

4.1. Pinout View (Bottom view)

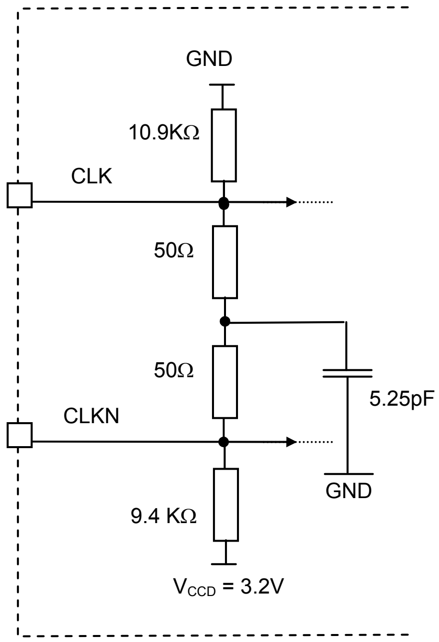
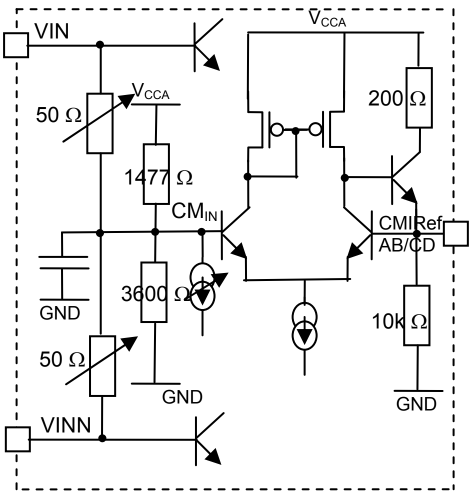
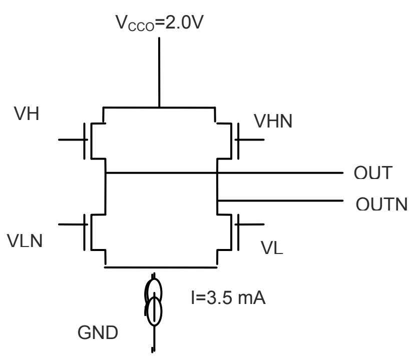
Figure 14. Pinout View

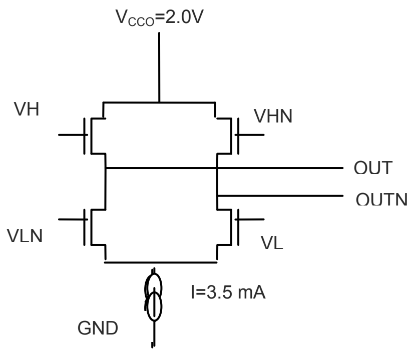
AD	GND	VCCD	BBP	BDR	BIR	GND	DiodeA	GND	GND	SYNCP	GND	CLK	CLKN	GND	DNC	sclk	mosi	VCCO2	GND	CIR	CDR	CBP	VCCD	GND
AC	GND	VCCD	BBPN	BDRN	BIRN	GND	DiodeC	NC	GND	SYNCN	GND	GND	GND	GND	rstn	csn	miso	VCCO2	GND	CIRN	CDRN	CBPN	VCCD	GND
AB	B11	B11N	VCCD	GND	VCCD	GND	VCCD	GND	GND	VCCD	VCCD	GND	GND	VCCD	VCCD	GND	GND	VCCD	GND	VCCD	GND	VCCD	C11N	C11
AA	B10	B10N	VCCD	GND	VCCO1	VCCD	VCCD	GND	GND	VCCD	VCCD	GND	GND	VCCD	VCCD	GND	GND	VCCD	VCCD	VCCO1	GND	VCCD	C10N	C10
Y	B9	B9N	VCCO1	GNDO	GNDO	VCCO1	VCCD	GND	GND	VCCD	VCCD	GND	GND	VCCD	VCCD	GND	GND	VCCD	VCCO1	GNDO	GNDO	VCCO1	C9N	C9
W	B8	B8N	VCCO1	GNDO	GNDO															GNDO	GNDO	VCCO1	C8N	C8
V	B6	B6N	B7	B7N	GNDO															GNDO	C7N	C7	C6N	C6
U	B4	B4N	B5	B5N	VCCO1															VCCO1	C5N	C5	C4N	C4
T	B2	B2N	B3	B3N	GND															GND	C3N	C3	C2N	C2
R	B0	B0N	B1	B1N	VCCD															VCCD	C1N	C1	C0N	C0
P	GND	GND	NC	GND	VCCD															VCCD	GND	NC	GND	GND
N	VCCA	GND	VCCA	GND	VCCD															VCCD	GND	VCCA	GND	VCCA
M	VCCA	GND	VCCA	GND	VCCD															VCCD	GND	VCCA	GND	VCCA
L	GND	GND	NC	GND	VCCD															VCCD	GND	NC	GND	GND
K	A0	A0N	A1	A1N	VCCD															VCCD	D1N	D1	D0N	D0
J	A2	A2N	A3	A3N	GND															GND	D3N	D3	D2N	D2
H	A4	A4N	A5	A5N	VCCO1															VCCO1	D5N	D5	D4N	D4
G	A6	A6N	A7	A7N	GNDO															GNDO	D7N	D7	D6N	D6
F	A8	A8N	VCCO1	GNDO	GNDO															GNDO	GNDO	VCCO1	D8N	D8
E	A9	A9N	VCCO1	GNDO	GNDO	VCCO1	VCCD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VCCD	VCCO1	GNDO	GNDO	VCCO1	D9N	D9
D	A10	A10N	VCCD	GND	VCCO1	VCCD	VCCD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VCCD	VCCD	VCCO1	GND	VCCD	D10N	D10
C	A11	A11N	VCCD	GND	VCCD	VCCD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VCCD	VCCD	GND	VCCD	D11N	D11
B	GND	VCCD	ABPN	ADRN	AIRN	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	DIRN	DDRN	DBPN	VCCD	GND
A	GND	VCCD	ABP	ADR	AIR	GND	CMIRef AB	CMIRef CD	GND	GND	GND	VIN	VINN	GND	GND	GND	NC	NC	GND	DIR	DDR	DBP	VCCD	GND
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24

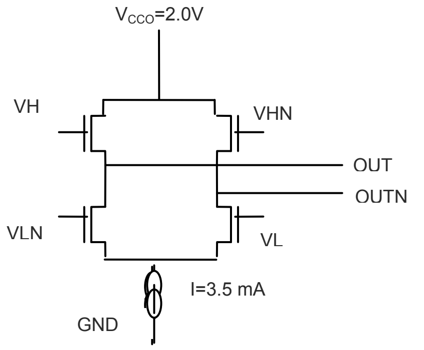
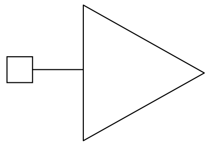
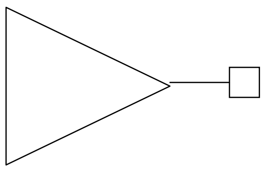
4.2. Pinout Table

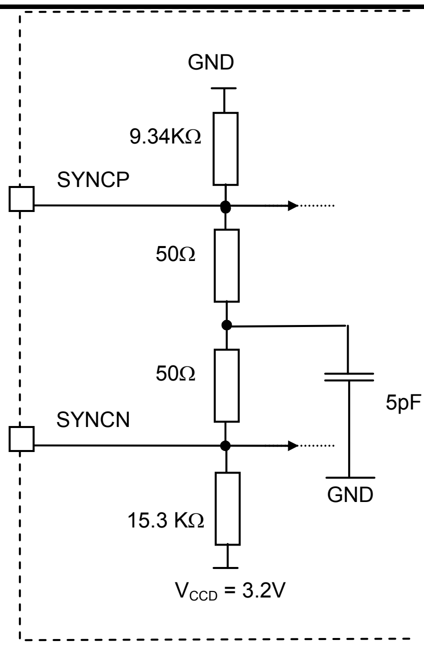
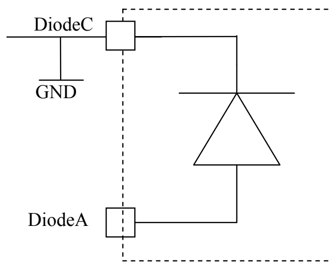
Table 10. Pinout Table

Pin Label	Pin number	Description	Direction	Simplified electrical schematics
Power supplies				
GND	A1,B1,L1,P1,AC1,AD1, L2,P2,M2,N2, C4,D4,,L4,M4,N4,P4 AA4,AB4, J5,T5, A6,B6,AB6,AC6,AD6, B7,C7, B8,C8,D8,E8,Y8,AA8,AB8, AD8, A9,B9,C9,D9,E9,Y9,AA9,AB9,A C9,AD9, A10,B10,C10,D10,E10, A11,B11,C11,D11,E11,AC11, AD11, B12,C12,D12,E12,Y12,AA12, AB12,AC12, B13,C13,D13,E13,Y13,AA13, AB13,AC13, A14,B14,C14,D14,E14,AC14, AD14, A15,B15,C15,D15,E15, A16,B16,C16,D16,E16,Y16, AA16,AB16, B17,C17,D17,E17,Y17,AA17, AB17, B18,C18, A19,B19,AB19,AC19,AD19, J20,T20, C21,D21, L21,M21,N21,P21,AA21,AB21, L23, M23,N23,P23, A24,B24,L24,P24,AC24,AD24	Ground		All ground pins (GND and GNDO) must be connected to a one solid ground plane on board (Common ground)
GNDO	E4, F4,W4,Y4, E5, F5,G5,V5,W5,Y5, E20,F20,G20,V20,W20,Y20 E21, F21,W21,Y21	Ground for Digital outputs		
VCCA	M1,N1,M3,N3,M22,N22, M24,N24	Analog power supply (4.8V)		
VCCD	A2,B2,AC2,AD2, C3,D3,AA3,AB3, C5,K5,L5,M5,N5,P5,R5,AB5, C6,D6,AA6, D7,E7,Y7,AA7,AB7, Y10,AA10,AB10, Y11,AA11,AB11, Y14,AA14,AB14, Y15,AA15,AB15, D18,E18,Y18,AA18,AB18, C19,D19,AA19, C20,K20,L20,M20,N20,P20,R20, AB20 C22,D22,AA22,AB22, A23,B23,AC23,AD23,	Digital power supply (3.2V)		
VCCO1	E3,F3,W3,Y3, D5,H5,U5,AA5, E6,Y6, E19,Y19,D20,H20,U20,AA20, E22,F22,W22,Y22,	Output power supply (2.0V)		GNDO referenced
VCCO2	AC18, AD18,	Digital power supply (2.0V)		Note: GND referenced
Clock signal				

Pin Label	Pin number	Description	Direction	Simplified electrical schematics
CLK CLKN	AD12, AD13	In phase and Out of phase input clock signal	I	
Analog input signals				
VIN VINN	A12 A13	In phase analog input Out of phase analog input	I	
CMIREFAB CMIREFCD	A7, A8	Output voltage reference In AC coupling operation this output could be left floating (not used) In DC coupling operation, these pins provides an output voltage witch is the common mode voltage for the analog input signal and should be used to set the common mode voltage of the input driving buffer.	O	
Digital Output signals				
A0, A0N A1, A1N A2, A2N A3, A3N A4, A4N A5, A5N A6, A6N A7, A7N A8, A8N A9, A9N A10, A10N A11, A11N	K1, K2 K3, K4 J1, J2 J3, J4 H1, H2 H3, H4 G1, G2 G3, G4 F1, F2 E1, E2 D1, D2 C1, C2	Channel A in phase output data A0 is the LSB, A11 is the MSB Channel A out of phase output data A0N is the LSB, A11N is the MSB	O	
ABP, ABPN	A3, B3	Channel A output parity bit ABP Channel A out of phase parity bit ABPN	O	
AIR, AIRN	A5, B5	Channel A In Range bit AIR Channel A out of phase In Range bit AIRN	O	

Pin Label	Pin number	Description	Direction	Simplified electrical schematics
ADR ADRN	A4, B4	Channel A Output clock (Data Ready clock in DDR mode)	O	
B0, B0N B1, B1N B2, B2N B3, B3N B4, B4N B5, B5N B6, B6N B7, B7N B8, B8N B9, B9N B10, B10N B11, B11N	R1, R2 R3, R4 T1, T2 T3, T4 U1, U2 U3, U4 V1, V2 V3, V4 W1, W2 Y1, Y2 AA1, AA2 AB1, AB2	Channel B in phase output data B0 is the LSB, B11 is the MSB Channel B out of phase output data B11N is the LSB, B11N is the MSB	O	
BBP, BBPN	AD3, AC3	Channel B output parity bit BBP Channel B out of phase parity bit BBPN	O	
BIR, BIRN	AD5, AC5	Channel B In Range bit BIR Channel B Out of phase In Range bit BIRN	O	
BDR, BDRN	AD4, AC4	Channel B Output clock (Data Ready clock in DDR mode)	O	
C0, C0N C1, C1N C2, C2N C3, C3N C4, C4N C5, C5N C6, C6N C7, C7N C8, C8N C9, C9N C10, C10N C11, C11N	R24, R23 R22, R21 T24, T23 T22, T21 U24, U23 U22, U21 V24, V23 V22, V21 W24, W23 Y24, Y23 AA24, AA23 AB24, AB23	Channel C in phase output data C0 is the LSB, C11 is the MSB Channel C out of phase output data C0N is the LSB, C11N is the MSB	O	
CBP, CBPN	AD22, AC22	Channel C output parity bit CPB Channel C out of phase parity bit CPBN	O	
CIR, CIRN	AD20, AC20	Channel C In Range bit CIR Channel C out of phase In Range bit CIRN	O	
CDR CDRN	AD21, AC21	Channel C Output clock (Data Ready clock in DDR mode)	O	
D0, D0N D1, D1N D2, D2N D3, D3N D4, D4N D5, D5N D6, D6N D7, D7N D8, D8N D9, D9N D10, D10N D11, D11N	K24, K23 K22, K21 J24, J23 J22, J21 H24, H23 H22, H21 G24, G23 G22, G21 F24, F23 E24, E23 D24, D23 C24, C23	Channel D in phase output data D0 is the LSB, D11 is the MSB Channel D out of phase output data D0N is the LSB, D11N is the MSB	O	
DBP, DBPN	A22, B22	Channel D output parity bit DBP Channel D out of phase parity bit DBPN	O	

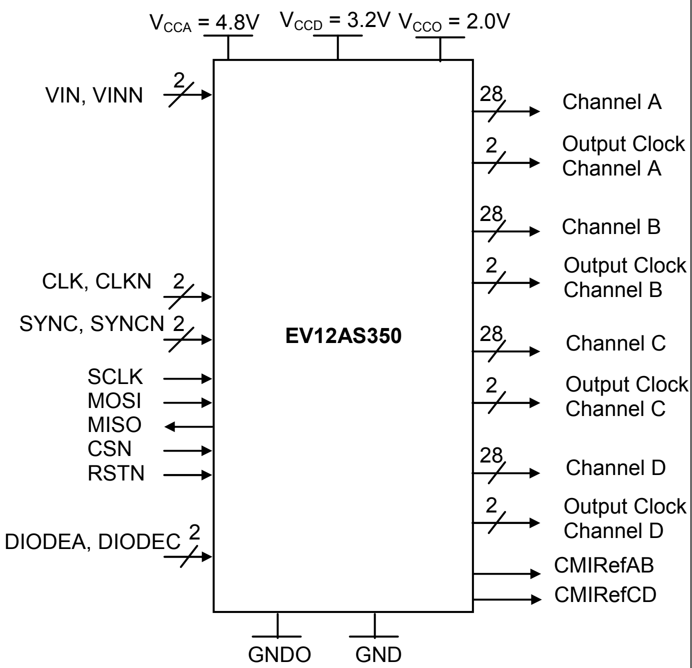
Pin Label	Pin number	Description	Direction	Simplified electrical schematics
DIR, DIRN	A20, B20	Channel D In Range bit DIR Channel D out of phase In Range bit DIRN	O	
DDR DDRN	A21, B21	Channel D Output clock (Data Ready clock in DDR mode)	O	
SPI signals				
csn	AC16	SPI signal Input Chip Select signal (Active low) When this signal is active low, sclk is used to clock data present on MOSI or MISO signal Refer to section 5.2 for more information	I	 Non-inverting CMOS Schmitt-trigger input
sclk	AD16	SPI signal Input SPI serial Clock Serial data is shifted into and out SPI synchronously to this signal on positive transition of sclk Refer to section 5.2 for more information	I	
mosi	AD17	SPI signal Data SPI Input signal (Master Out Slave In) Serial data input is shifted into SPI while csn is active low Refer to section 5.2 for more information	I	
rstn	AC15	SPI signal Input Digital asynchronous SPI reset (Active low) This signal allows to reset the internal value of SPI to their default value Refer to section 5.2 for more information	I	
miso	AC17	SPI signal Data output SPI signal (Master In Slave Out) Serial data output is shifted out SPI while sldn is active low. MISO not tristated when inactive Refer to section 5.2 for more information	O	 Output Pad 80Ohm 4mA
Other signals				

Pin Label	Pin number	Description	Direction	Simplified electrical schematics
SYNCP SYNCN	AD10 AC10	Differential Input Synchronization signal (LVDS) Active high signal This signal is used to synchronize internal ADC, Refer to section 5.7.1. for more information Equivalent internal differential 100Ω input resistor	I	
DiodeA, DiodeC	AD7,AC7	Temperature diode Anode Temperature diode Cathode Refer to section 5.22 for more information. Note: it is mandatory to connect DiodeC to GND.	I	
NC	A17,A18,AC8,AD15, L3, P3, L22, P22,	Do Not Connect		

5 Theory Of Operation

5.1. Overview

Table 11. Functional Description



Name	Function		
V_{CCA}	4.8V Power		
V_{CCO}	2.0V Output Power Supply		
V_{CCD}	3.2V Digital Power Supply		
GND	Ground		
GNDO	Ground for digital outputs		
VIN,VINN	Differential Analog Input		
CLK,CLKN	Differential Clock Input		
[A0:A11] [A0N:A11N]	Channel A Differential Output Data		
AIR, AIRN	Channel A Differential In Range bit		
ABP, ABPN	Channel A Differential bit parity		
ADR, ADRN	Channel A Data Ready Differential Output Clock		
[B0:B11] [B0N:B11N]	Channel B Differential Output Data		
BIR, BIRN	Channel B Differential In Range bit		
BBP, BBPN	Channel B Differential bit parity		
BDR, BDRN	Channel B Data Ready Differential Output Clock		
[C0:C11] [C0N:C11N]	Channel C Differential Output Data		
CIR, CIRN	Channel C Differential In Range bit		
CBP, CBPN	Channel C Differential bit parity		
CDR, CDRN	Channel C Data Ready Differential Output Clock		
[D0:D11] [D0N:D11N]	Channel D Differential Output Data		
DIR, DIRN	Channel D Differential In Range bit		
DBP, DBPN	Channel D Parity bit	CSN	Chip Select Input (Active Low)
DDR, DDRN	Channel D Data Ready Differential Output Clock	RSTN	SPI Asynchronous Reset Input (Active Low)
SYNCP, SYNCN	Synchronization of Data Ready (LVDS input)	MOSI	SPI input Data (Master Out Slave In)
SCLK	SPI Input Clock	DIODEA	Diode Anode Input for die junction temperature monitoring
MISO	SPI Output Data (Master In Slave Out) MISO should be pulled up to Vcc using 1K – 3K3 resistor Note: MISO not tristated when inactive	DIODEC	Diode Cathode Input for die junction temperature monitoring
CMIRefAB	Output voltage Reference for Input common Mode reference Core A & B	CMIRefCD	Output voltage Reference for Input common Mode reference Core C & D

5.2. ADC Digital Interface (SPI: Serial Peripheral Interface)

The digital interface is a SPI with:

- 8 bits for the address A[7:0] including a Read Write bit
  A[7]is the MSB and the Read Write bit, A[0] is the LSB
- 16 bits of data D[15:0] with D[15] the MSB and D[0] the LSB.
- Half Duplex mode (see timing below)

5 signals are required:

- RSTN for the SPI reset;
- SCLK for the SPI clock;
- CSN for the Chip Select;
- MISO for the Master In Slave Out (SPI output)
- MOSI for the Master Out Slave In (SPI input)

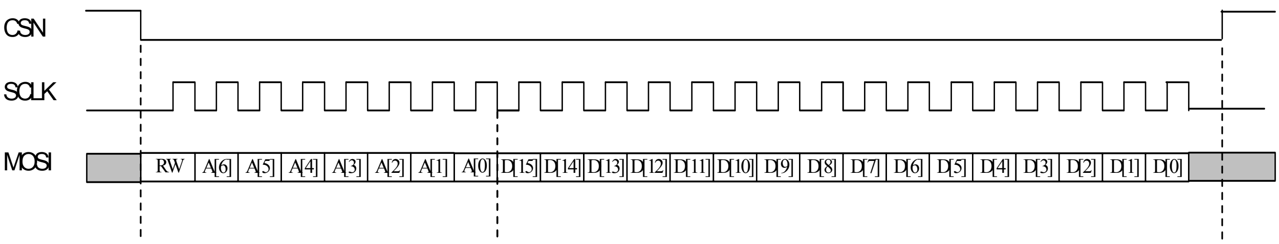
MISO is not tristated when SPI not selected (MISO = GND when SPI not selected)

The MOSI sequence should start with one R/W bit:

- R/W = 0 is a read procedure
- R/W = 1 is a write procedure

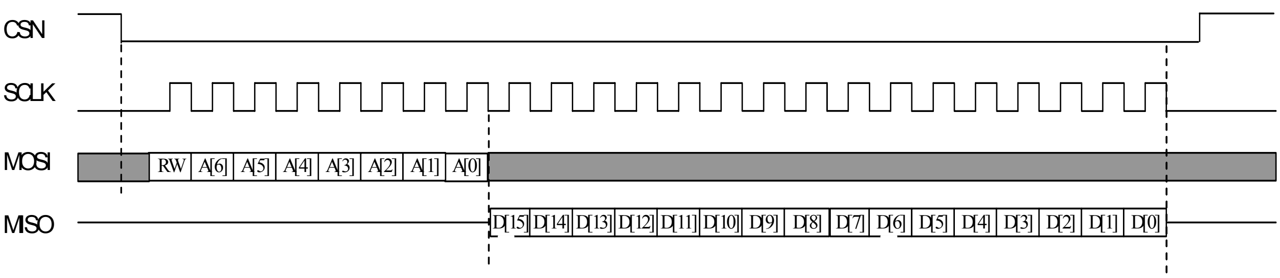
5.2.1. SPI Write/Read

Figure 15. SPI writing (16-bit register)



D[15] is the MSB of the 16 bit data word
D[0] is the LSB of the 16 bit data word
A[6] is the MSB of the 7 bit address word
A[0] is the LSB of the 7 bit address word
Bit RW = 1 for writing

Figure 16. SPI reading



Bit RW = 0 for reading

See section 3.6 for SPI timing characteristics (max clock frequency, …).
MOSI must be generated on the falling edge of SCLK

5.2.2. SPI Register mapping

SPI Registers that are common to the four ADC cores are implemented in the Master SPI described in Table 12 (There are two exceptions for x_CRC_STATUS and x_OFFSET_CAL with x=A, B, C or D). SPI Registers that are specific to one ADC core are described in Table 13.

Table 12. List of Master SPI registers

ADDRESS (hexa)	REGISTER	ACCESS	BIT	DEFAULT VALUE (hexa)	DESCRIPTION	REFER TO SECTION
00	Reserved	-	-	-	Must not be written	- -
01	CHANNEL_SEL	W	[2:0]	0x04	Selection of channel (A,B,C, D) By default all channels are selected	5.3
02	CHIP_ID	R	[15:0]	0x62C	Chip ID and chip version	5.17
05	CRC_OTP_STATUS	R	[7:0]		Notified when OTP values are available. CRC status for A, B, C and D channels	5.18
07	CLK_MODE_SEL	RW	[1:0]	0x001	Choice between aligned output clocks or staggered output clock. Choice between clock divided by 2 or not	5.9
15	CAL_SET_SEL	RW	[0]	0x000	Selection of 1 of the 2 sets of MASTER OTP written during manufacturing.	5.8
16	OTP_SPI_SEL	RW	[3:0]	0x000	Selection between MASTER OTP or SPI value	5.3
17	A_OFFSET_CAL	RW	[8:0]	0x100	Adjustment of channel A offset	5.8
18	B_OFFSET_CAL	RW	[8:0]	0x100	Adjustment of channel B offset	5.8
19	C_OFFSET_CAL	RW	[8:0]	0x100	Adjustment of channel C offset	5.8
1A	D_OFFSET_CAL	RW	[8:0]	0x100	Adjustment of channel D offset	5.8
1B	CM_IN	RW	[4:0]	0x010	Adjustment of analog input common mode	5.14
1C	R_IN	RW	[3:0]	0x008	Adjustment of analog input impedance	5.13
6B	A_OFFSET_CAL_R	R	[8:0]	0x100	Reading of channel A offset	5.8
6C	B_OFFSET_CAL_R	R	[8:0]	0x100	Reading of channel B offset	5.8
6D	C_OFFSET_CAL_R	R	[8:0]	0x100	Reading of channel C offset	5.8
6E	D_OFFSET_CAL_R	R	[8:0]	0x100	Reading of channel D offset	5.8
6F	CM_IN_R	R	[4:0]	0x010	Reading of analog input common mode	5.14
70	R_IN_R	R	[3:0]	0x008	Reading of analog input impedance	5.13

Table 13. List of CHANNEL SPI registers (CHANNEL A, B, C and D)

ADDRESS (hexa)	REGISTER	ACCESS	BIT	DEFAULT VALUE (hexa)	DESCRIPTION	REFER TO SECTION
00	Reserved	-	-	-	Must not be written	-
15	CAL_SET_SEL	RW	[0]	0x000	Selection of one of the 2 sets of CHANNEL OTP written during the manufacturing	5.8
16	OTP_SPI_SEL	RW	[9:6] [4]	0x000	Selection between CHANNEL OTP or SPI value	5.3
33	CAL1	RW	[6:0]	0x040	7 Calibration parameters (for each channel) To be modified for custom interleaving only	5.8
34	CAL2	RW	[6:0]	0x040		5.8
35	CAL3	RW	[6:0]	0x040		5.8
36	CAL4	RW	[6:0]	0x040		5.8
37	CAL5	RW	[6:0]	0x040		5.8
38	CAL6	RW	[6:0]	0x040		5.8
39	CAL7	RW	[6:0]	0x040		5.8
3A	GAIN_CAL	RW	[9:0]	0x200	Gain (for each channel) To be modified for custom interleaving only	5.8
3B	INT_GAIN_CAL	RW	[7:0]	0x080	Internal gain (for each channel) To be modified for custom interleaving only	5.8
3D	PHASE_ CAL	RW	[7:0]	0x080	Phase (for each channel) To be modified for custom interleaving only	5.8
4F	CAL1	R	[6:0]	0x040	Calibration (OTP or SPI) sending to ADC core	5.8
50	CAL2	R	[6:0]	0x040	Calibration (OTP or SPI) sending to ADC core	5.8
51	CAL3	R	[6:0]	0x040	Calibration (OTP or SPI) sending to ADC core	5.8
52	CAL4	R	[6:0]	0x040	Calibration (OTP or SPI) sending to ADC core	5.8
53	CAL5	R	[6:0]	0x040	Calibration (OTP or SPI) sending to ADC core	5.8
54	CAL6	R	[6:0]	0x040	Calibration (OTP or SPI) sending to ADC core	5.8
55	CAL7	R	[6:0]	0x040	Calibration (OTP or SPI) sending to ADC core	5.8
56	GAIN_ CAL_R	R	[9:0]	0x200	Calibration (OTP or SPI) sending to ADC core	5.8
57	INT_GAIN_CAL_R	R	[7:0]	0x080	Calibration (OTP or SPI) sending to ADC core	5.8
59	PHASE_ CAL_R	R	[7:0]	0x080	Calibration (OTP or SPI) sending to ADC core	5.8
5A	OTP_STATUS	R	[0]		Status signal for OTP. Notify when OTP values are available.	5.19
5C	STDBY	RW	[4:0]	0x000	Power down mode (for each channel)	5.11
5D	TEST_MODE	RW	[6:0]	0x000	Test Mode selection : • Flash mode • Ramp mode	5.15
5F	PRBS_CTRL	RW	[1:0]	0x000	Pseudo Random Bit Sequence control	5.16
66	RST_LENGTH	RW	[5:0]	0x008	Data_ready reset length	5.7.2.
69	FLASH_LENGTH	RW	[5:0]	0x018	Flash motif length	5.15
6A	FULL_SWING_EN	RW	[9:0]	0x000	Selection between nominal or reduced swing on Data output buffers (for power consumption reduction)	5.12

All registers are 16-bit width
R = read only register
W = write only register
RW = Read/Write register

5.3. Addressing Master SPI and Channel SPI

Table 14 below describes how to address Master SPI or Channel SPI.

Table 14. Master SPI - CHANNEL_SEL register description

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
													CHANNEL_SEL <2:0>		

Bit label	Value (binary)	Description	Default Setting (hexa)	Address for W (hexa)
CHANNEL_SEL <2:0>	000	Channel A selected	0004	01
	001	Channel B selected		
	010	Channel C selected		
	011	Channel D selected		
	100	ALL channels selected (default)		
	111	Master SPI selected		

CHANNEL_SELECTION	WRITE INSTRUCTION				
	Master	A	B	C	D
Channel A SELECTED	OK	OK			
Channel B SELECTED	OK		OK		
Channel C SELECTED	OK			OK	
Channel D SELECTED	OK				OK
ALL Channels SELECTED	OK	OK	OK	OK	OK
Master SPI SELECTED	OK				

Note: Master SPI is only accessible in writing (reading not possible)

Table 15. Example 1: OTP_SPI_SEL is a register of the channel A, B, C, D and the Master SPI. It is the same address for channel and Master SPI

		Register OTP_SPI_SEL				
Order of SPI instruction	SPI Instruction (in hexa)	SPI Master	Channel A	Channel B	Channel C	Channel D
	Initial state (default value)	OTP value	OTP value	OTP value	OTP value	OTP value
1	Write @CHANNEL_SEL 00 (A selected) Write @OTP_SPI_SEL 01D0	OTP value	SPI value	OTP value	OTP value	OTP value
2	Write @CHANNEL_SEL 01 (B selected) Write @OTP_SPI_SEL 01D0	OTP value	SPI value	SPI value	OTP value	OTP value
3	Write @CHANNEL_SEL 02 (C selected) Write @OTP_SPI_SEL 01D0	OTP value	SPI value	SPI value	SPI value	OTP value
4	Write @CHANNEL_SEL 03 (D selected) Write @OTP_SPI_SEL 01D0	OTP value	SPI value	SPI value	SPI value	SPI value
5	Write @CHANNEL_SEL 07 (Master SPI selected) Write @OTP_SPI_SEL 0007	SPI value	SPI value	SPI value	SPI value	SPI value
6	Write @CHANNEL_SEL 04 (All Channels selected) Write @OTP_SPI_SEL 0000	OTP value	OTP value	OTP value	OTP value	OTP value
7	Write @CHANNEL_SEL 04 (All Channels selected) Write @OTP_SPI_SEL 01D7	SPI value	SPI value	SPI value	SPI value	SPI value

Table 16. EXAMPLE 2: STDBY is a register of the channel A, B, C, D.

		Register STDBY				
Order of SPI instruction	SPI Instruction (in hexa)	SPI Master	Channel A	Channel B	Channel C	Channel D
1	Initial state (default value)	Not concerned	Power ON	Power ON	Power ON	Power ON
2	Write @CHANNEL_SEL 04 (All selected) Write @STDBY 0001	Not concerned	standby	standby	standby	standby
3	Write @CHANNEL_SEL 00 (A selected) Write @STDBY 0000	Not concerned	Power ON	standby	standby	standby
4	Write @CHANNEL_SEL 01 (B selected) Write @STDBY 0000	Not concerned	Power ON	Power ON	standby	standby
5	Write @CHANNEL_SEL 02 (C selected) Write @STDBY 0000	Not concerned	Power ON	Power ON	Power ON	standby
6	Write @CHANNEL_SEL 03 (D selected) Write @STDBY 0000	Not concerned	Power ON	Power ON	Power ON	Power ON
7	Write @CHANNEL_SEL 04 (all Channels selected) Write @STDBY 0001	Not concerned	standby	standby	standby	standby
8	Write @CHANNEL_SEL 04 (all Channels selected) Write @STDBY 0000	Not concerned	Power ON	Power ON	Power ON	Power ON

5.4. Selection between OTP and SPI registers

Some settings programmed during the manufacturing in OTP cells (One Time Programmable or fuses) can be modified by the user in applying its own settings via the SPI.
This selection is done thanks to the OTP_SPI_SEL register defined in the Master SPI (described in Table 17 below) and the OTP_SPI_SEL register defined in the Channel SPI (described in Table 18 below).

Table 17. Master SPI - OTP_SPI_SEL register description

Bit (15 down to 4)	Bit 3	Bit 2	Bit 1	Bit 0
	0	SEL _R_IN	SEL_CM_IN	SEL_OFFSET_CAL

Bit label	Value	Description	Default Setting (hexa)	Address for R/W (hexa)
SEL_OFFSET_CAL	0	x_OFFSET_CAL (with x=A, B, C and D) OTP values are selected	0	16
	1	x_OFFSET_CAL (with x=A, B, C and D) SPI registers are selected		
SEL_CM_IN	0	CM_IN OTP value is selected		
	1	CM_IN SPI register is selected		
SEL _R_IN	0	R_IN OTP value is selected		
	1	R_IN SPI register is selected		

By default, OTP values are selected
OTP_SPI_SEL is a common register with the Channel A,B,C,D and Master SPI. That means it is the same address for Channel and Master SPI.

Procedure example:
Below xxxx represents the value to be written by the user.

Changing R_IN calibration:
WRITE @ CHANNEL_SEL 0007 # Master SPI is selected
WRITE @OTP_SPI_SEL 0004 # Now, R_IN value comes from SPI register
WRITE @R_IN xxxx # The SPI R_IN value is taken into account
NB : The considered values for x_OFFSET_CAL (with x=A, B, C and D) and CM_IN are OTP values

Changing x_OFFSET_CAL calibration:
WRITE @ CHANNEL_SEL 0007 # Master SPI is selected
WRITE @OTP_SPI_SEL 0001 # Now, x_OFFSET_CAL (with x= A,B,C,D) values come from SPI register
WRITE @A_OFFSET_CAL xxxx # The SPI A_OFFSET_CAL value is taken into account
WRITE @B_OFFSET_CAL xxxx # The SPI B_OFFSET_CAL value is taken into account
WRITE @C_OFFSET_CAL xxxx # The SPI C_OFFSET_CAL value is taken into account
WRITE @D_OFFSET_CAL xxxx # The SPI D_OFFSET_CAL value is taken into account
NB : The considered values for R_IN and CM_IN are OTP values

Changing OFFSET_CAL and R_IN calibration:
WRITE @CHANNEL_SELT 0007 # Master SPI is selected
WRITE @OTP_SPI_SEL 0005 # Now, x_OFFSET_CAL (with x=A,B,C,D) and R_IN values come from SPI register
WRITE @A_OFFSET_CAL xxxx # The SPI A_OFFSET_CAL value is taken into account
WRITE @B_OFFSET_CAL xxxx # The SPI B_OFFSET_CAL value is taken into account
WRITE @C_OFFSET_CAL xxxx # The SPI C_OFFSET_CAL value is taken into account
WRITE @D_OFFSET_CAL xxxx # The SPI D_OFFSET_CAL value is taken into account
WRITE @R_IN xxxx # The SPI R_IN value is taken into account

NB: in order to avoid any confusion about channels selection, all procedures should begin with the instruction **WRITE @CHANNEL_SEL xxxx**

Table 18. Channel SPI - OTP_SPI_SEL register description

Bit[15:10]	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit[3:0]
	0	OTP_SPI_SEL_CAL	OTP_SPI_SEL_GAIN	OPT_SPI_SEL_INT_GAIN	0	OTP_SPI_SEL_PHASE	

Bit label	Value	Description	Default Setting (hexa)	Address for R/W (hexa)
OTP_SPI_SEL_PHASE	0	OTP Interleaving Phase calibration value is selected	0	16
	1	SPI Interleaving Phase calibration value is selected		
OTP_SPI_SEL_INT_GAIN	0	OTP Internal Gain value is selected		
	1	SPI Internal Gain value is selected		
OTP_SPI_SEL_GAIN	0	OTP Interleaving Gain Calibration value is selected		
	1	SPI Interleaving Gain Calibration value is selected		
OTP_SPI_SEL_CAL	0	OTP CAL1 to CAL7 calibration values are selected		
	1	SPI CAL1 to CAL7 calibration values are selected		

By default, OTP values are selected
OTP_SPI_SEL is a common register of the channel A,B,C,D and Master SPI. That means it is the same address for the Channel and Master SPI.

Procedure examples:
Below xxxx represents the value to be written by the user.

Changing PHASE_CAL calibrations:
WRITE @CHANNEL_SEL 0000 # Channel A selected
WRITE @OTP_SPI_SEL 0010 # Now, PHASE_CAL A value comes from SPI register
All other settings (x_OFFSET_CAL (with x=A, B, C &D), CM_IN, R_IN,
INT_GAIN_CAL, GAIN_CAL, CAL1 to CAL7 and
x_PHASE_CAL with x=B, C, & D) remains with OTP values
WRITE @PHASE_CAL xxxx # Only PHASE_CAL A SPI value is taken into account

```
WRITE @CHANNEL_SEL   0001          # Channel B selected
WRITE @OTP_SPI_SEL   0010          # Now, PHASE_CAL B value comes from SPI register
                                   # All other settings (x_OFFSET_CAL (with x=A, B, C &D), CM_IN, R_IN,
                                   # INT_GAIN_CAL, GAIN_CAL, CAL1 to CAL7 and
                                   # x_PHASE_CAL with x=C & D) remains with OTP values
WRITE @PHASE_CAL   xxxx            # Only PHASE_CAL A & B SPI values are taken into account

WRITE @CHANNEL_SEL   0002          # Channel C selected
WRITE @OTP_SPI_SEL   0010          # Now, PHASE_CAL C value comes from SPI register
                                   # All other settings (x_OFFSET_CAL (with x=A, B, C &D), CM_IN, R_IN,
                                   # INT_GAIN_CAL, GAIN_CAL, CAL1 to CAL7, x_PHASE_CAL with x=D)
                                   # remains with OTP values
WRITE @ PHASE_CAL   xxxx           # Only PHASE_CAL A, B & C SPI values are taken into account

WRITE @CHANNEL_SEL   0003          # Channel D selected
WRITE @OTP_SPI_SEL   0010          # Now, PHASE_CAL D value comes from SPI register
                                   # All other settings (x_OFFSET_CAL (with x=A, B, C &D), CM_IN, R_IN,
                                   # INT_GAIN_CAL, GAIN_CAL, CAL1 to CAL7) remains with OTP values
WRITE @CHANNEL_PHASE   xxxx        # Only PHASE_CAL A, B, C & D SPI values are taken into account
```

If all PHASE_CAL (A, B, C & D) have to switch from OTP to SPI, the following procedure is simpler and recommended:
Changing all PHASE_CAL calibrations:

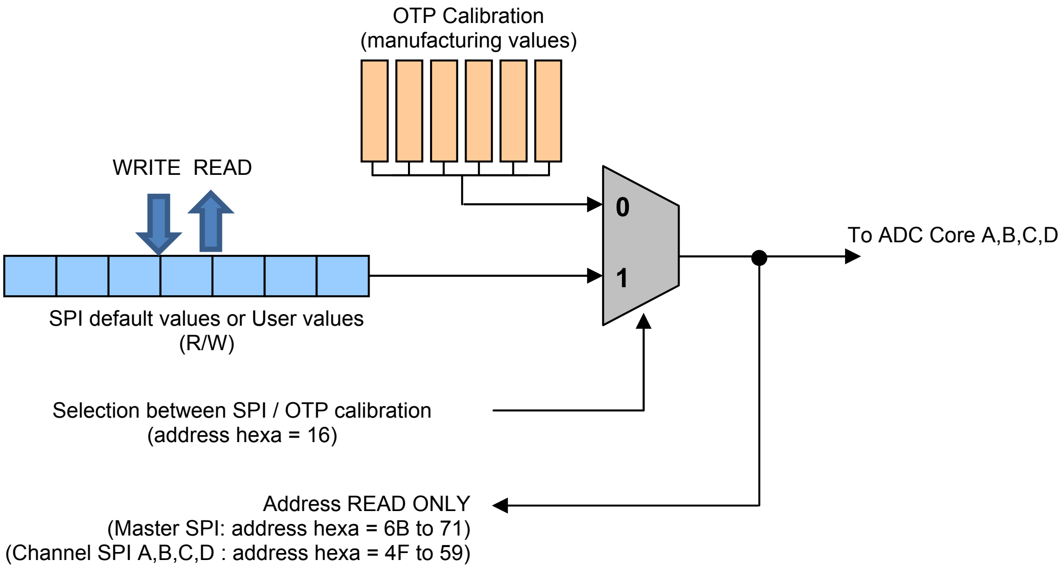
```
WRITE @CHANNEL_SEL   0004          # ALL Channel + SPI Master selected
WRITE @OTP_SPI_SEL   0010          # Now, PHASE_CAL values come from SPI register

WRITE @CHANNEL_SEL   0000          # Channel A selected
WRITE @ PHASE_CAL   xxxx           # The SPI value is taken into account

WRITE @CHANNEL_SEL   0001          # Channel B selected
WRITE @ PHASE_CAL   xxxx           # The SPI value is taken into account

WRITE @CHANNEL_SEL   0002          # Channel C selected
WRITE @PHASE_CAL   xxxx            # The SPI value is taken into account

WRITE @CHANNEL_SEL   0003          # Channel D selected
WRITE @PHASE_CAL   xxxx            # The SPI value is taken into account
```

Changing PHASE_CAL and R_IN calibration:
The procedure “Changing R_IN calibration” and “Changing PHASE_CAL calibration” can be launched separately.
This procedure (12 instead 15 SPI instructions) can also be launched:

```
WRITE @CHANNEL_SEL   0004          # ALL Channel + SPI Master selected
WRITE @OTP_SPI_SEL   0014          # Now, PHASE_CAL and R_IN values come from SPI register

WRITE @CHANNEL_SEL   0007          # SPI Master selected
WRITE @R_IN   xxxx                 # The SPI value is taken into account

WRITE @CHANNEL_SEL   0000          # Channel A selected
WRITE @PHASE_CAL   xxxx            # The SPI value is taken into account

WRITE @CHANNEL_SEL   0001          # Channel B selected
WRITE @PHASE_CAL   xxxx            # The SPI value is taken into account

WRITE @CHANNEL_SEL   0002          # Channel C selected
WRITE @PHASE_CAL   xxxx            # The SPI value is taken into account

WRITE @CHANNEL_SEL   0003          # Channel D selected
WRITE @PHASE_CAL   xxxx            # The SPI value is taken into account
```

NB: in order to avoid any confusion about channels selection, all procedures should begin with the instruction **WRITE @CHANNEL_SEL xxxx**

Figure 17. Selection between OTP and SPI registers



Note that reading at the READ ONLY address enables to verify the value really taken into consideration. Reading at the Read/Write address send the SPI default values or User values even if OTP calibration values are selected via OTP_SPI_SEL register.

5.5. Functionalities summary

Table 19 provides a summary of all functionalities and indicates if it is configured by OTP (One Time Programmable) or by SPI registers.

Table 19. Functionalities summary

Functionalities / mode	Default mode	Control	SPI registers	Comment
ADC synchronization with programmable reset length	-	SPI	RST_LENGTH	A SYNC signal is mandatory to properly initialize and synchronize the 4 ADC channels. When reset output data ready are going to zero during a RESET_LENGTH time which is set by the user via the SPI.
Core ADCs calibration	OTP during manufacturing	OTP	-	INL calibration of 4 ADC channels. Cannot be modified by user.
ADCs interleaving calibration	OTP during manufacturing	OTP / SPI	x_OFFSET_CAL GAIN_CAL INT_GAIN_CAL PHASE_CAL	x = A, B, C or D Manufacturing settings can be modified by user via the SPI
Temperature Range selection	Ambient & Hot temperature	SPI selection	CAL_SET_SEL	2 sets of ADCs interleaving calibration are programmed in OTP during manufacturing and can be selected by SPI ▪ 1 set for cold temperature ▪ 1 set for ambient and hot temperature
Junction temperature monitoring	-	-	-	External current source needed See diode characteristics in section 5.22
Staggered or Simultaneous mode	Staggered	SPI selection	CLK_CTRL	• In staggered mode 4 ADC channels are interleaved. Output data of each channel is delayed by 1/4 of external clock period • In Simultaneous mode, 4 ADC channels are not interleaved and convert the same analog input signal. Output data of each channel are outputted simultaneously.
Clock control CLOCK_DIV2	No clock division	SPI selection	CLK_MODE_SEL	2 modes available: ▪ CLOCK_DIV2 = 0: input clock is not divided ▪ CLOCK_DIV2 = 1: input clock is not divided by 2
Standby mode	No standby	SPI selection	STDBY CHANNEL_SEL	Power down mode. Data Ready outputs are stopped. Each channel is controlled individually
Swing Adjust	Reduced swing	SPI selection	FULL_SWING_EN	Selection between 2 configurations for all output data and data ready outputs ▪ Standard LVDS (nominal swing) ▪ Reduced swing Reducing the swing enables to save around 180 mW
Analog input impedance calibration	OTP during manufacturing	OTP / SPI	R_IN	Manufacturing settings can be modified by user via the SPI
Analog input common mode calibration	OTP during manufacturing	OTP / SPI	CM_IN	Manufacturing settings can be modified by user via the SPI
Test Modes	disabled	SPI selection	TEST_MODE FLASH_LENGTH	Ramp mode. Flash mode. Sequence length is programmable via SPI
PRBS	Signal only	SPI selection	PRBS_CTRL	3 possible configurations for Pseudo Random Bit Sequence: ▪ PRBS only ▪ SIGNAL (output data from input signal) + PRBS ▪ SIGNAL only (default mode)
Chip identification	-	-	CHIP_ID	Identification of chip ID
CRC status	-	SPI	CRC_OTP_STATUS	Verification of OTP integrity (Cyclic Redundancy Check)
Parity Bit	-	-		1 dedicated output buffer by channel
In Range Bit	-	-		1 dedicated output buffer by channel
OTP status	-	-	CRC_OTP_STATUS OTP_STATUS	Verification of OTP status

5.6. Reset and start up procedure

RSTN is a global reset for the SPI and OTP (One Time Programmable registers or fuses)
It is active Low. It is mandatory to put RSTN at low level during a minimum of 10 µs.
It will set ALL configuration registers to their default values.

1) Reset for digital and OTP (mandatory)
   ➔ Low state pulse on RSTN (10 µs minimum)

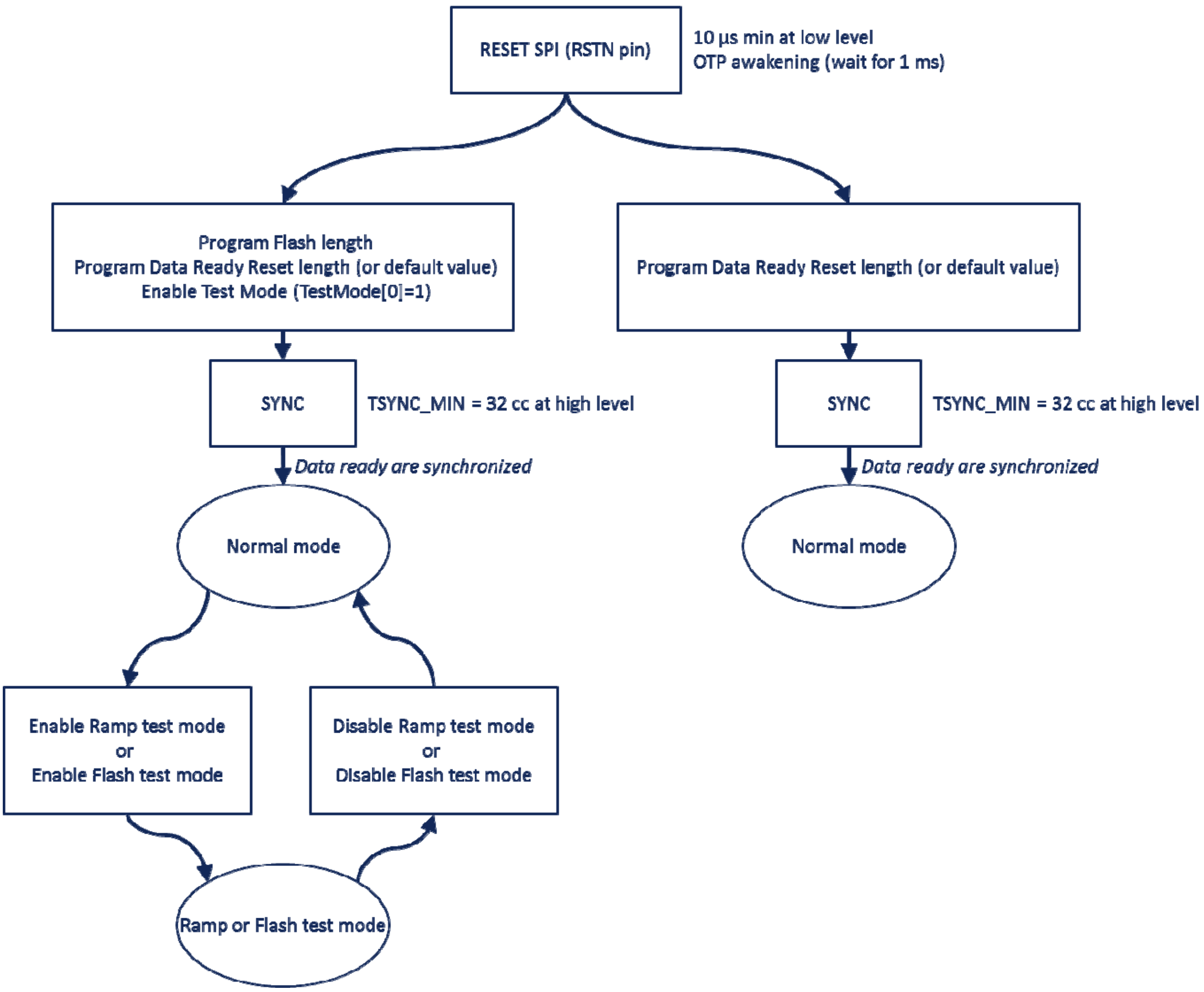
2) Wait for OTP awakening (wait for 1 ms)

3) Program Flash length and reset length (optional)

4) Enable Test Modes (Optional) if Ramp or Flash pattern is used

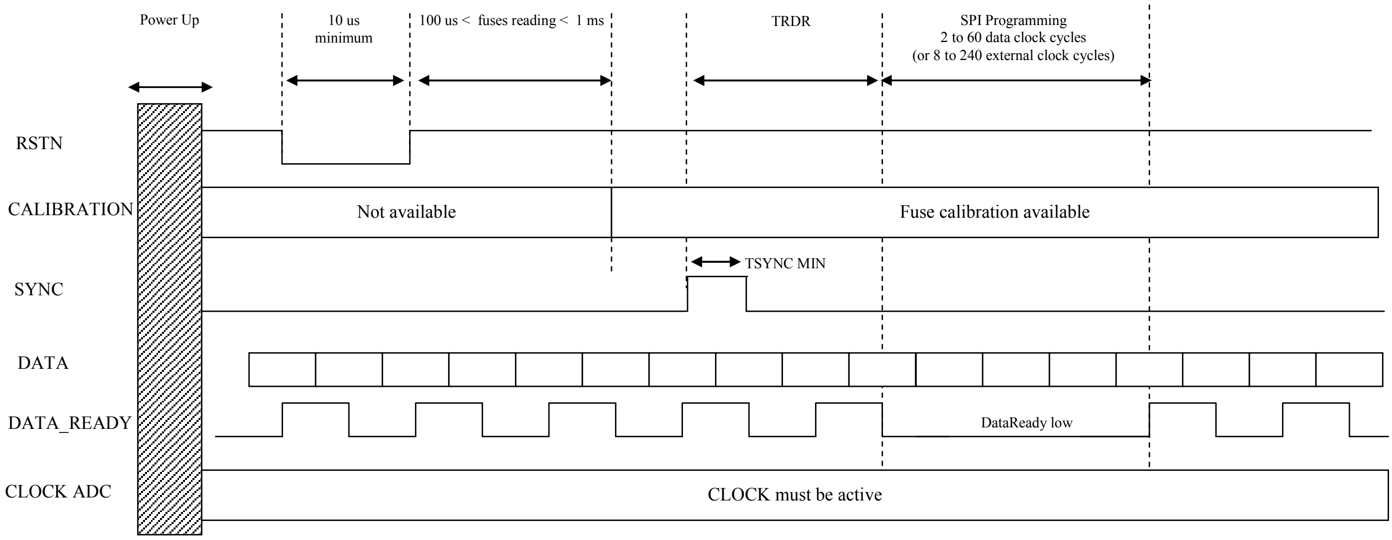
5) Synchronisation of Data-Ready ➔ High pulse on SYNC (See TSYNC_MIN length on Table 7)

Figure 18. Software reset and start up procedure diagram



Note 1: Above procedure is detailed in section 7.7.
Note 2: When in Flash test mode, if the Flash length is changed, a SYNC must follow.

Figure 19. Software reset and start up procedure

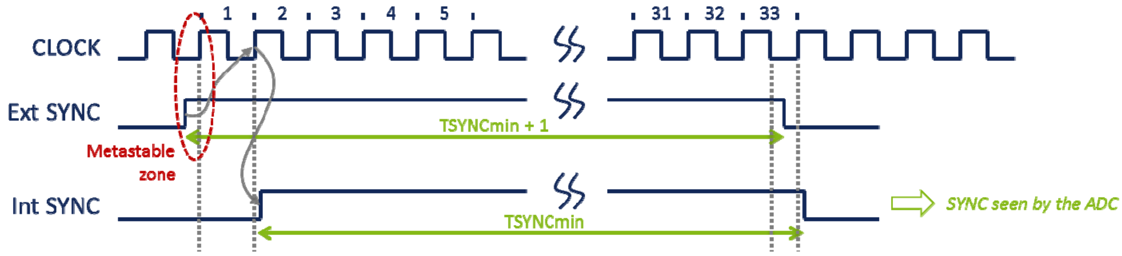


5.7. ADC Synchronization (SYNC) with programmable reset duration

5.7.1. ADC Synchronization (SYNC)

Synchronization is done through the SYNC, SYNCN signal which has LVDS electrical characteristics. SYNC is active high and should last at least the “TSYNC_MIN” time defined in Table 7.
In order to have a deterministic starting order of the four output data and data ready signals, a synchronous SYNC, SYNCN signal is mandatory and must comply with SYNC valid timings (T1, T2) defined in Table 7 (for further details, please see section 3.6.3.). It becomes effective on the rising edge of SYNC, SYNCN. The four data ready are reset after a time equal to TRDR defined in Table 7 (see details on Figure 21 in section 5.7.3.). In this case the same deterministic behavior is obtained between successive synchronization sequences. Synchronous SYNC, SYNCN signal is to be used in applications where multiple ADCs have to be synchronized and in applications where deterministic starting of the ADC is needed.
During the reset phase the four data ready are stopped at low level during a period that can be adjusted through SPI (see section 5.7.2. for more details).
However, an asynchronous SYNC signal (relative to the external clock) can be used in applications that do not require deterministic starting behavior of the ADC. In this case, the output data order is the same between successive synchronization sequences. However the starting and the latency is variable. An asynchronous SYNC signal must last at least TSYNCmin + 1 clock cycles; otherwise it may not be seen by the ADC due to metastability zone for example (see Figure 20).

Figure 20. Example of an asynchronous SYNC signal rising in a metastable zone



5.7.2. Data Ready reset length programming

The programming of Data Ready Reset length is done in the Channel SPI.
The register RESET_LENGTH is described below:

Table 20. Channel SPI - RESET_LENGTH register description

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
										RESET_LENGTH <5:0>					

Bit label	Description	Default Setting (hexa)	Address for R/W (hexa)
RESET_LENGTH <5:0>	Programming of the reset length. User can programme 2 to 63 internal clock cycles	0008	66

Note: there is one internal clock cycle uncertainty on the reset length. See Figure 21 and Table 21 below.

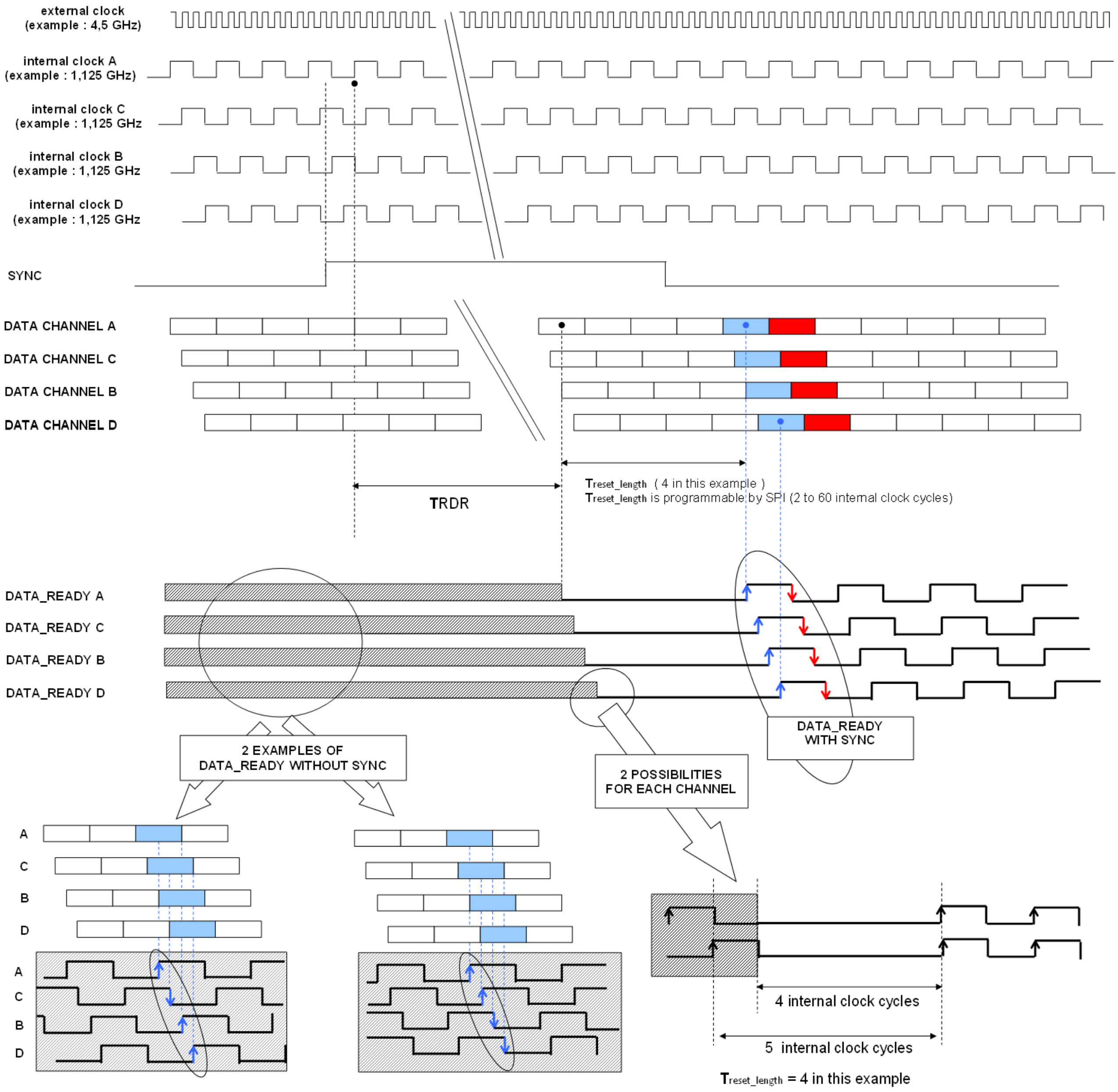
Procedure for reset length programming:
WRITE @01 0004 # ALL channels selected
WRITE @66 xxxx # Data Ready reset length programming (2 to 63 output data period)
For example with an external clock of 5.4 GHz, data output period is equal to 1.35 GHz clock period. Programming 8 means Data Ready will stay to '0' during 8 internal clock period.

Table 21. Reset length according to RESET_LENGTH register

RESET_LENGTH value (hexa)	Reset length (external clock cycles)
3F	252
08	32
2	8
1	Not to be used
0	0 (no reset)
Excursion	244
Step	4

5.7.3. SYNC timing diagram

Figure 21. SYNC Timing



5.8. ADC calibration

Refer to Application Note AN1190 for more information about ADC calibrations.

5.8.1. Core ADCs calibrations

Each ADC core has its INL calibrated during the manufacturing. The user does not have to modify OTP calibrations dedicated to INL of ADC cores.

5.8.2. Core interleaving calibrations

Interleaving calibrations are done during the manufacturing and two sets of OTP calibration are available: one set is recommended for cold temperature (optimum near Tj diode=50°C) and another set of OTP calibration is recommended for ambient and hot temperature (optimum near Tj diode=90°C). The selection of these two sets of calibrations is explained in the paragraph below.

5.8.3. Selection of one of the 2 sets of calibration

The selection of a set of OTP calibration is done in both Channel and Master SPI with CAL_SET_SEL register described below:

Table 22. Channel & Master SPI - CAL_SET_SEL register description

Bit 15	Bit 14	Bit 13	Bit 15	Bit 14	Bit 13	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
															CAL_SET_SEL

Bit label	Value	Description	Default Setting (hexa)	Address for R/W (hexa)
CAL_SET_SEL	0	OTP calibration for ambient and hot temperature selected	0	15
	1	OTP calibration for cold temperature selected		

CAL_SET_SEL is a common register with the Channel A,B,C,D and Master SPI. That means it is the same address for Channel and Master SPI.

Procedure for selecting one set of CAL_SET_SEL calibration:

```
WRITE  @01  0004    # ALL channels selected
WRITE  @15  0001    # OTP calibration cold temperature selected for ALL channels
```

or

```
WRITE  @01  0004    # ALL channels selected
WRITE  @15  0000    # OTP calibration hot temperature selected for ALL channels
```

5.8.4. Interpolation of calibrations (for temperature)

When the device is functioning at a junction temperature that is not close to Tj diode=50°C (cold calibration) or Tj diode=90°C (ambient and hot temperature), it is possible to interpolate linearly the OTP calibration settings to optimize dynamic performances.
The principle consists in reading the OTP value dedicated to the calibration at cold, then reading the OTP value dedicated to the calibration at ambient and hot temperature and then interpolate the value for the temperature of interest (Tj) and write it via the SPI.

Interpolation formula is given below:

Equation 1 - Interpolation formula

$$\text{Register}(V_{diode}) = (R_0 - R_1)/(787-830) * (V_{diode} - 830) + R_1$$

With :
Vdiode = Value of the diode of temperature for the considered temperature in mV.
R_1 = Register when CAL_SET_SEL=1 is selected and R_0=Register when CAL_SET_SEL=0.
Register = each register listed in Table 23.

Registers to be interpolated over temperature are listed in Table 23 and described in section 5.8.4.1 to 5.8.4.5.

Table 23. List of registers to be interpolated over temperature for optimum calibrations.

Registers in Master SPI	**Registers in Channel SPI**
A_OFFSET_CAL	CAL1
B_OFFSET_CAL	CAL2
C_OFFSET_CAL	CAL3
D_OFFSET_CAL	CAL4
	CAL5
	CAL6
	CAL7
	GAIN_CAL
	INT_GAIN_CAL
	PHASE_ CAL

5.8.4.1. Description of x_OFFSET_CAL registers (with x=A, B, C or D)

Table 24. Master SPI – A_OFFSET_CAL register description

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
							A_OFFSET_CAL <8:0>								

Bit label	Description	Default Setting (hexa)	Address for R/W (hexa)	Address for read only (hexa)
A_OFFSET_CAL <8:0>	Channel A offset adjustment	0100	17	6B

Table 25. Master SPI – B_OFFSET_CAL register description

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
							B_OFFSET_CAL <8:0>								

Bit label	Description	Default Setting (hexa)	Address for R/W (hexa)	Address for read only (hexa)
B_OFFSET_CAL <8:0>	Channel B offset adjustment	0100	18	6C

Table 26. Master SPI - C_OFFSET_CAL register description

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
							C_OFFSET_CAL <8:0>								

Bit label	Description	Default Setting (hexa)	Address for R/W (hexa)	Address for read only (hexa)
C_OFFSET_CAL <8:0>	Channel C offset adjustment	0100	19	6D

Table 27. Master SPI - D_OFFSET_CAL register description

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
							D_OFFSET_CAL <8:0>								

Bit label	Description	Default Setting (hexa)	Address for R/W (hexa)	Address for read only (hexa)
D_OFFSET_CAL <8:0>	Channel D offset adjustment	0100	1A	6E

Table 28. ADC Core offset adjustment according to x_OFFSET_CAL register (x=A, B, C or D)

OFFSET_CHANNEL_x value (hexa)	ADC Core x typical offset (LSB)
1FF	2016
100	2044
000	2073
Excursion	57
Step	0.11

5.8.4.2. **Description of CAL1 to CAL7 registers**

Table 29. Channel SPI - CALx registers description

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
									CALx <6:0>						

Bit label	Description	Default Setting	Address for R/W (hexa)	Address for read only (hexa)
CAL1 <6:0>	Channel CAL1	0040	33	4F
CAL2 <6:0>	Channel CAL2	0040	34	50
CAL3 <6:0>	Channel CAL3	0040	35	51
CAL4 <6:0>	Channel CAL4	0040	36	52
CAL5 <6:0>	Channel CAL5	0040	37	53
CAL6 <6:0>	Channel CAL6	0040	38	54
CAL7 <6:0>	Channel CAL7	0040	39	55

Procedure for CAL1 to 7 calibrations:

```
WRITE @CHANNEL_SEL   0007              # Master SPI selected
READ @OTP_SPI_SEL                      # save bit(3:0)

WRITE @CHANNEL_SEL   0000              # Channel A selected
WRITE @CAL1                xxxx
WRITE @CAL2                xxxx
…
WRITE @CAL7                xxxx
WRITE @OTP_SPI_SEL   bit(8)  1         # CAL1 to CAL7 switching from OTP value to SPI value


WRITE @CHANNEL_SEL   0001              # Channel B selected
WRITE @CAL1                xxxx
WRITE @CAL2                xxxx
…
```

```
WRITE @CAL7                xxxx
WRITE @OTP_SPI_SEL   bit(8)  1              # CAL1 to CAL7 switching from OTP value to SPI value

WRITE @CHANNEL_SEL  0002                    # Channel C selected
WRITE @CAL1                xxxx
WRITE @CAL2                xxxx
…
WRITE @CAL7                xxxx
WRITE @OTP_SPI_SEL   bit(8)  1              # CAL1 to CAL7 switching from OTP value to SPI value

WRITE @CHANNEL_SEL  0003                    # Channel D selected
WRITE @CAL1                xxxx
WRITE @CAL2                xxxx
…
WRITE @CAL7                xxxx
WRITE @OTP_SPI_SEL   bit(8)  1              # CAL1 to CAL7 switching from OTP value to SPI value
```

5.8.4.3. **Description of GAIN_CAL registers**

Table 30. Channel SPI – GAIN_CAL register description

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
						GAIN_CAL <9:0>									

Bit label	Description	Default Setting (hexa)	Address for R/W (hexa)	Address for read only (hexa)
GAIN_CAL <9:0>	ADC Core Gain for channel A, B, C or D	200	3A	56

Table 31. ADC Core Gain adjustment according to GAIN_CAL register

GAIN_CAL value (hexa)	ADC Core typical gain (dB)
3FF	-1.71
200	-1.22
000	-0.70
Excursion	1.02
Step	993 E-09

5.8.4.4. **Description of INT_GAIN_CAL registers**

Table 32. SPI Channel - INT_GAIN_CAL register description

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
								INT_GAIN_CAL <7:0>							

Bit label	Description	Default Setting (hexa)	Address for R/W (hexa)	Address for read only (hexa)
INT_GAIN_CAL <7:0>	Internal Gain for channel A, B, C or D	0080	3B	57

5.8.4.5. **Description of PHASE_CAL registers**

Table 33. SPI_Channel - PHASE_CAL register description

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
								PHASE_CAL <7:0>							

Bit label	Description	Default Setting (hexa)	Address for R/W (hexa)	Address for read only (hexa)
PHASE_CAL <7:0>	Phase for channel A, B, C or D	0080	3D	59

Table 34. ADC Core Phase adjustment according to PHASE_CAL register

PHASE_CAL value (hexa)	ADC Core typical Phase (ps)
FF	3.05
80	0
00	-3.05
Excursion	6.1
Step	0.024

5.8.4.6. **Procedure for interpolation of calibration versus temperature**

Procedure for interpolation of calibration versus temperature:

```
WRITE @CHANNEL_SEL   0007                      # Master SPI selected

WRITE @CAL_SET_SEL          0000               # Temperature 0 selected (ambient & hot temperature)
READ  @A_OFFSET_CAL_R (read only register)     # READ  OTP calibration OFFSET temperature 0 for channel  A
READ  @B_OFFSET_CAL_R (read only register)     # READ  OTP calibration OFFSET temperature 0 for channel  B
READ  @C_OFFSET_CAL_R (read only register)     # READ  OTP calibration OFFSET temperature 0 for channel  C
READ  @D_OFFSET_CAL_R (read only register)     # READ  OTP calibration OFFSET temperature 0 for channel  D

WRITE @CAL_SET_SEL          0001               # Temperature 1 selected (cold temperature)
READ  @A_OFFSET_CAL_R (read only register)     # READ  OTP calibration OFFSET temperature 1 for channel  A
READ  @B_OFFSET_CAL_R (read only register)     # READ  OTP calibration OFFSET temperature 1 for channel  B
READ  @C_OFFSET_CAL_R (read only register)     # READ  OTP calibration OFFSET temperature 1 for channel  C
READ  @D_OFFSET_CAL_R (read only register)     # READ  OTP calibration OFFSET temperature 1 for channel  D

# All OFFSET calibrations were read
# Do calibration interpolation on each x_OFFSET_CAL registers in using the formula given in Equation 1

WRITE  @A_OFFSET_CAL_A  xxxx (RW register)
WRITE  @B_OFFSET_CAL_B  xxxx (RW register)
WRITE  @C_OFFSET_CAL_C  xxxx (RW register)
WRITE  @D_OFFSET_CAL_D  xxxx (RW register)

WRITE @OTP_SPI_SEL 0001                # Only x_OFFSET_CAL with x=A, B, C & D switch from OTP to SPI value


WRITE @CHANNEL_SEL   0004              # ALL Channels selected
WRITE @CAL_SET_SEL    0000             # Temperature 0 selected (ambient & hot temperature)

WRITE @CHANNEL_SEL   0000              # channel A selected
READ @CAL1                             # READ channel A calibration CAL1 temperature 0
READ @CAL2
READ @CAL3
READ @CAL4
READ @CAL5
READ @CAL6
READ @CAL7

WRITE @CHANNEL_SEL   0001              # channel B selected
READ @CAL1
READ @CAL2
```

```
READ @CAL3
READ @CAL4
READ @CAL5
READ @CAL6
READ @CAL7

WRITE @CHANNEL_SEL   0002                # channel C selected
READ @CAL1
READ @CAL2
READ @CAL3
READ @CAL4
READ @CAL5
READ @CAL6
READ @CAL7

WRITE @CHANNEL_SEL   0003                # channel D selected
READ @CAL1
READ @CAL2
READ @CAL3
READ @CAL4
READ @CAL5
READ @CAL6
READ @CAL7

WRITE @CHANNEL_SEL   0004                # ALL Channels selected
WRITE @CAL_SET_SEL    0001               # Temperature 1 selected (cold temperature)

WRITE @CHANNEL_SEL   0000                # channel A selected
READ @CAL1                               # READ channel A calibration CAL1 temperature 1
READ @CAL2
READ @CAL3
READ @CAL4
READ @CAL5
READ @CAL6
READ @CAL7

WRITE @CHANNEL_SEL   0001                # channel B selected
READ @CAL1
READ @CAL2
READ @CAL3
READ @CAL4
READ @CAL5
READ @CAL6
READ @CAL7

WRITE @CHANNEL_SEL   0002                # channel C selected
READ @CAL1
READ @CAL2
READ @CAL3
READ @CAL4
READ @CAL5
READ @CAL6
READ @CAL7

WRITE @CHANNEL_SEL   0003                # channel D selected
READ @CAL1
READ @CAL2
READ @CAL3
READ @CAL4
READ @CAL5
READ @CAL6
READ @CAL7

# All calibrations were read

# Do calibration interpolation on each CALx registers in using the formula given in Equation 1

WRITE @CHANNEL_SEL   0000                # channel A selected
WRITE @CAL1  xxxx                        # Write channel A  calibration CAL1
WRITE @CAL2  xxxx
WRITE @CAL3  xxxx
WRITE @CAL4  xxxx
WRITE @CAL5  xxxx
WRITE @CAL6  xxxx
WRITE @CAL7  xxxx
```

```
WRITE @CHANNEL_SEL   0001                # channel B selected
WRITE @CAL1  xxxx
WRITE @CAL2  xxxx
WRITE @CAL3  xxxx
WRITE @CAL4  xxxx
WRITE @CAL5  xxxx
WRITE @CAL6  xxxx
WRITE @CAL7  xxxx

WRITE @CHANNEL_SEL   0002                # channel C selected
WRITE @CAL1  xxxx
WRITE @CAL2  xxxx
WRITE @CAL3  xxxx
WRITE @CAL4  xxxx
WRITE @CAL5  xxxx
WRITE @CAL6  xxxx
WRITE @CAL7  xxxx

WRITE @CHANNEL_SEL   0003                # channel D selected
WRITE @CAL1  xxxx
WRITE @CAL2  xxxx
WRITE @CAL3  xxxx
WRITE @CAL4  xxxx
WRITE @CAL5  xxxx
WRITE @CAL6  xxxx
WRITE @CAL7  xxxx

WRITE @CHANNEL_SEL   0004                # ALL Channels selected
WRITE @OTP_SPI_SEL    0101               # x_OFFSET_CHANNEL (with x=A, B, C & D) remain with SPI value
                                         # CAL1 to CAL7 for channels A, B, C & D switch from OTP to SPI value
```

Proceed as per CALx with GAIN_CAL,

```
# Read temperature 0 and temperature 1
# Do calibration interpolation on each GAIN_CAL registers in using the formula given in Equation 1
# Write interpolated values
WRITE @CHANNEL_SEL   0004                # ALL Channels selected
WRITE @OTP_SPI_SEL    0181               # x_OFFSET_CHANNEL (with =A, B, C & D) remain with SPI value
                                         # CAL1 to CAL7 for channels A, B, C & D remain with SPI value
                                         # GAIN_CAL for channels A, B, C, D switch from OTP to SPI value
```

Proceed as per CALx with INT_GAIN_CAL,

```
# Read temperature 0 and temperature 1
# Do calibration interpolation on each INT_GAIN_CAL registers in using the formula given in Equation 1
# Write interpolated values
WRITE @CHANNEL_SEL   0004                # ALL Channels selected
WRITE @OTP_SPI_SEL    01C1               # x_OFFSET_CHANNEL (with x=A, B, C & D) remain with SPI value
                                         # CAL1 to CAL7 for channels A, B, C & D remain with SPI value
                                         # GAIN_CAL for channels A, B, C, D remain with SPI value
                                         # INT_GAIN_CAL for channels A, B, C, D switch from OTP to SPI value
```

Proceed as per CALx with PHASE_CAL,

```
# Read temperature 0 and temperature 1
# Do calibration interpolation on each GAIN_CAL registers in using the formula given in Equation 1
# Write interpolated values
WRITE @CHANNEL_SEL   0004                # ALL Channels selected
WRITE @OTP_SPI_SEL 01D1                  # x_OFFSET_CAL (with x=A, B, C & D) remain with SPI value
                                         # CAL1 to CAL7 for channels A, B, C & D remain with SPI value
                                         # GAIN_CAL for channels A, B, C, D remain with SPI value
                                         # INT_GAIN_CAL for channels A, B, C, D remain with SPI value
                                         # PHASE_CAL for channels A, B, C, D switch from OTP to SPI value
```

5.8.5. User's own interleaving calibration

It is possible for the user to write its own adjustment settings (Offset, Gain, Phase) in order to improve the dynamic performance of the ADC in its own using conditions (clock frequency, analogue input frequencies …). In this case, it is recommended to first do an interpolation of calibration registers at the considered temperature of the system (refer to Section 5.8.4.), and then adjust Offset, Gain and Phase registers.

5.9. Staggered or simultaneous mode

It is possible to select one of the two modes described below in using the register CLK_MODE_SEL defined in Table 35 in the Master SPI.

Table 35. Master SPI - CLK_MODE_SEL register description

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
														CLOCK_ DIV2	CLOCK_ INTERLEAVING

Bit label	Value	Description	Default Setting (hexa)	Address for R/W (hexa)
CLOCK_INTERLEAVING	0	The 4 clocks channel are aligned/simultaneous	0001	07
	1	The 4 clocks channel are staggered ¼ phase shift for the 4 clocks (default value)		
CLOCK_DIV2	0	No internal division of the frequency of input clock signal (default value)		
	1	Internal division (factor 2) of the frequency of input clock signal		

5.9.1. Staggered mode

This is the default mode where the output cores are shifted by ¼ of the external clock period. The ADC can be seen as an ADC with a DEMUX 1:4.
There are 3 possibilities for the staggered mode (ADC cores interleaved):

- 4 ADC cores powered ON. See timing diagram on Figure 5.
- ADC cores A & B powered ON (C & D powered OFF)
- ADC cores C & D powered ON (A & B powered OFF)

When only 2 ADC cores are interleaved each clock channel are shifted by ½ of the external clock period

5.9.1. Simultaneous mode

In this mode each ADC core sample the same analog input signal and output the data simultaneously at the same time. This mode can be used for averaging.
See timing diagram on Figure 6.
In this mode, each ADC Core can be powered OFF as wished by the user (1 core ON, 2 cores ON, 3 cores ON or 4 cores ON)

5.10. CLOCK_DIV2: internal division of the clock frequency

It is possible (for debug purpose) to divide by two the clock frequency applied to the ADC. The clock division is done internally in addressing the CLK_MODE_SEL register of Master SPI described in Table 35 above.
By default there is no division by two of the input clock frequency.

5.11. Stand-by mode

It is possible to power down each core individually in addressing the STDBY register defined in the Channel SPI.

Table 36. CHANNEL SPI - STANDBY register description

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
											0	0	0	0	STDBY

Bit label	Value	Description	Default Setting (hexa)	Address for R/W (hexa)
STDBY	0	ADC Core(s) powered ON (no stand-by)	0	5C
	1	ADC Core(s) powered OFF (stand-by mode)		

Staggered mode is possible in the only case where 2 or 4 ADC cores are powered ON. See section 5.9.1. Simultaneous mode is possible with 1, 2, 3 or 4 ADC cores powered ON. When only one or two cores are powered ON, they can be selected indiscriminately (for instance Core B and Core D can be powered ON while others are OFF).

See section 5.3 for ADC core channel selection.

Procedure for ALL channels in STDBY mode:
```
WRITE  @01   0004           # ALL channels selected
WRITE  @5C  0001            # ALL channels are powered OFF (standby)
```

Procedure for channel A and B in STDBY mode
```
WRITE  @01   0000           # channel A selected
WRITE  @5C  0001            # channel A in standby mode
WRITE  @01   0001           # channel B  selected
WRITE  @5C  0001            # channel B standby mode (A remains in standby mode)
```

Procedure for channel B,C,D in STDBY mode
```
WRITE  @01   0001           # channel B  selected
WRITE  @5C  0001            # channel B in standby mode
WRITE  @01  0002            # channel C  selected
WRITE  @5C  0001            # channel C in standby mode
WRITE  @01  0003            # channel D  selected
WRITE  @5C  0001            # channel D in standby mode ( B & C remains in standby mode)
```

5.12. Swing Adjust

It is possible to select 2 types of swing for LVDS output data (including Data Ready outputs, Parity Bits and In Range bits):

- Standard LVDS output swing
- Reduced swing (leading to around 180mW power saving).

Reduced swing is the default mode, and a standard LVDS swing can be selected in addressing FULL_SWING_EN register in the Master SPI.

Table 37. Master SPI – FULL_SWING_EN register description

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
						FULL_SWING_EN	0								

Bit label	Value	Description	Default Setting (hexa)	Address for R/W (hexa)
FULL_SWING_EN	0	Reduced swing (for power saving)	0	6A
	1	Standard LVDS swing		

5.13. Analog input impedance calibration

It is possible to modify the analog input impedance calibrated during manufacturing. The modification is done via the register R_IN defined in the Master SPI.
To modify the R_IN value (from OTP), it is mandatory to modify register OTP_SPI_SEL defined in the Master SPI: bit SEL_R_IN has to be set to 1 level.

Table 38. Master SPI - OTP_SPI_SEL register description

Bit (15 down to 4)	Bit 3	Bit 2	Bit 1	Bit 0
	0	SEL _R_IN	SEL_CM_IN	SEL_OFFSET_CAL

Bit label	Value	Description	Default Setting (hexa)	Address for R/W (hexa)
SEL_OFFSET_CAL	0	OFFSET_CAL OTP values are selected	0	16
	1	OFFSET_CAL SPI registers are selected		
SEL_CM_IN	0	CM_IN OTP value is selected		
	1	CM_IN SPI register is selected		
SEL _R_IN	0	R_IN OTP value is selected		
	1	R_IN SPI register is selected		

Table 39. Master SPI - R_IN register description

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
												R_IN <3:0>			

Bit label	Description	SPI Default Setting (hexa)	Address for R/W (hexa)	Address for read only (hexa)
R_IN <3:0>	Analog input resistor value	0008	1C	70

Table 40. Analog input impedance (R_{IN}) value according to R_IN register

R_IN value (hexa)	R_{IN} typ value (Ω)
F	90
8	100
0	118
Excursion	28
Step	1.75

Procedure to have only R_IN value from SPI while all other settings from OTP:
WRITE @ CHANNEL_SEL 0007 # Master SPI is selected
WRITE @OTP_SPI_SEL 0004 # Now, R_IN value comes from SPI register
WRITE @R_IN xxxx # The SPI R_IN value is taken into account
Note: all other Master SPI settings come from OTP value (independently from previous configuration)
To conserve the previous configuration and change only R_IN, all bits of register OTP_SPI_SEL have to remain unchanged except bit 2 (SEL_R_IN) that needs to be set to level 1.

5.14. Analog input common mode calibration

It is possible to modify the analog input common mode calibrated during manufacturing. The modification is done via the register CM_IN defined in the Master SPI.
To modify the CM_IN value (from OTP), it is mandatory to modify register OTP_SPI_SEL defined in the Master SPI: bit SEL_CM_IN has to be set to 1 level.

Table 41. Master SPI - OTP_SPI_SEL register description

Bit (15 down to 4)	Bit 3	Bit 2	Bit 1	Bit 0
	0	SEL_R_IN	SEL_CM_IN	SEL_OFFSET_CAL

Bit label	Value	Description	Default Setting (hexa)	Address for R/W (hexa)
SEL_OFFSET_CAL	0	OFFSET_CAL OTP values are selected	0	16
	1	OFFSET_CAL SPI registers are selected		
SEL_CM_IN	0	CM_IN OTP value is selected		
	1	CM_IN SPI register is selected		
SEL_R_IN	0	R_IN OTP value is selected		
	1	R_IN SPI register is selected		

Table 42. Master SPI - CM_IN register description

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
											CM_IN <4:0>				

Bit label	Description	SPI Default Setting (hexa)	Address for R/W (hexa)	Address for read only (hexa)
CM_IN <4:0>	Analog input common mode value	0010	1B	6F

Table 43. CMIRef value according to CM_IN register

CM_IN value (hexa)	CMIRef typical value for V_{CCA} = 4.8V (Volt)
1F	2.96
10	3.15
0	3.34
Excursion	0.38
Step	$12.3.10^{-3}$

Procedure to have only CM_IN value from SPI while all other settings from OTP:
WRITE @ CHANNEL_SEL 0007 # Master SPI is selected
WRITE @OTP_SPI_SEL 0002 # Now, CM_IN value comes from SPI register
WRITE @CM_IN xxxx # The SPI CM_IN value is taken into account
Note: all other Master SPI settings come from OTP value (independently from previous configuration)
To conserve the previous configuration and change only CM_IN, all bits of register OTP_SPI_SEL have to remain unchanged except bit 1 (SEL_CM_IN) that needs to be set to level 1.

5.15. Test modes: Flash and Ramp

Two test modes can be used for debug and testability:

- Flash mode is useful to align the interface between the ADC and the FPGA.
- In Ramp mode, the data output is a 12 bit ramp on the four ADC cores

The activation of these test modes are done the Channel SPI via the TEST_MODE register described below:

Table 44. Channel SPI - TEST_MODE register description

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
									TEST_MODE <5:0>						TEST_ENA

Bit label	Value (binary)	Description	Default Setting	Address for R/W (hexa)
TEST_ENA	0	Test mode disabled (default value)	0	5D
	1	Test mode enabled		
TEST_MODE <5:0>	000 000	Reserved		
	000 001	Reserved		
	000 010	Reserved		
	000 110	Flash mode selected		
	000 100	Ramp mode selected		
	111 000	Reserved		
	110 000	Reserved		

The length of the flash can be modified via the FLASH_LENGTH register defined in Channel SPI.

Table 45. Channel SPI - FLASH_LENGTH register description

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
										FLASH_LENGTH <5 :0>					

Bit label	Description	Default Setting (hexa)	Address for R/W (hexa)
FLASH_LENGTH <5:0>	Programming of the flash length. User can programme 2 to 64 internal clock cycles	0018	69

Procedure for FLASH_LENGTH adjustment:
WRITE @CHANNEL_SEL 0004 # ALL channels selected
WRITE @FLASH_LENGTH xxxx

Table 46. Flash length according to FLASH_LENGTH register

FLASH_LENGTH value (hexa)	Flash length (external clock cycles)
3F	256
1F	128
18	100
2	12
1	8
0	Not to be used
Excursion	248
Step	4

Important note:
After enabling Test Modes, a SYNC is mandatory to have a proper synchronization between four ADC cores.

5.16. PRBS: Pseudo Random Bit Sequence

The PRBS could be used as a test mode (recognition by FPGA of the sequence sent by the ADC) or data scrambling. The idea is to add the same pseudo random bit to all output data including Parity bit and In Range bit.
When this mode is activated, the Pseudo Random Bit is sent every N clock cycles, with N ranging from 1 to 31.
PRBS uses the following polynomial to generate the sequence: $X^7 + X^6 + 1$

Figure 22. PRBS encoding data

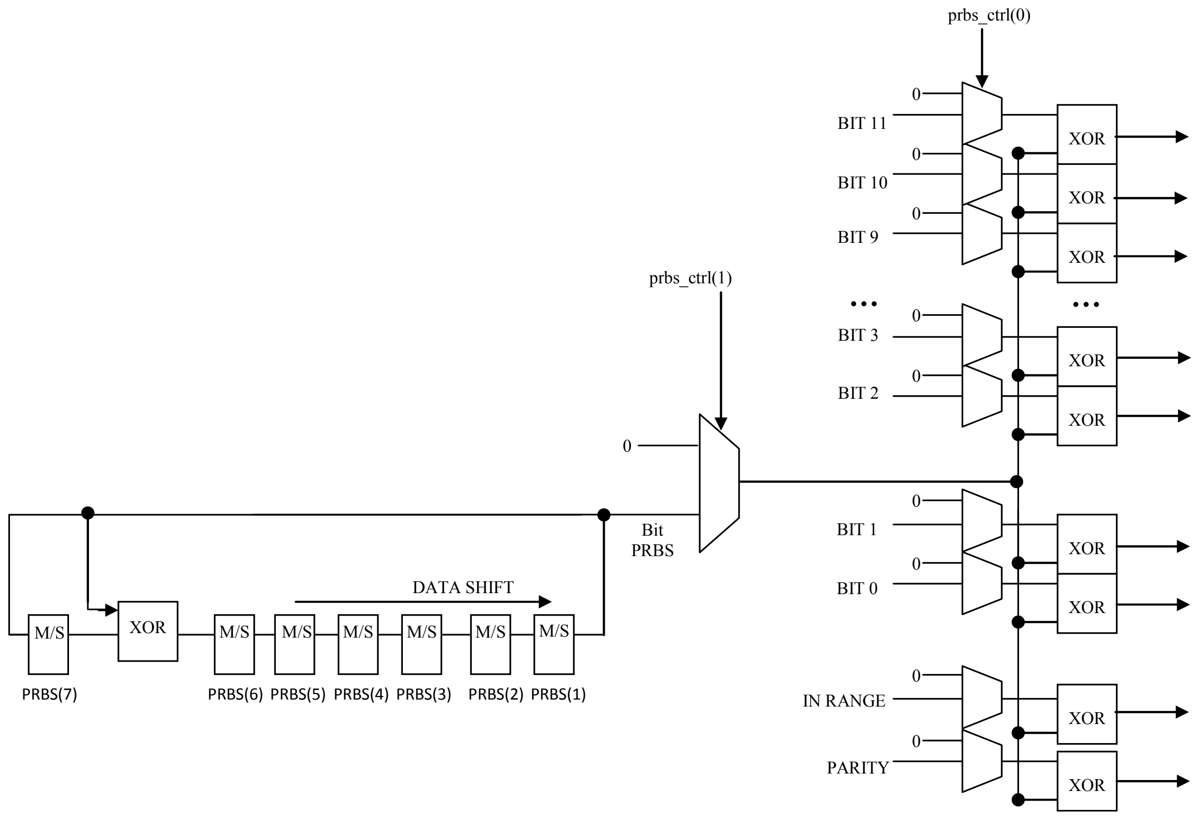


Table 47. Channel SPI - PRBS_CTRL description

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
														PRBS_MODE	PRBS_ENA

Bit label	Value	Description	Default Setting	Address for R/W (hexa)
PRBS_ENA	0	PRBS disabled (default)	0	5F
	1	PRBS enabled		
PRBS_MODE	0	SIGNAL enabled (default)		
	1	SIGNAL disabled		

Procedure to launch PRBS mode:
WRITE @CHANNEL_SEL 0004 # ALL channels selected
WRITE @PRBS_CTRL 0003 # PRBS ONLY
WRITE @PRBS_CTRL 0001 # PRBS+SIGNAL

Procedure to stop PRBS mode:
WRITE @PRBS_CTRL 0000 # SIGNAL ONLY

By default PRBS mode is disabled.
A SYNC pulse synchronizes the PRBS on the 4 channels.

Figure 23. Example of 2 ramps with PRBS mode disabled (default mode)

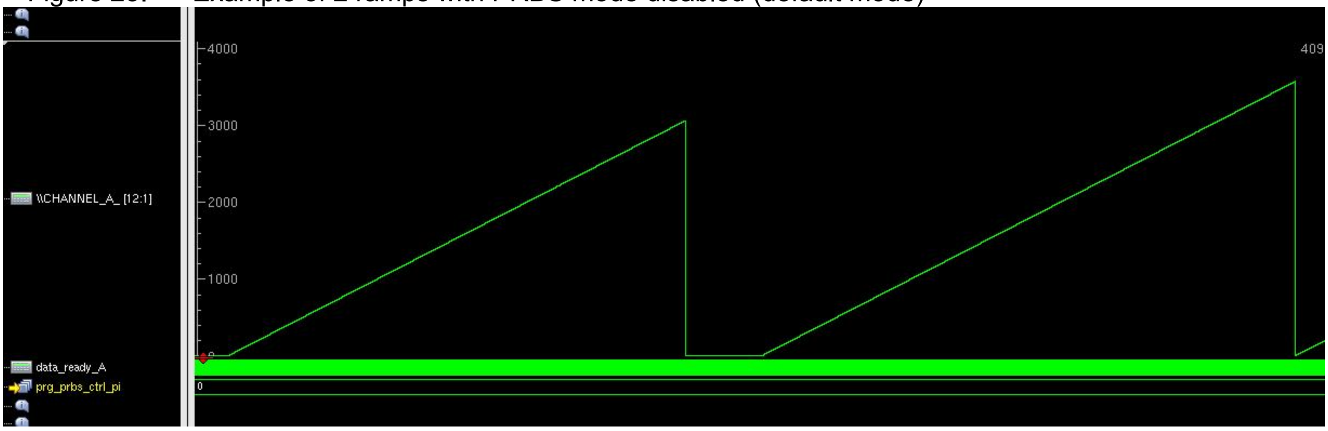


Figure 24. Example of PRBS mode only

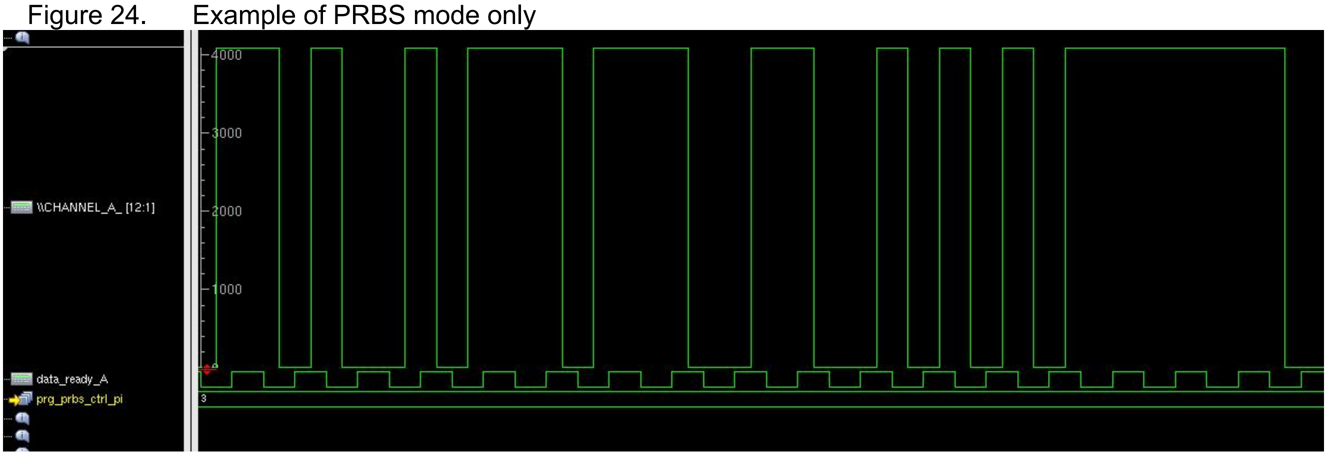


Figure 25. Example of PRBS mode only with 4 channels synchronized

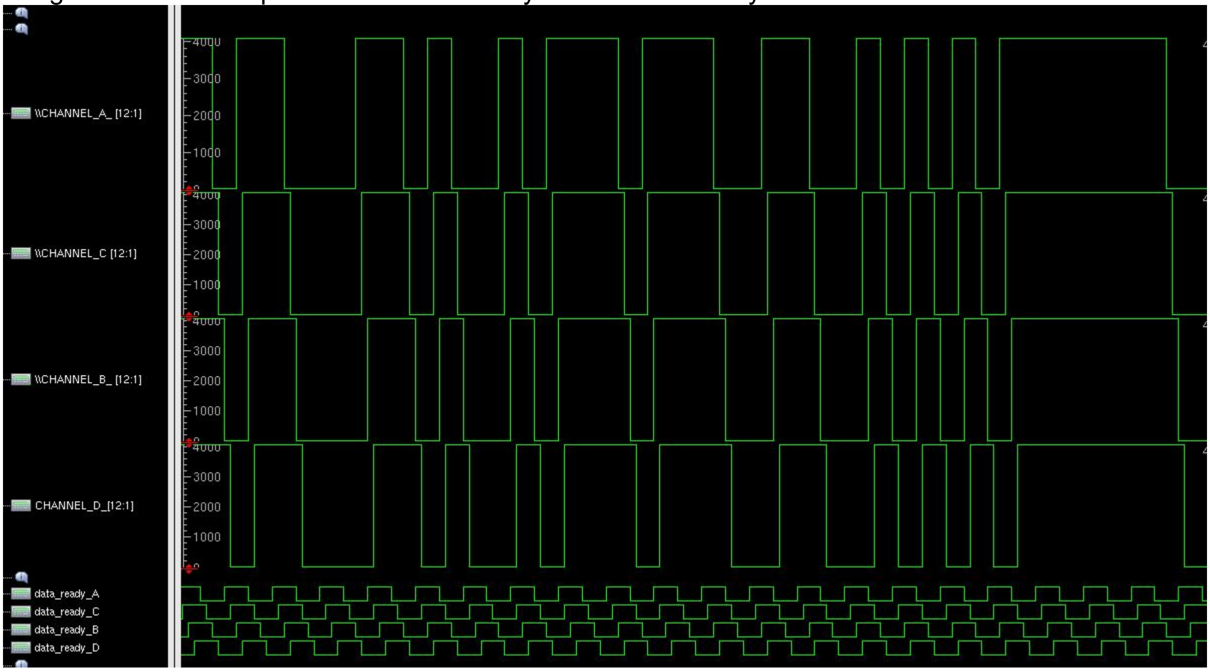
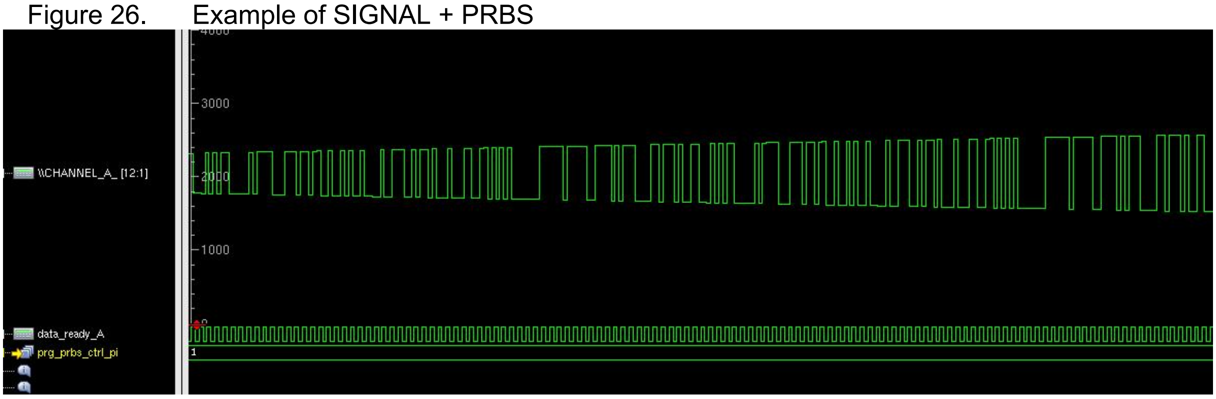


Figure 26. Example of SIGNAL + PRBS



5.17. Chip identification

It is possible to read the chip ID in using the register CHIP_ID defined in the Master SPI.

Chip ID is 0x62C for all part numbers except for EVP12AS350TP-V2 whose chip ID is 0x618

Procedure to read CHIP_ID:
WRITE @CHANNEL_SEL 0007 # Master SPI selected
READ @CHIP_ID

5.18. CRC status

It is possible to read CRC status of OTP: this verification is optional.

Reference CRC values written in OTP during manufacturing can be compared to values recalculated after the SPI procedure described below. The result of the comparison is written in the CRC_OTP_STATUS register defined in Master SPI.

Table 48. Master SPI – CRC_OTP_STATUS register description

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
								CRC MASTER STATUS	D_CRC STATUS	C_CRC STATUS	B_CRC STATUS	A_CRC STATUS	0		OTP STATUS

Bit label	Value	Description	Address Read Only (hexa)
OTP_STATUS	0	OTP data (Master SPI only) are not ready.	05
	1	OTP data (Master SPI only) are ready and available	
D_CRC_STATUS	0	CRC check channel D failed	
	1	CRC check channel D is successful	
C_CRC_STATUS	0	CRC check channel C failed	
	1	CRC check channel C is successful	
B_CRC_STATUS	0	CRC check channel B failed	
	1	CRC check channel B is successful	
A_CRC_STATUS	0	CRC check channel A failed	
	1	CRC check channel A is successful	
MASTER_CRC_STATUS	0	CRC check MASTER failed	
	1	CRC check MASTER is successful	

PROCEDURE TO CHECK CRC:

RSTN # low state during 10 µs min
WRITE @01 0004 # ALL Channels selected
WRITE @5D 0001 # TEST_MODE enabled (clock used to calculate CRC is activated)
WAIT 4500 external clock cycles # Minimum waiting time for CRC calculation
WRITE @01 0007 # Master SPI selected
READ @05 # read bit (7 down to 3)
⇨ 1 means OK
⇨ 0 means CRC failed

5.19. OTP status

It is possible to verify that OTP cells are awaken (fuses are ready to be used) in reading OTP_STATUS defined in Channel SPI (see Table 49) and CRC_OTP_STATUS defined in Master SPI (see Table 50)

Table 49. Channel SPI - OTP_STATUS register description

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
															OTP_STATUS

Bit label	Value	Description	Address (Read Only) (hexa)
OTP_STATUS	0	OTP (Channel SPI only) are not ready	5A
	1	OTP (Channel SPI only) are ready and available	

This signal starts to 0 level and goes to 1 level, 1 ms maximum after the digital reset.

Table 50. Master SPI – CRC_OTP_STATUS register description

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
								CRC MASTER STATUS	D_CRC STATUS	C_CRC STATUS	B_CRC STATUS	A_CRC STATUS	0		OTP STATUS

Bit label	Value	Description	Address Read Only (hexa)
OTP_STATUS	0	OTP data (Master SPI only) are not ready.	05
	1	OTP data (Master SPI only) are ready and available	
D_CRC_STATUS	0	CRC check channel D failed	
	1	CRC check channel D is successful	
C_CRC_STATUS	0	CRC check channel C failed	
	1	CRC check channel C is successful	
B_CRC_STATUS	0	CRC check channel B failed	
	1	CRC check channel B is successful	
A_CRC_STATUS	0	CRC check channel A failed	
	1	CRC check channel A is successful	
MASTER_CRC_STATUS	0	CRC check MASTER failed	
	1	CRC check MASTER is successful	

PROCEDURE TO CHECK OTP STATUS:

OTP_STATUS is available 1 ms after a reset (pin RSTN)

```
WRITE  @01  0007          # Master SPI selected
READ   @05                # OTP_STATUS register read only

WRITE  @01  0000          # Channel A selected
READ   @5A                # OTP_STATUS register read only

WRITE  @01  0001          # Channel B selected
READ   @5A                #  OTP_STATUS register read only

WRITE  @01  0002          # Channel C selected
READ   @5A                # OTP_STATUS register read only

WRITE  @01  0003          # Channel D selected
READ   @5A                # OTP_STATUS register read only
```

- ⇨ READ 1 means OTP are ready
- ⇨ READ 0 means OTP doesn’t work !

5.20. Parity Bit

The parity of the 12 output bit of each data is calculated in performing an XOR combination between the 12-bit of output data.

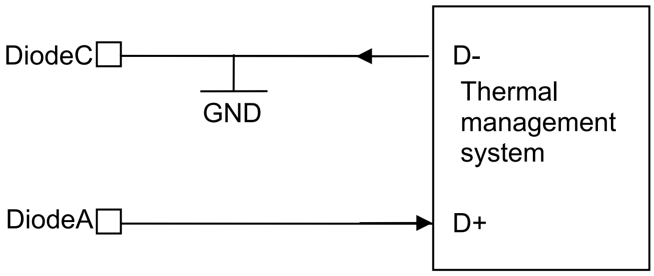
5.21. In Range Bit

In Range bits (AIR/AIRN, BIR/BIRN, CIR/CIRN, DIR/DIRN) are switched to level 0 when the analog input exceed ADC Full scale. See section 3.7.

5.22. Die junction temperature monitoring diode

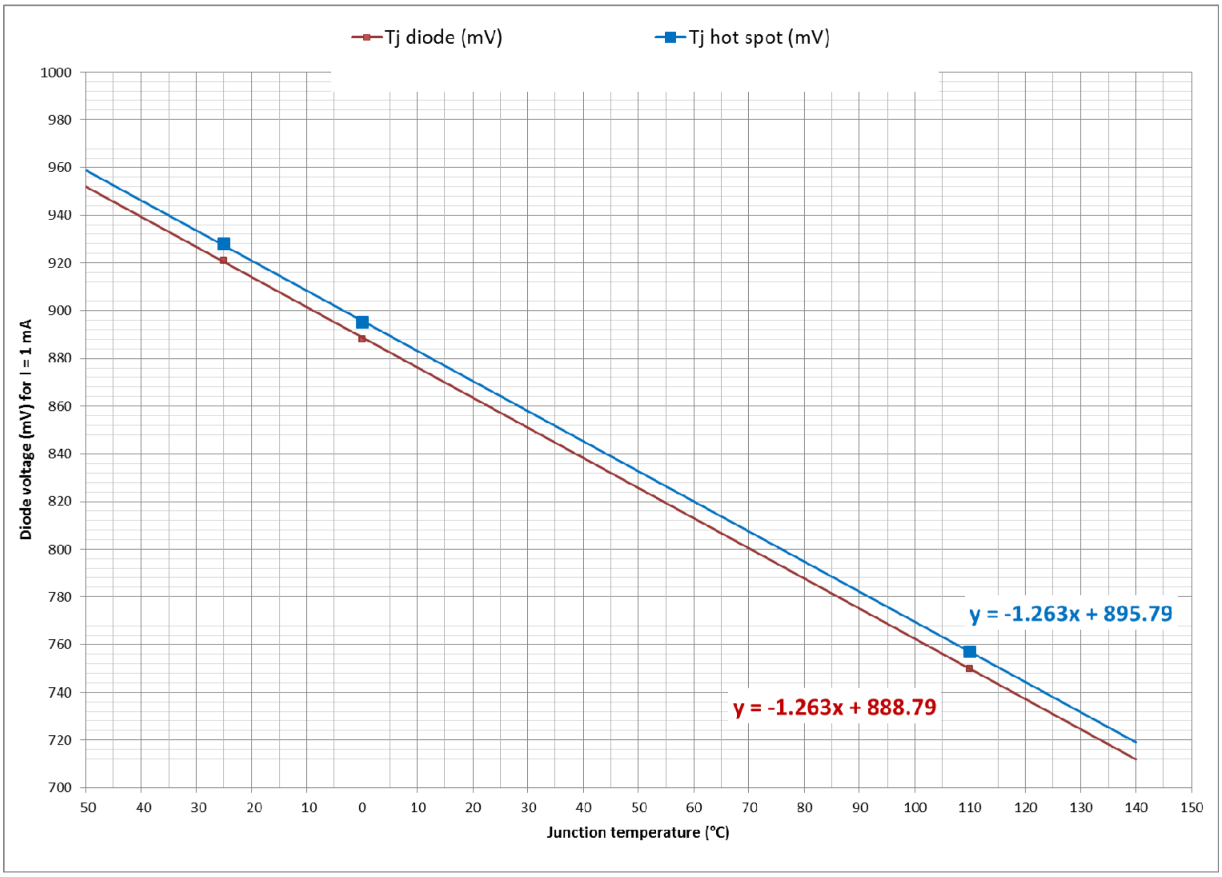
DIODE: Two pins are provided so that the diode can be probed using standard temperature sensors.
The diode measures the junction temperature which is 7°C below the hot spot (but higher than die average temperature)

Figure 27. Junction temperature monitoring diode system



Note: If the diode function is not used, the diode pins can be left unconnected (open). If diode is used it is mandatory to connect DiodeC to GND.

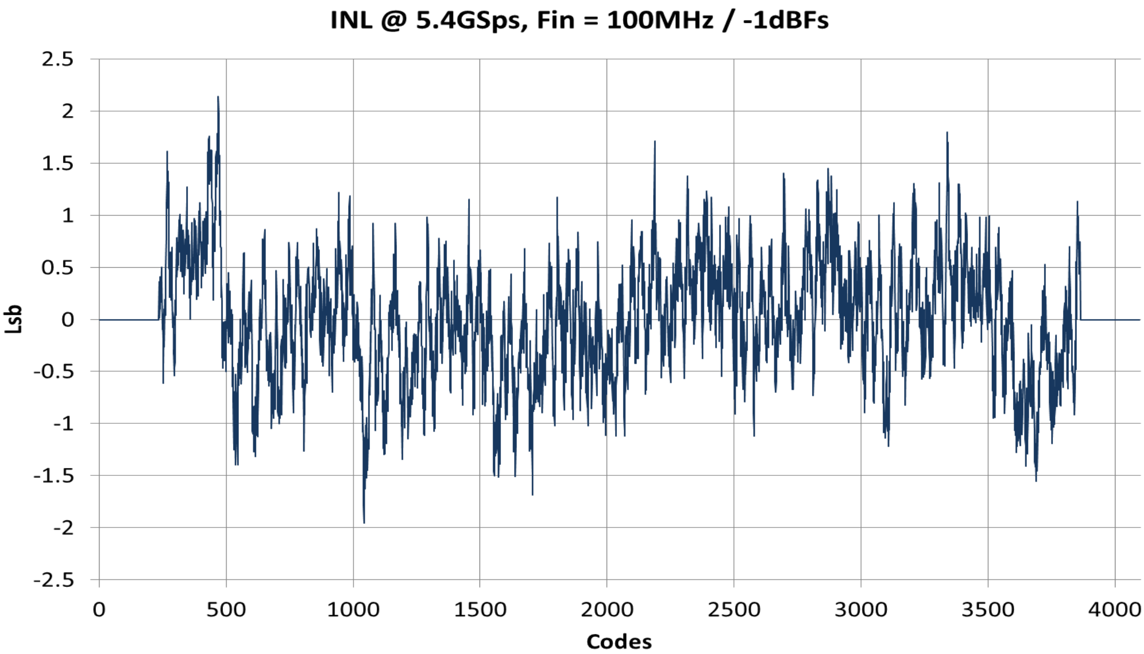
Figure 28. Temperature diode characteristics for I=1 mA (with DiodeC=GND)



6 Characterization result

6.1. INL at 5.4Gsps

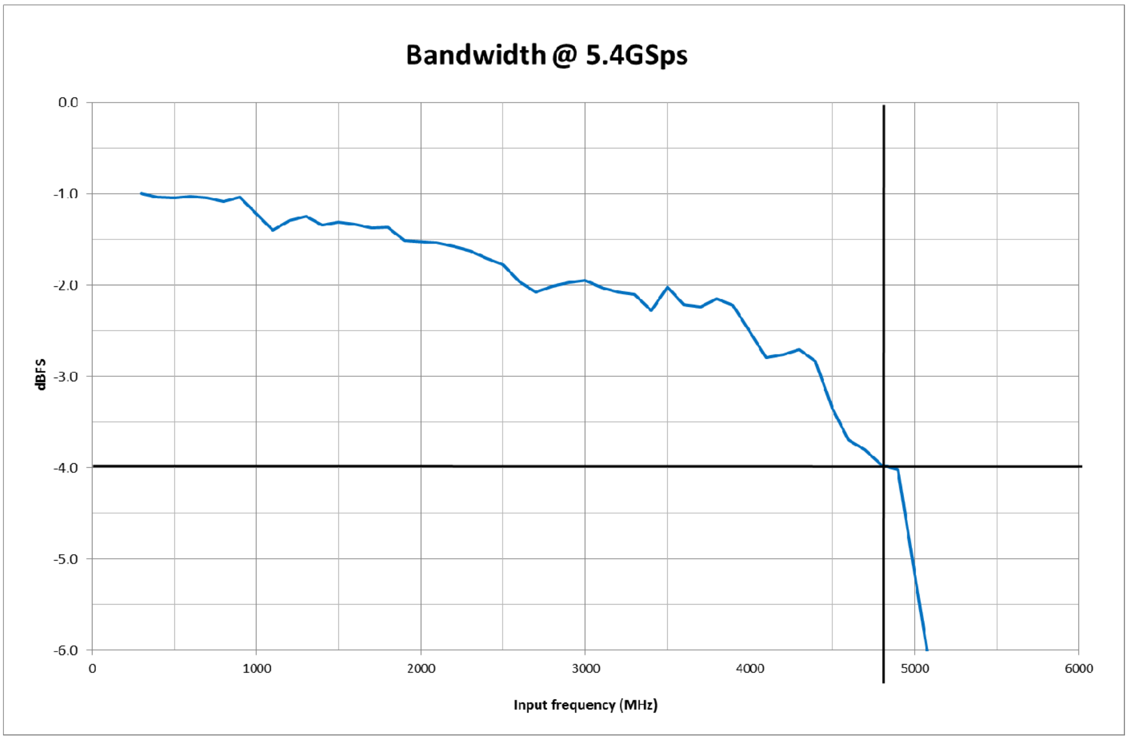
Figure 29. INL performances at 5.4GSps



Typical supplies - at ambient temperature - 4 cores interleaved (Staggered mode).

6.2. ADC output bandwidth (-3dB)

Figure 30. Bandwidth up to 4800MHz

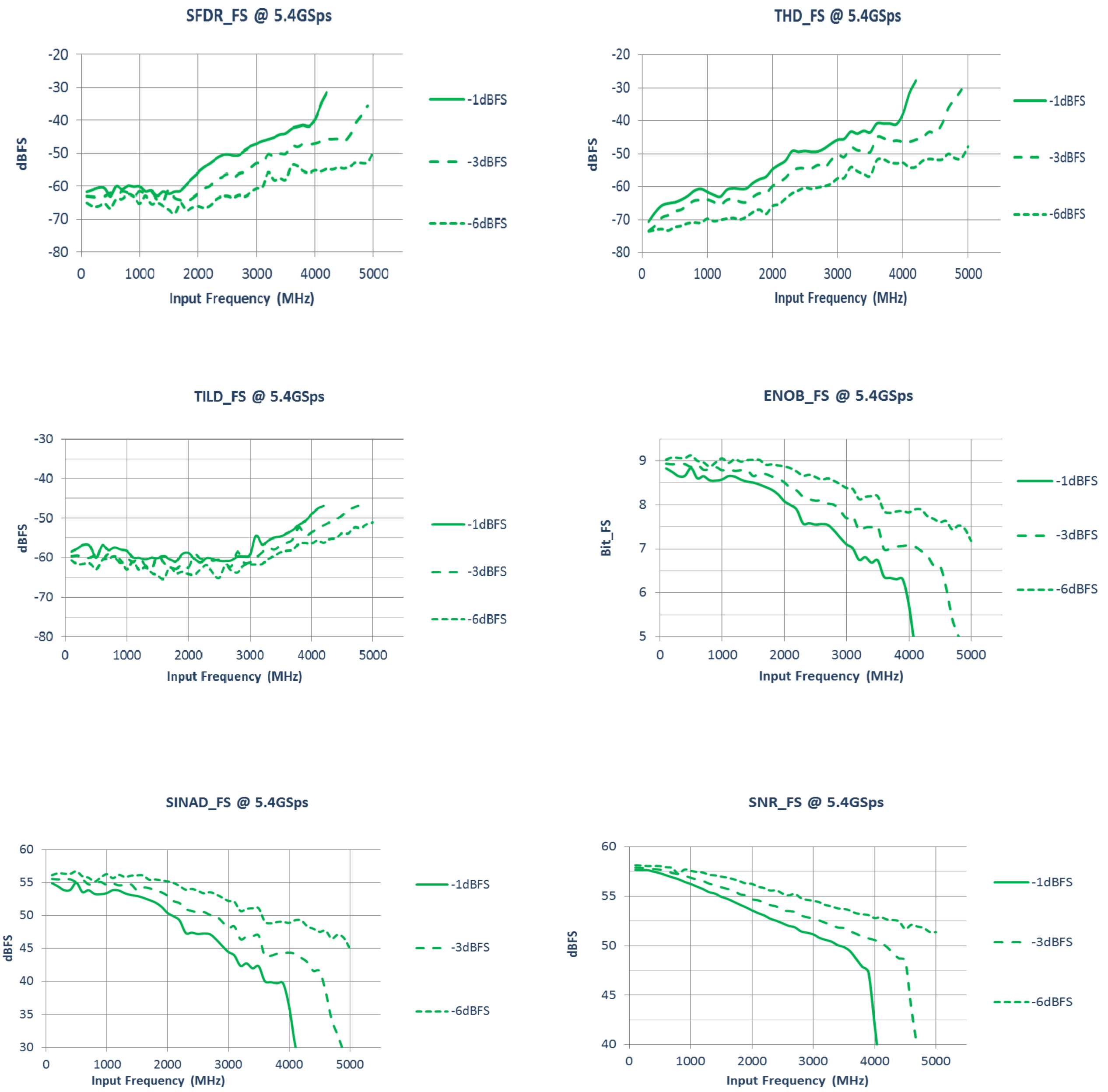


Typical supplies - at ambient temperature – one core

The applied input level has been calibrated so that the ADC SFSR should remain equal to -1dBFS for each input frequency.

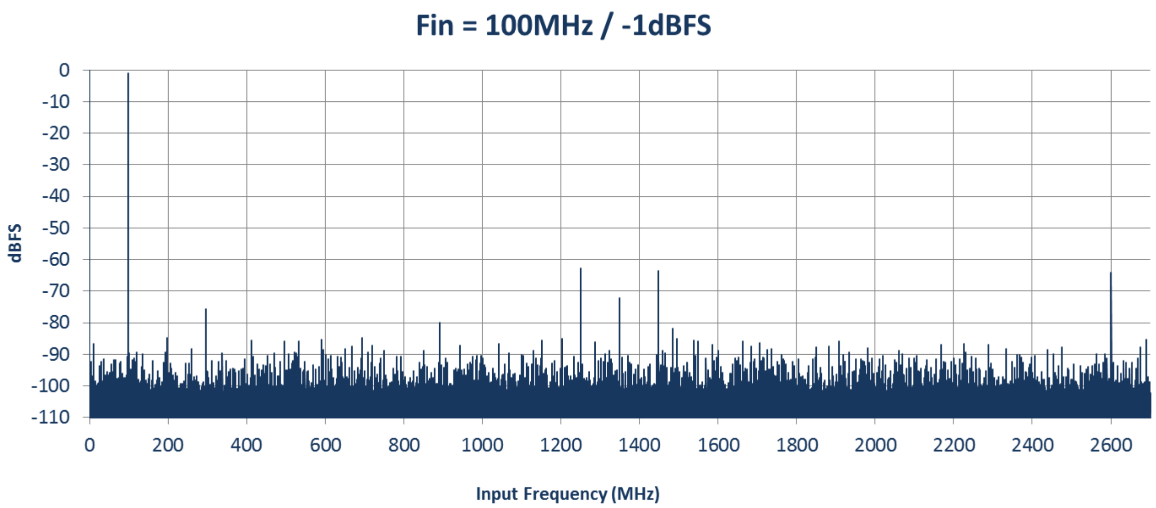
6.3. FFT performance versus Fin and Ain at 5.4Gsps

Figure 31. : SFDR, THD, ENOB, SINAD and SNR performances at versus input frequency at 5.4GSps



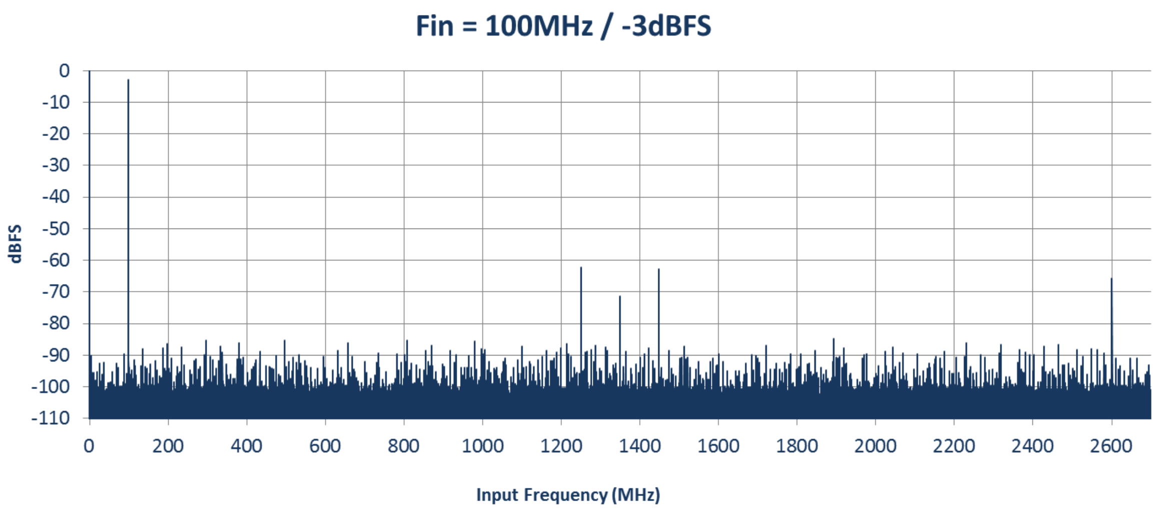
Typical supplies - at ambient temperature - 4 cores interleaved (Staggered mode).

Figure 32. FFT at 5.4GSps and Fin = 100MHz / -1dBFS



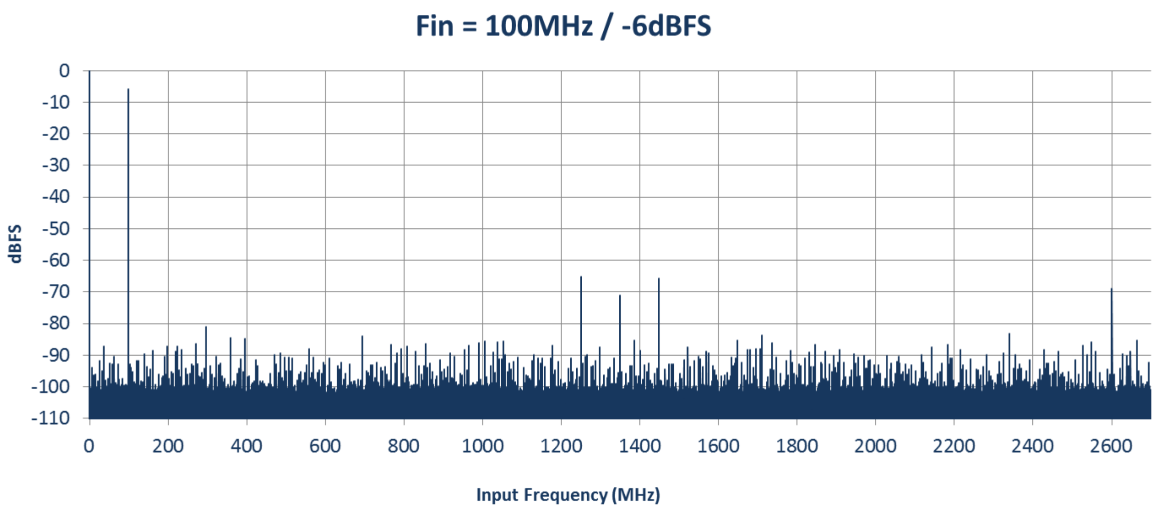
Typical supplies - at ambient temperature - 4 cores interleaved (Staggered mode).

Figure 33. FFT at 5.4GSps and Fin = 100MHz / -3dBFS



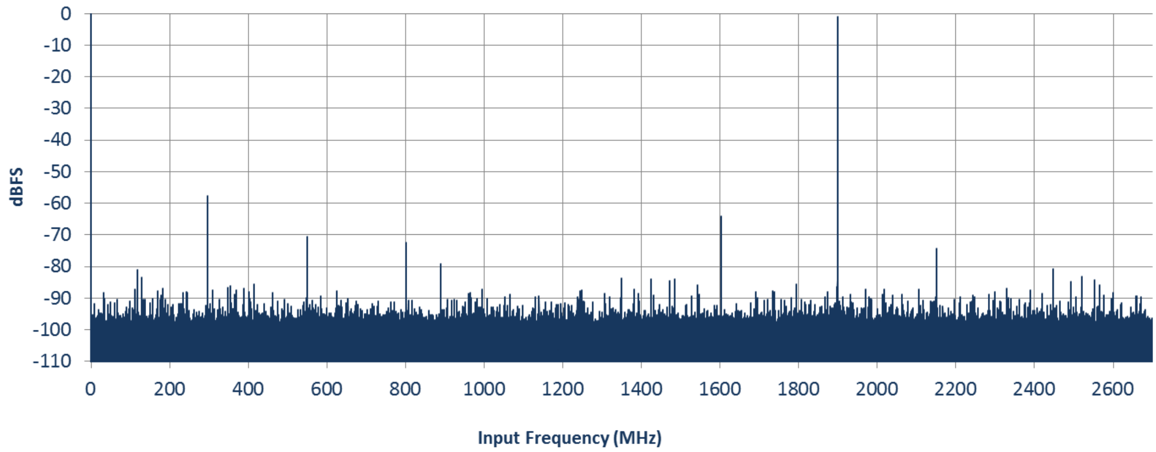
Typical supplies - at ambient temperature - 4 cores interleaved (Staggered mode).

Figure 34. FFT at 5.4GSps and Fin = 100MHz / -6dBFS



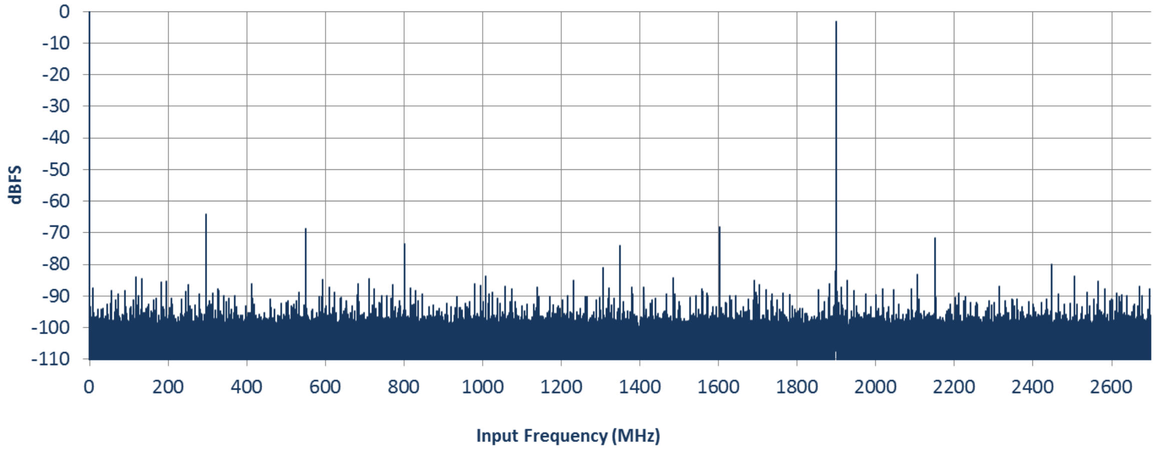
Typical supplies - at ambient temperature - 4 cores interleaved (Staggered mode).

Figure 35. FFT at 5.4GSps and Fin = 1900MHz / -1dBFS



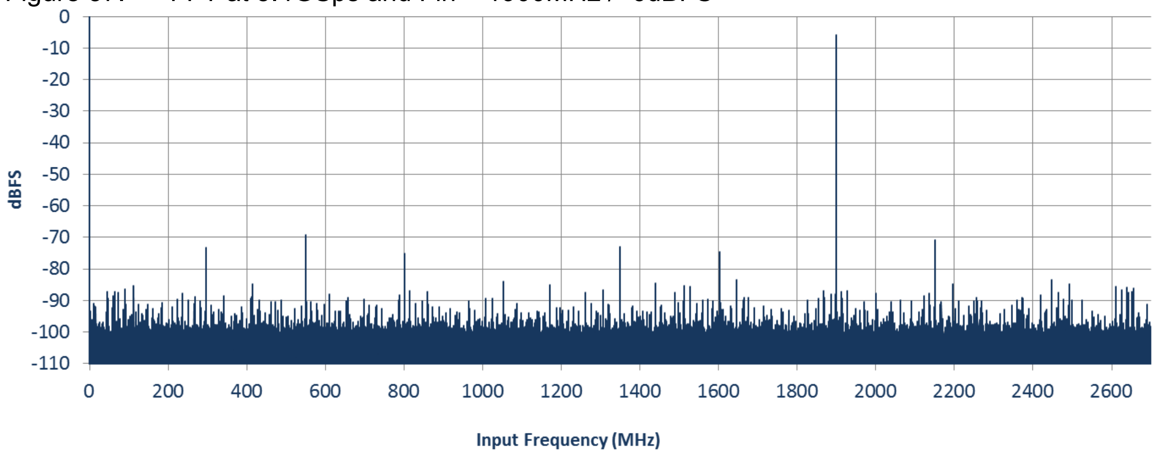
Typical supplies - at ambient temperature - 4 cores interleaved (Staggered mode).

Figure 36. FFT at 5.4GSps and Fin = 1900MHz / -3dBFS



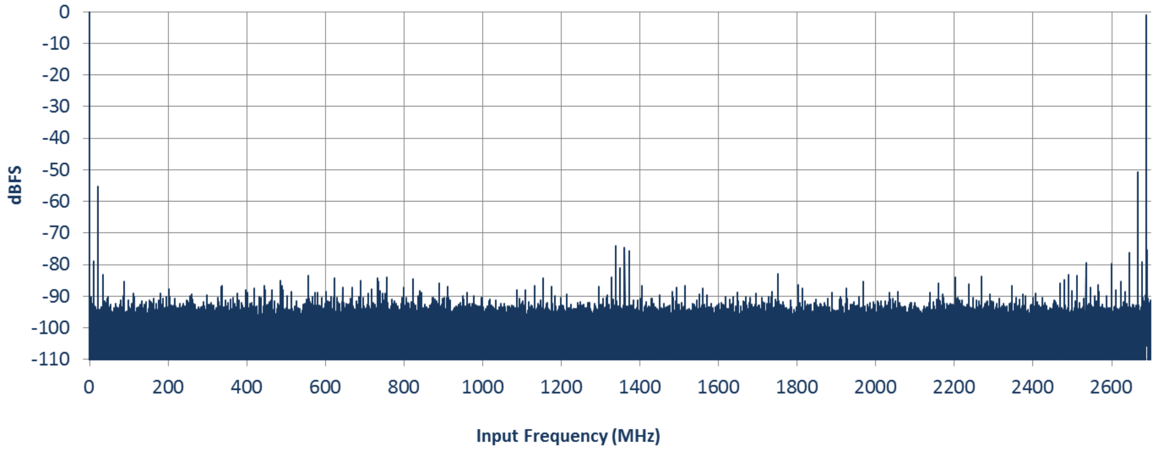
Typical supplies - at ambient temperature - 4 cores interleaved (Staggered mode).

Figure 37. FFT at 5.4GSps and Fin = 1900MHz / -6dBFS



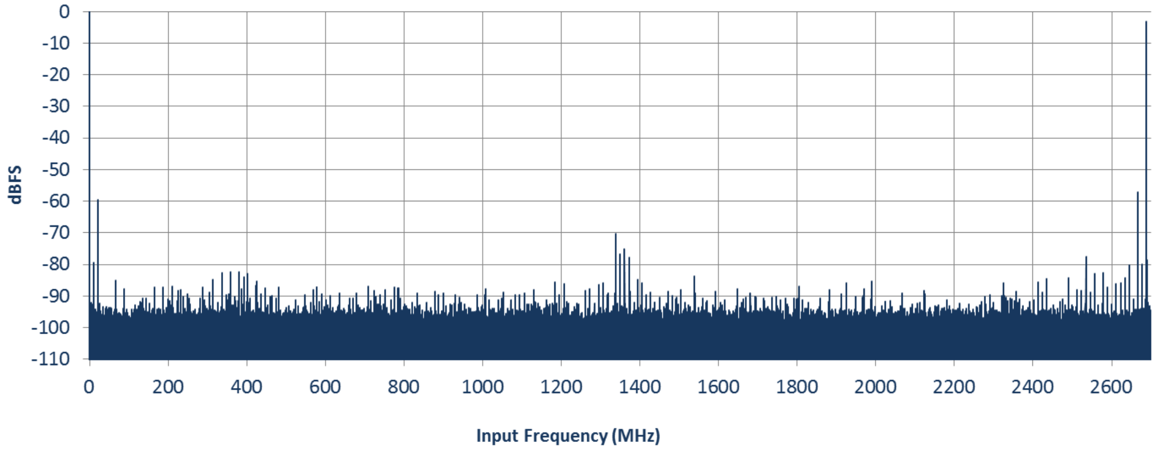
Typical supplies - at ambient temperature - 4 cores interleaved (Staggered mode).

Figure 38. FFT at 5.4GSps and Fin = 2690MHz / -1dBFS



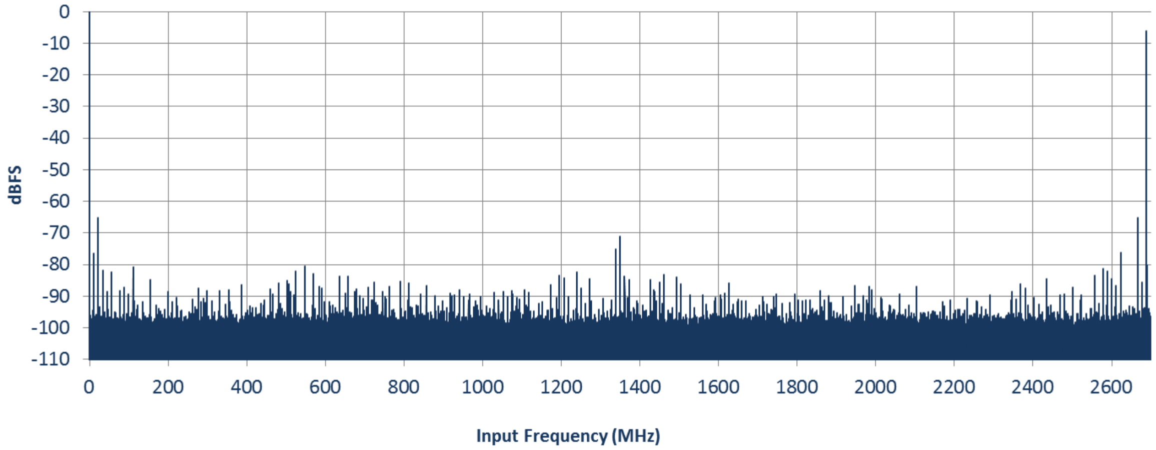
Typical supplies - at ambient temperature - 4 cores interleaved (Staggered mode).

Figure 39. FFT at 5.4GSps and Fin = 2690MHz / -3dBFS



Typical supplies - at ambient temperature - 4 cores interleaved (Staggered mode).

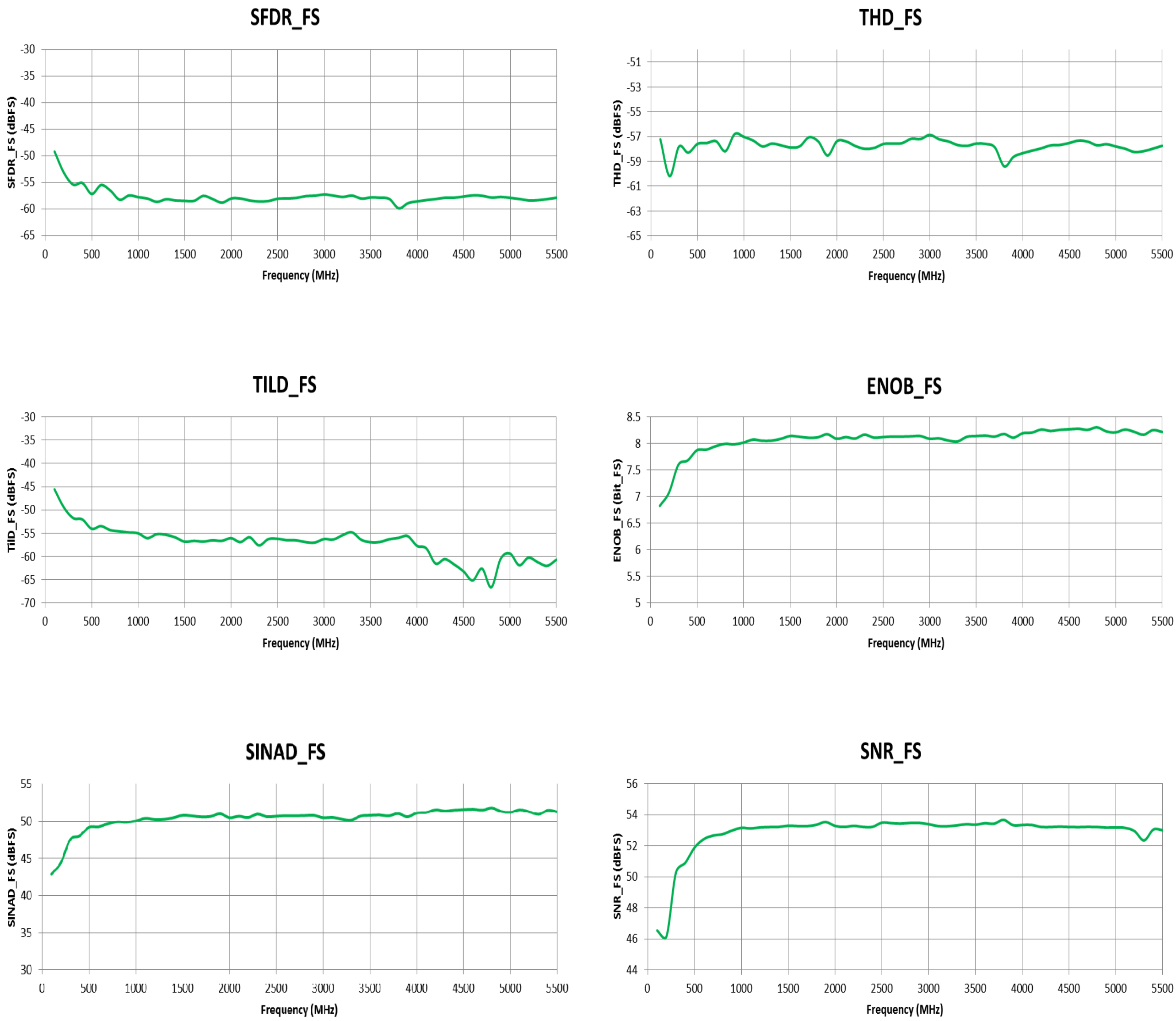
Figure 40. FFT at 5.4GSps and Fin = 2690MHz / -6dBFS



Typical supplies - at ambient temperature - 4 cores interleaved (Staggered mode).

6.4. FFT performance versus Fclock (Fin=1900MHz -1dBFS)

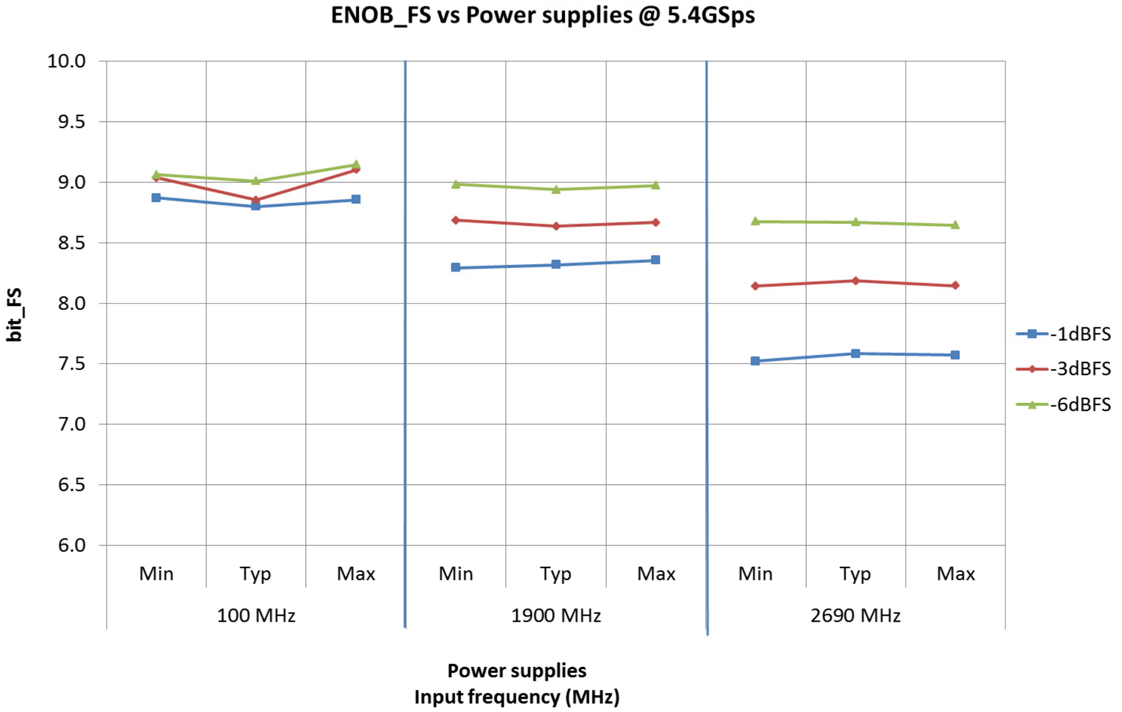
Figure 41. : SFDR, THD, TILD, ENOB, SINAD and SNR performances versus clock frequency at input frequency 1900MHz (-1dBFs).



Typical supplies - at ambient temperature - 4 cores interleaved (Staggered mode).

6.5. ENOB performance versus temperature and power supplies

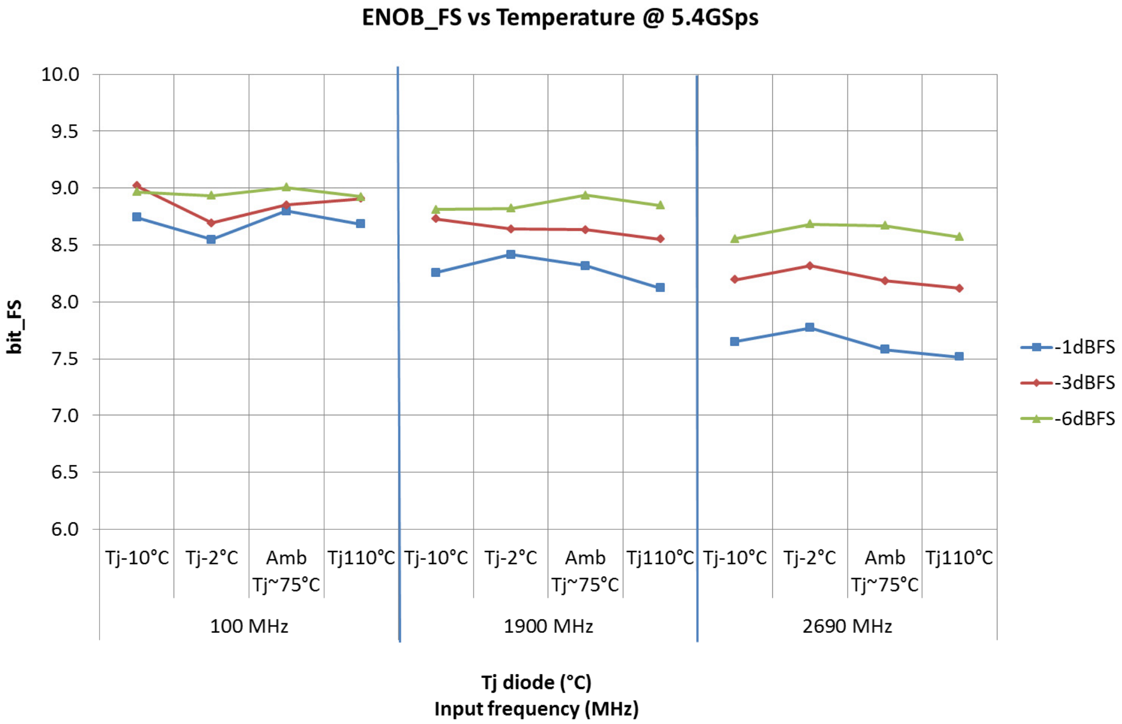
Figure 42. ENOB performance versus power supplies



Versus power supplies - at ambient temperature - 4 cores interleaved (Staggered mode).

Figure 43. ENOB performance versus temperature

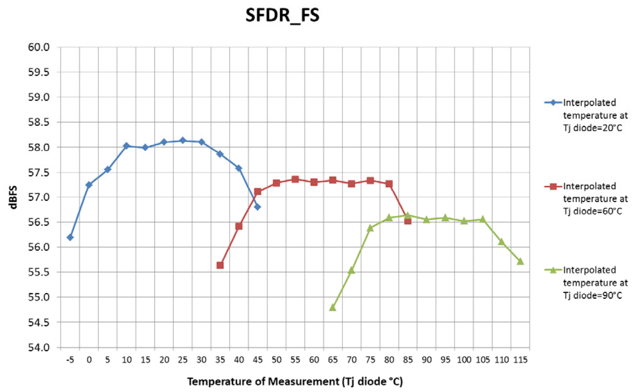
These acquisitions are done at typical supplies in 4 cores interleaved (Staggered mode).

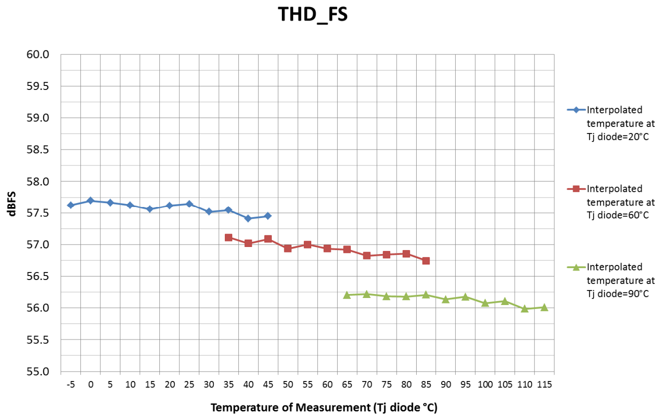


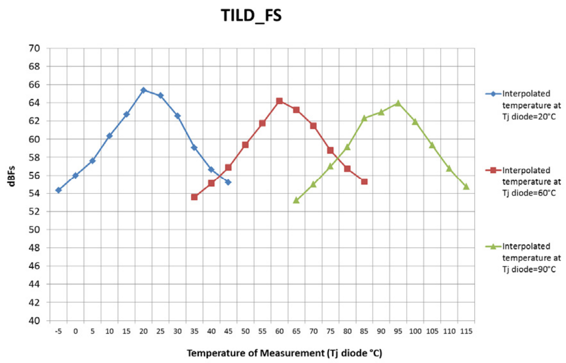
Versus Temperature - Typical supplies - 4 cores interleaved (Staggered mode).

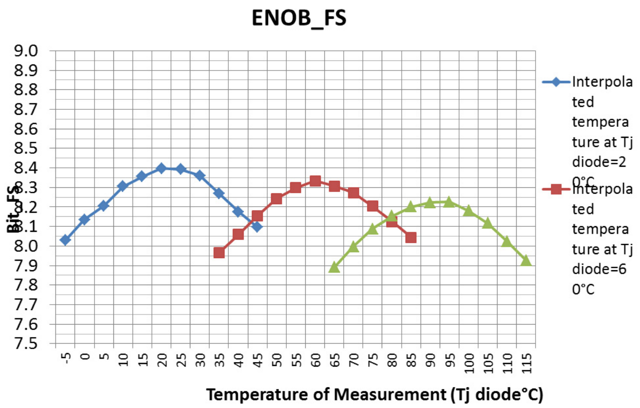
6.6. Impact of the temperature interpolation on FFT performance

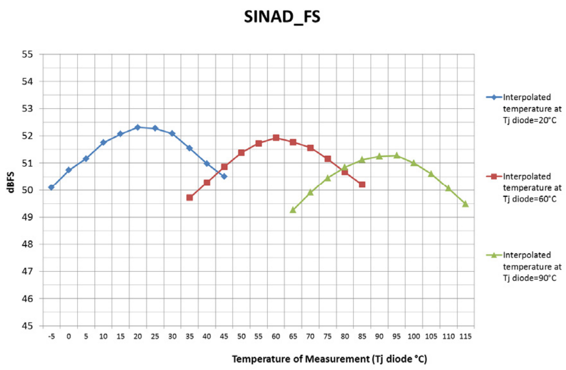
Figure 44. Impact of the temperature interpolation on SFDR, THD, TILD, ENOB, SINAD and SNR performances. Fc = 5Gsps, Fin = 1900MHz, Ain = -1dBFS

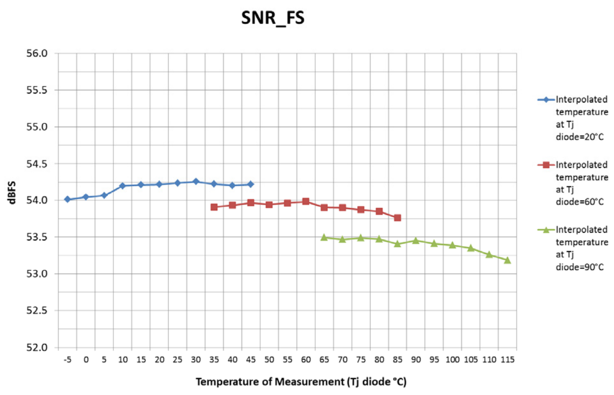








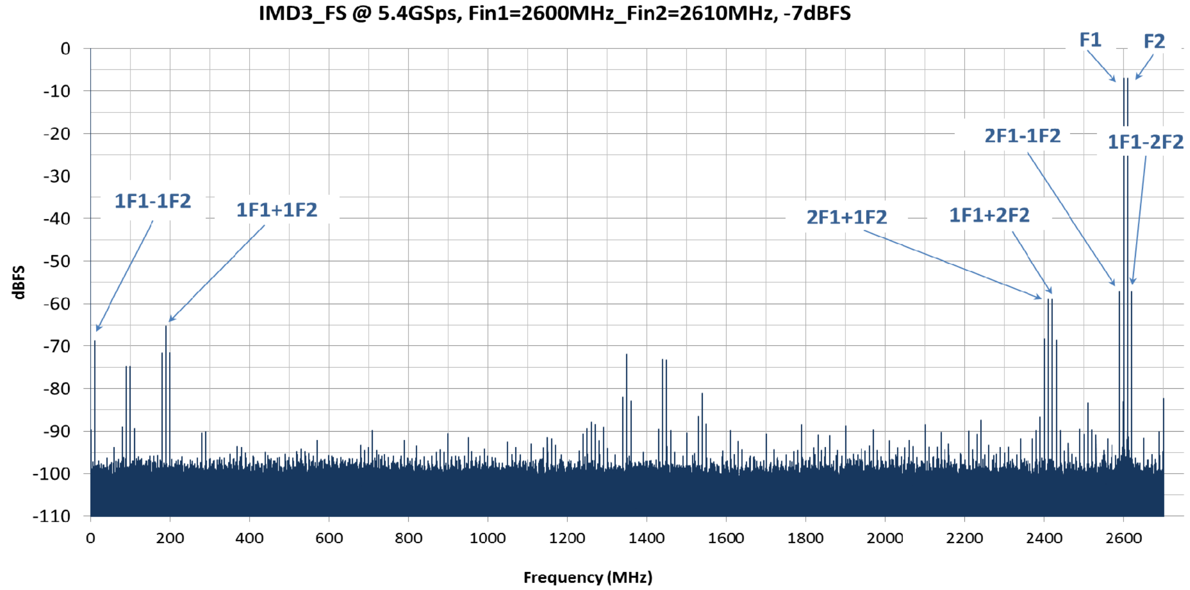




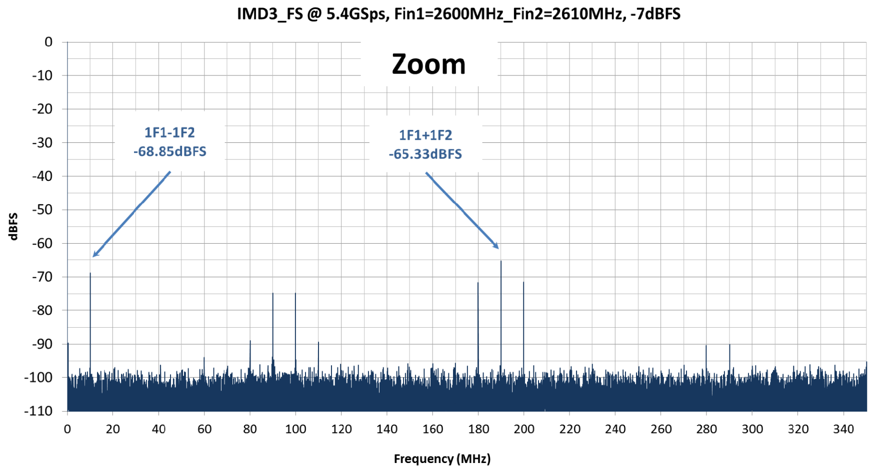
Versus Temperature - Typical supplies - 4 cores interleaved (Staggered mode).

6.7. IMD3 at 5.4Gsps

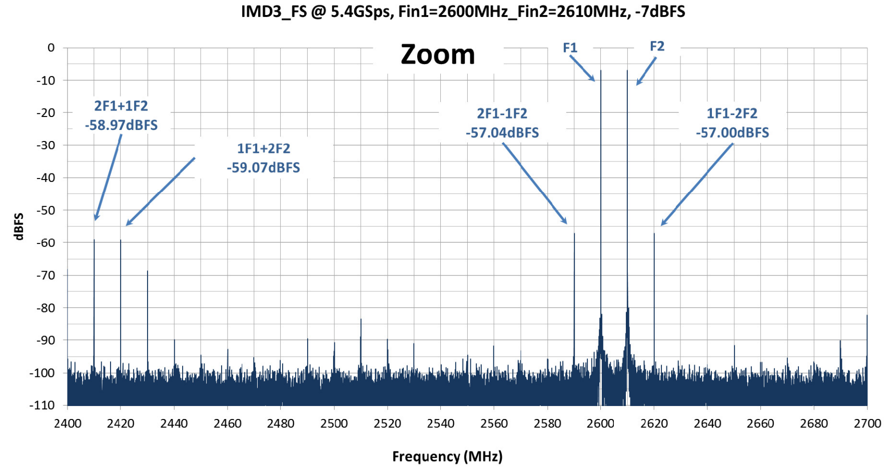
Figure 45. IMD3 at 5.4GSps Fin1 = 2600MHz, Fin2 = 2610 MHz, -7dBFS



Typical supplies - at ambient temperature - 4 cores interleaved (Staggered mode).

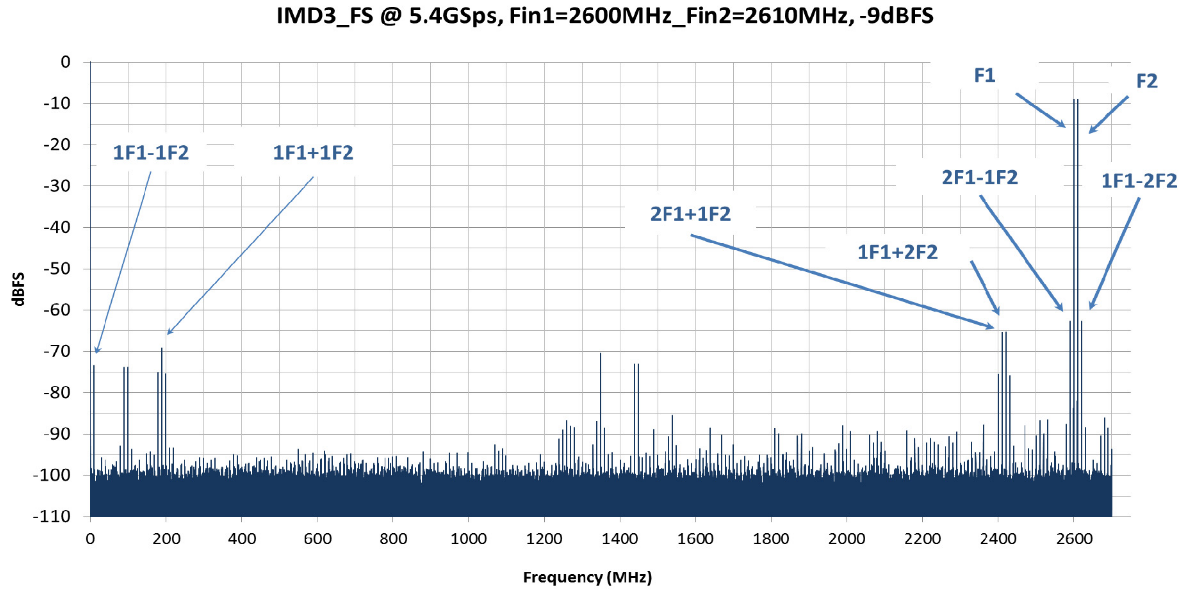


Typical supplies - at ambient temperature - 4 cores interleaved (Staggered mode).

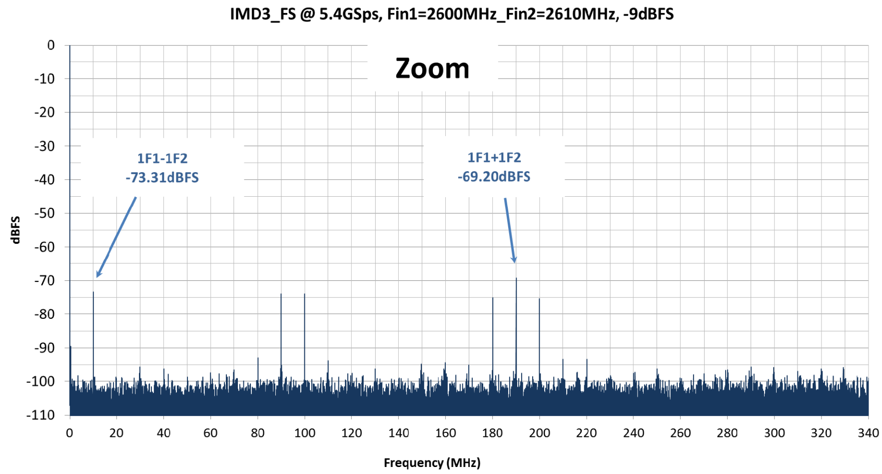


Typical supplies - at ambient temperature - 4 cores interleaved (Staggered mode).

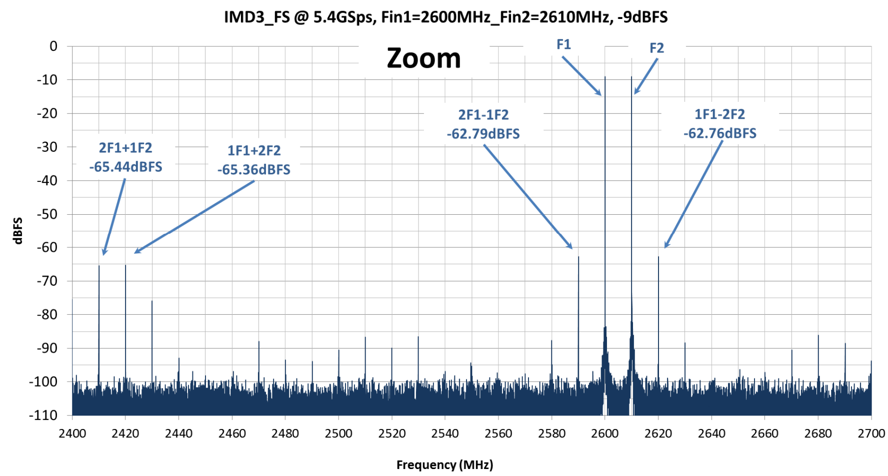
Figure 46. IMD3 at 5.4GSps Fin1 = 2600MHz, Fin2 = 2610 MHz, -9dBFS



Typical supplies - at ambient temperature - 4 cores interleaved (Staggered mode).

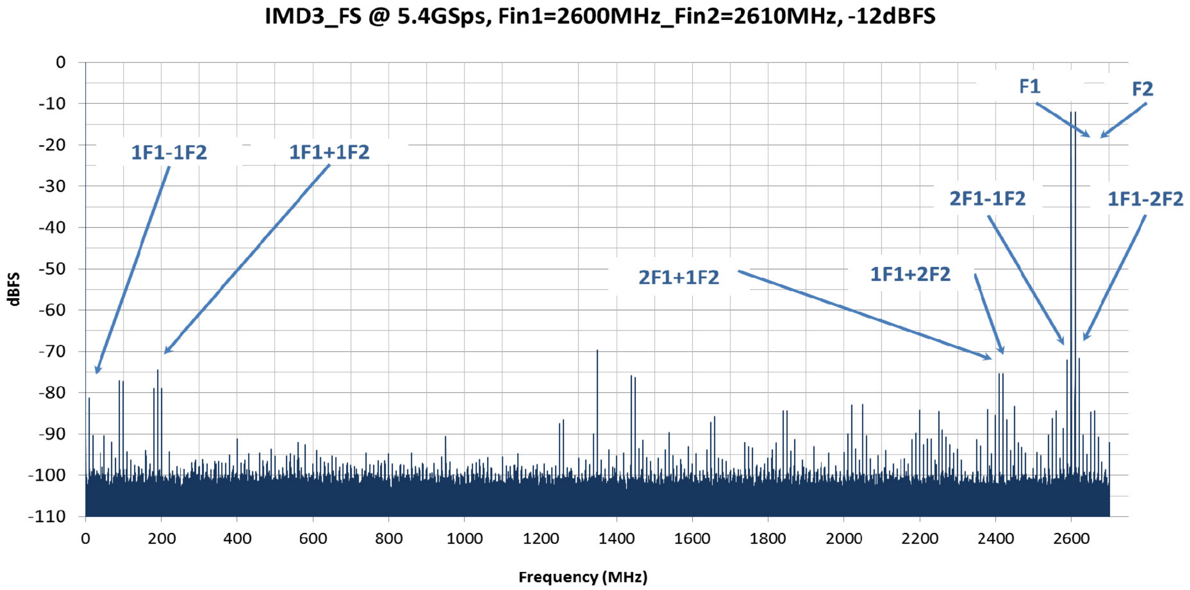


Typical supplies - at ambient temperature - 4 cores interleaved (Staggered mode).

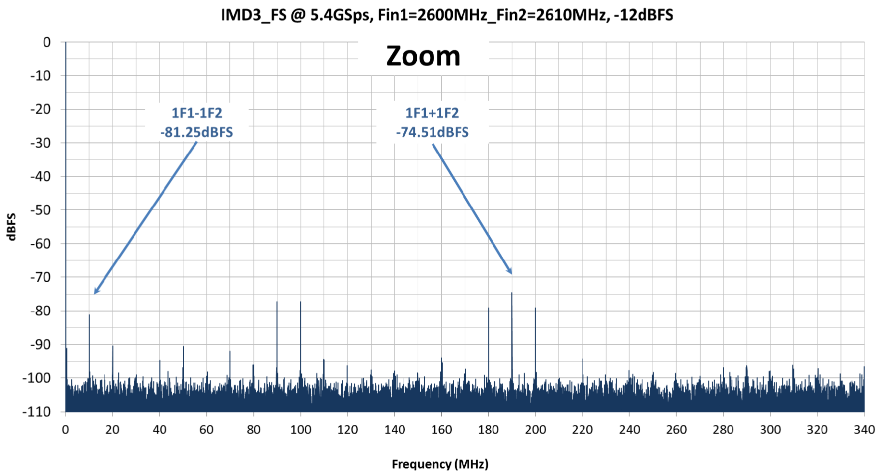


Typical supplies - at ambient temperature - 4 cores interleaved (Staggered mode).

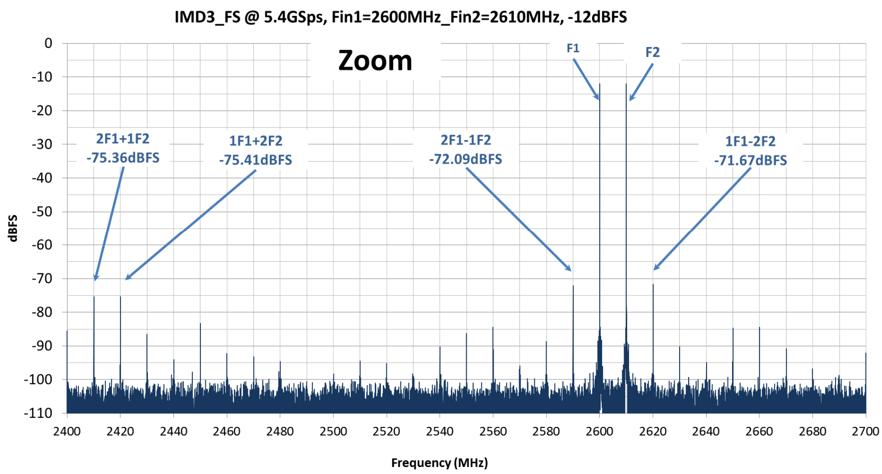
Figure 47. IMD3 at 5.4GSps Fin1 = 2600MHz, Fin2 = 2610 MHz, -12dBFS



Typical supplies - at ambient temperature - 4 cores interleaved (Staggered mode).



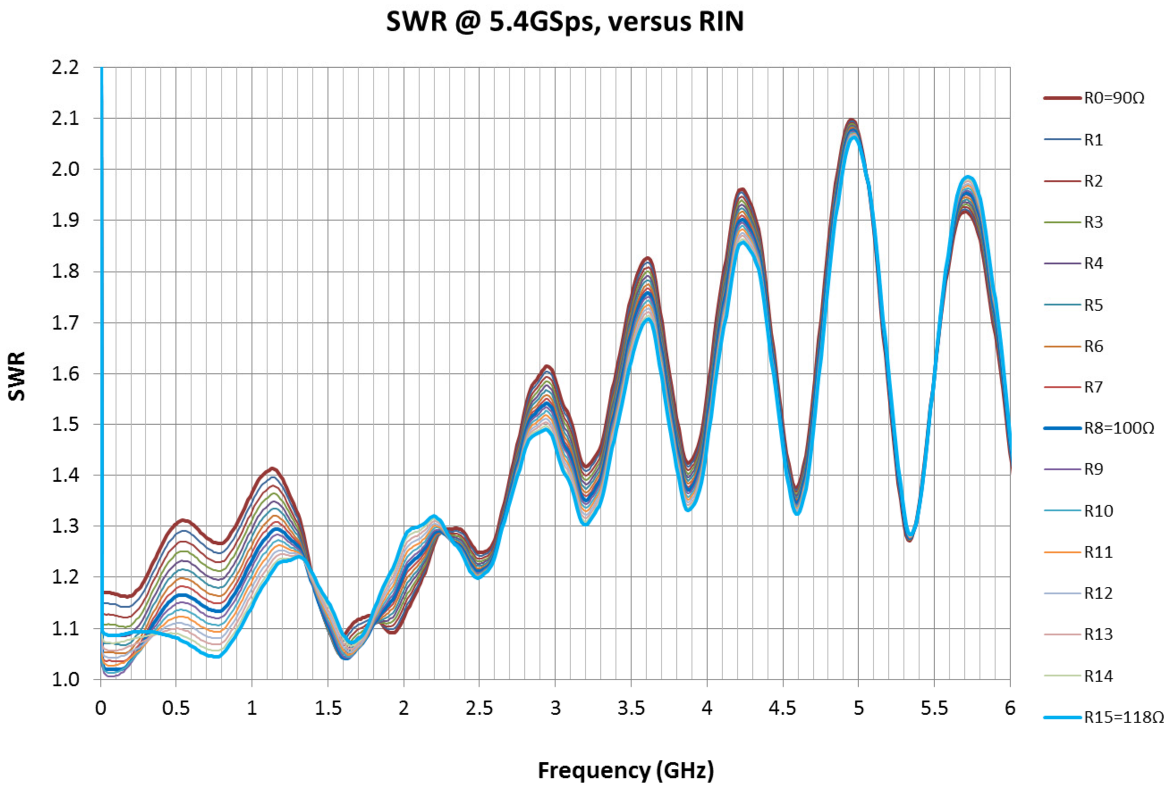
Typical supplies - at ambient temperature - 4 cores interleaved (Staggered mode).

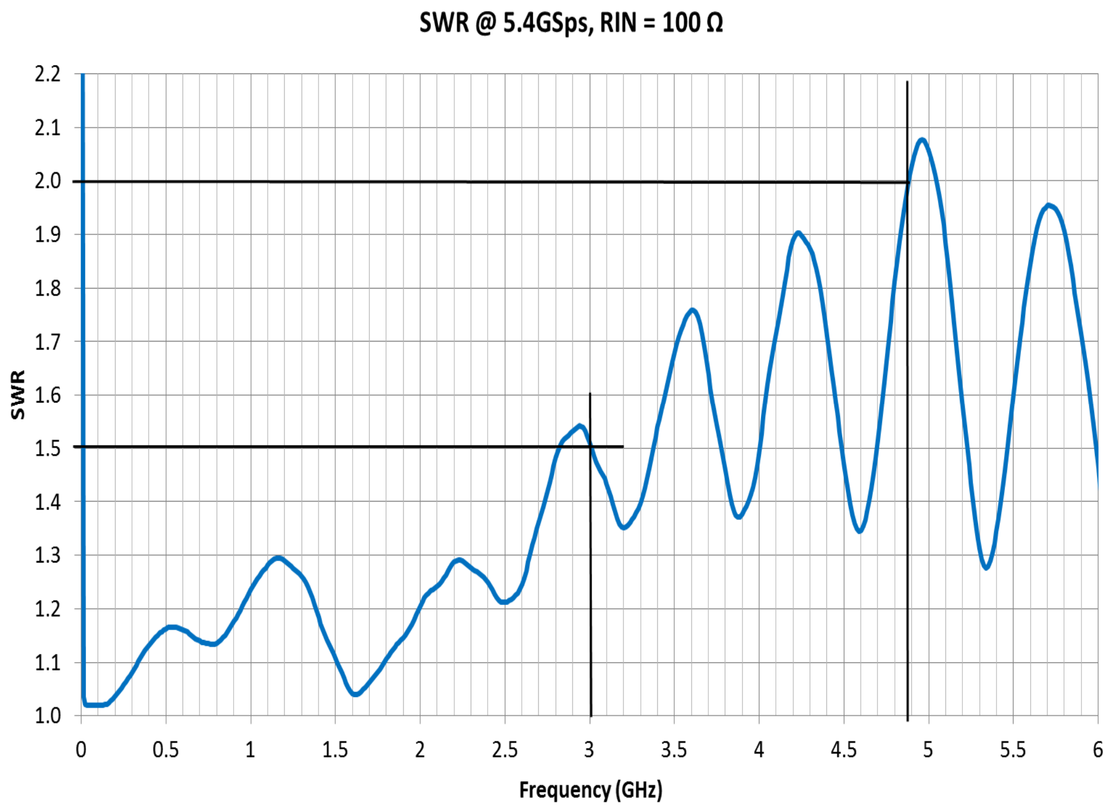


Typical supplies - at ambient temperature - 4 cores interleaved (Staggered mode).

6.8. VSWR

Figure 48. VSWR measurement on board with socket





6.9. FFT performance with ADX4 IP

Figure 49. ADC output spectrum with/without ADX4 IP: 5.4Gsps Fin=800MHz -1dBFS

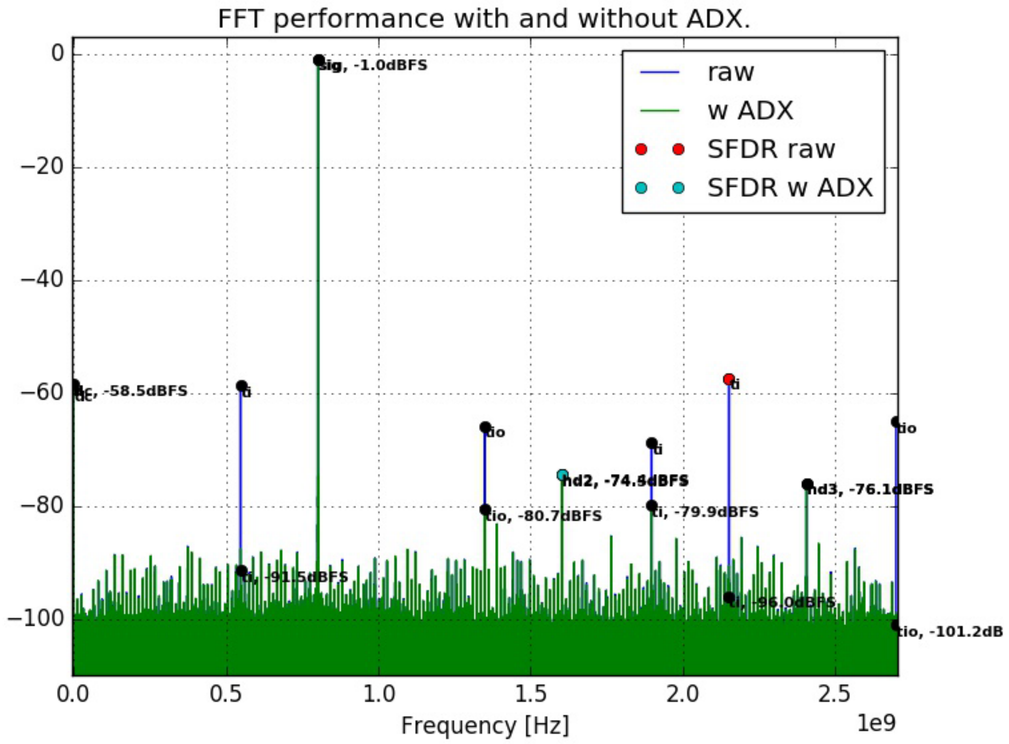
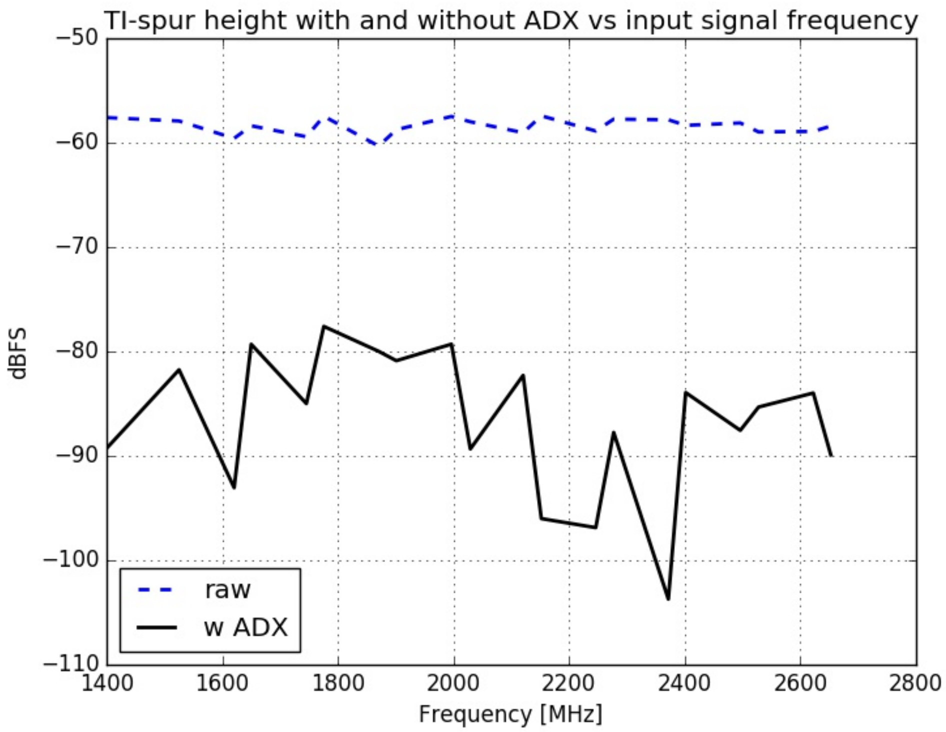


Figure 50. TI-spur height with and without ADX4 vs input signal frequency at 5.4Gsps

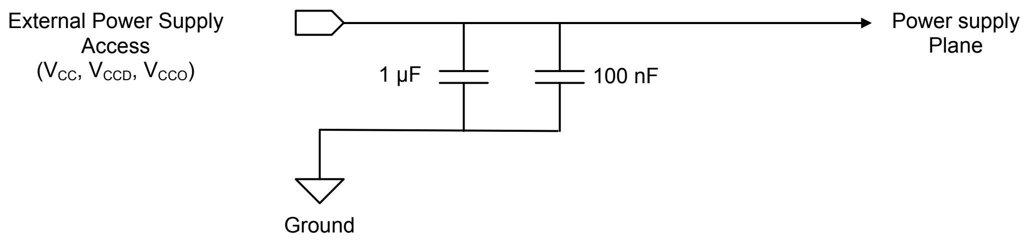


7 Application Information

7.1. Bypassing, decoupling and grounding

All power supplies have to be decoupled to ground as close as possible to the signal accesses to the board by 1 µF in parallel to 100 nF.

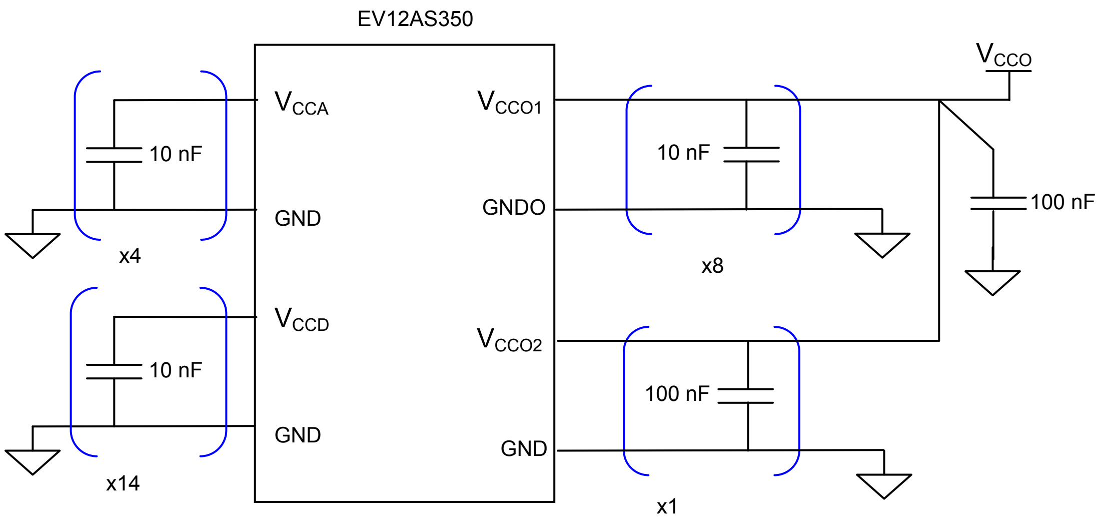
Figure 51. EV12AS350 Power supplies Decoupling and grounding Scheme



Note: GND and GNDO planes should be separated but the two power supplies must be reconnected by a strap on the board.

It is recommended to decouple all power supplies to ground as close as possible to the device balls with 10 nF capacitors for V_{CCA}, V_{CCD} and V_{CCO1} and 100 nF for V_{CCO2}. The minimum number of decoupling pairs of capacitors can be calculated as the minimum number of groups of neighboring pins as described in Figure 52 and Table 51.

Figure 52. EV12AS350 Power Supplies Bypassing recommended Scheme



The 100nF capacitor on V_{CCO} supply between V_{CCO1} and V_{CCO2} is intended to avoid any coupling of V_{CCO1} noise (output buffers) on V_{CCO2} (digital supply) and reciprocally.

Table 51. List of recommended neighboring pins for V_{CCA} decoupling (4 groups)

Decoupling (10nF)	V_{CCA}	GND
Group 1	Pins N24, M24	Pins L24, P24, N23, M23
Group 2	Pins N22, M22	Pins N21, M21
Group 3	Pins M3, N3	Pins N4, M4
Group 4	Pins M1, N1	Pins P1, N2, M2, L1

Table 52. List of recommended neighboring pins for V_{CCD} decoupling (14 groups)

Decoupling (10 nF)	V_{CCD}	GND
Group 1	Pins A2, B2, C3, D3	Pins A1, B1, C4, D4
Group 2	Pins C5, C6, D6, D7, E7	Pins A6, B6, B7, C7, C8, D8, E8
Group 3	Pins K5, M5, L5	Pins J5, L4
Group 4	Pins N5, P5, R5	Pins P4, T5
Group 5	Pins AA3, AB3, AC2, AD2	Pins AD1, AC1, AB4, AA4
Group 6	Pins AA6, AA7, Y7, AB5, AB7	Pins AB6, AC6, AD6, AA8, Y8
Group 7	Pins Y10, Y11, AA10, AA11, AB10, AB11	Pins Y9, Y12, AA9, AA12
Group 8	Pins AA14, AA15, AB14, AB15, Y14, Y15	Pins Y13, Y16, AA13, AA16, AB16
Group 9	Pins Y18, AA18, AA19, AB18, AB20	Pins AB19, AA17, Y17
Group 10	Pins AD23, AC23, AB22, AA22	Pins AA21, AB21, AC24, AD24
Group 11	Pins R20, P20, N20	Pins T20, P21
Group 12	Pins M20, L20, K20	Pins J20, L21
Group 13	Pins A23, B23, C22, D22	Pins D21, C21, B24, A24
Group 14	Pins C19, C20, D18, D19, E18	Pins A19, B19, B18, C18, C17, D17, E17

Table 53. List of recommended neighboring pins for V_{CCO1} decoupling (8 groups)

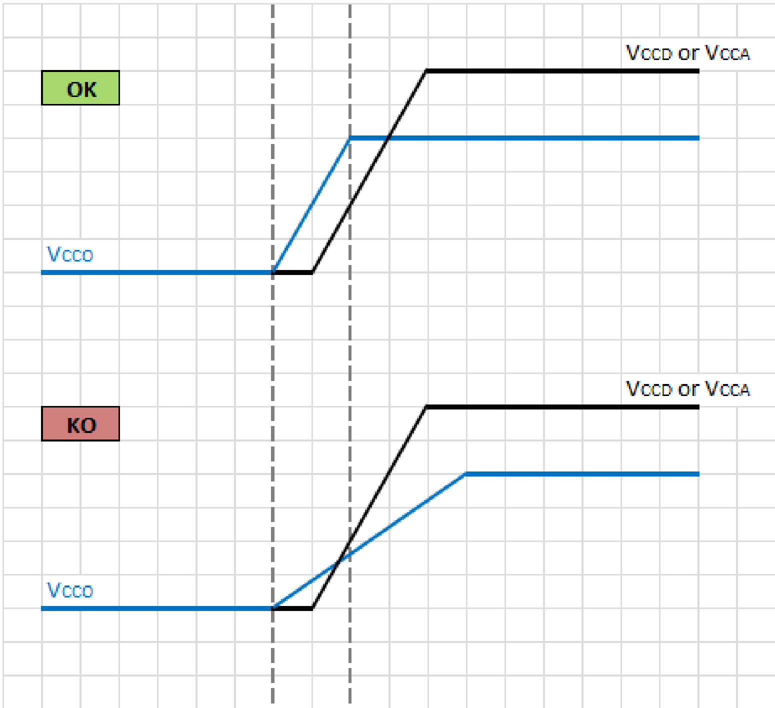
Decoupling (10 nF)	V_{CCO1}	GNDO
Group 1	Pins F22, E22	Pins E21, F21
Group 2	Pins H20, E19, D20	Pins G20, F20, E20
Group 3	Pins W22, Y22	Pins Y21, W21
Group 4	Pins AA20, Y19, U20	Pins Y20, W20, V20
Group 5	Pins Y3, W3	Pins W4, Y4
Group 6	Pins AA5, Y6, U5	Pins Y5, W5, V5
Group 7	Pins H5, E6, D5	Pins G5, F5, E5
Group 8	Pins F3, E3	Pins F4, E4

Table 54. List of recommended neighboring pins for V_{CCO2} decoupling (1 group)

Decoupling (100 nF)	V_{CCO2}	GND
Group 1	Pins AC18, AD18	Pins AC19, AD19

7.2. Power-up sequencing

Figure 53. EV12AS350 Power–up sequencing

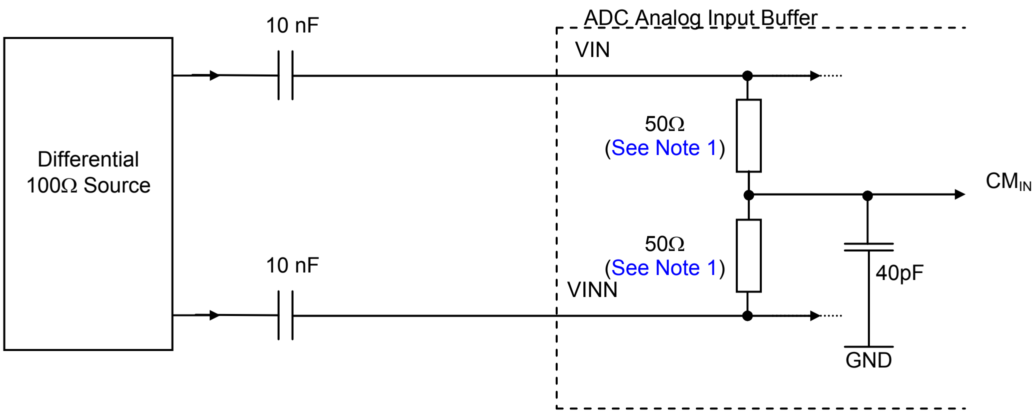


The device always starts properly when V_{CCO} is switched on first and is never overrun by the 2 other power supplies before its establishment. Once V_{CCO} has reached its steady state value, there is no constraint on V_{CCA} and V_{CCD} power-up.

7.3. Analog Inputs (VIN/VINN)

The analog input can be either DC or AC coupled as described in Figure 54 and Figure 55.

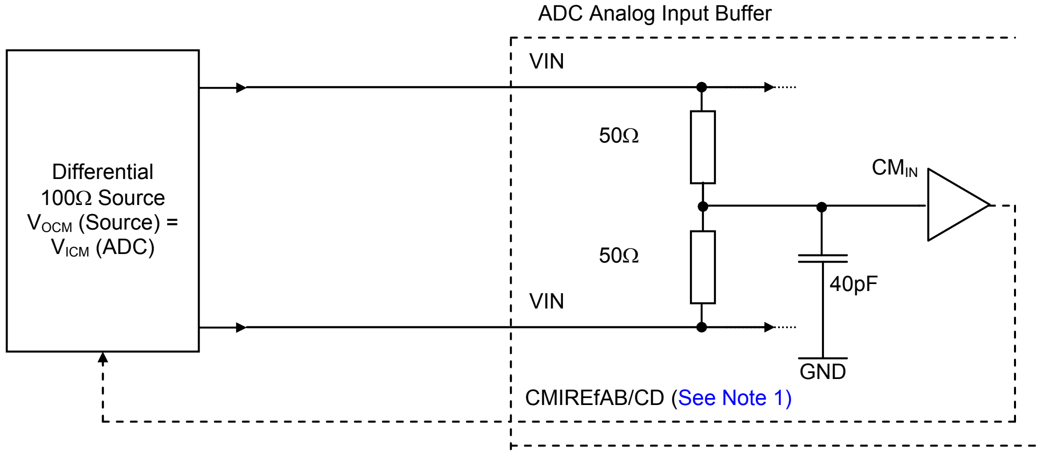
Figure 54. Differential analog input implementation (AC coupled)



Notes:

1. The 50Ω terminations are on chip.
2. CM_{IN} value is given in Table 3.

Figure 55. Differential analog input implementation (DC coupled)



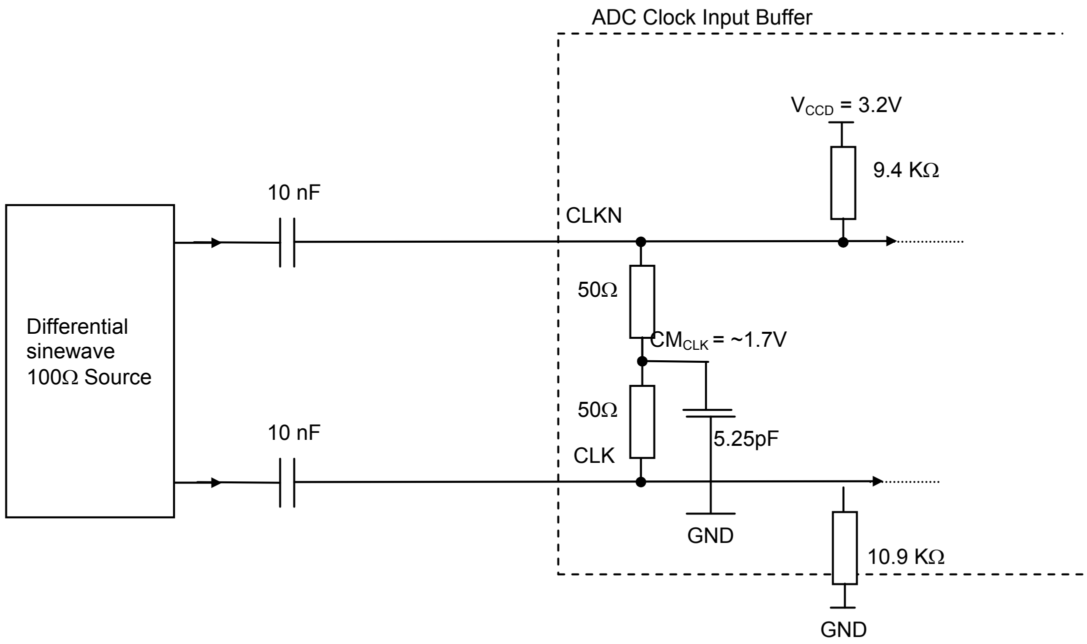
Notes:

1. CMIRefAB/CD value is given in Table 3.

7.4. Clock Inputs (CLK/CLKN)

It is recommended to enter the clock input signal in differential mode. Since the clock input common mode is around 1.7V, it is recommended to AC couple the input clock as described below.

Figure 56. Differential clock input implementation (AC coupled)

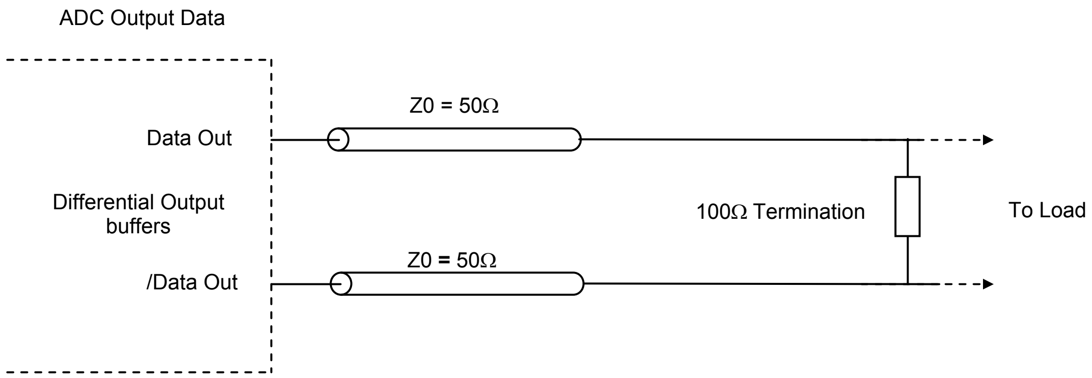


Differential mode is the recommended input scheme.
Single ended input is not allowed due to performance limitations.

7.5. Digital Outputs

The digital outputs are LVDS compatible (Output Data, Parity Bit, In Range bit and Data Ready). They have to be 100Ω differentially terminated.

Figure 57. Differential digital outputs Terminations (100Ω LVDS)

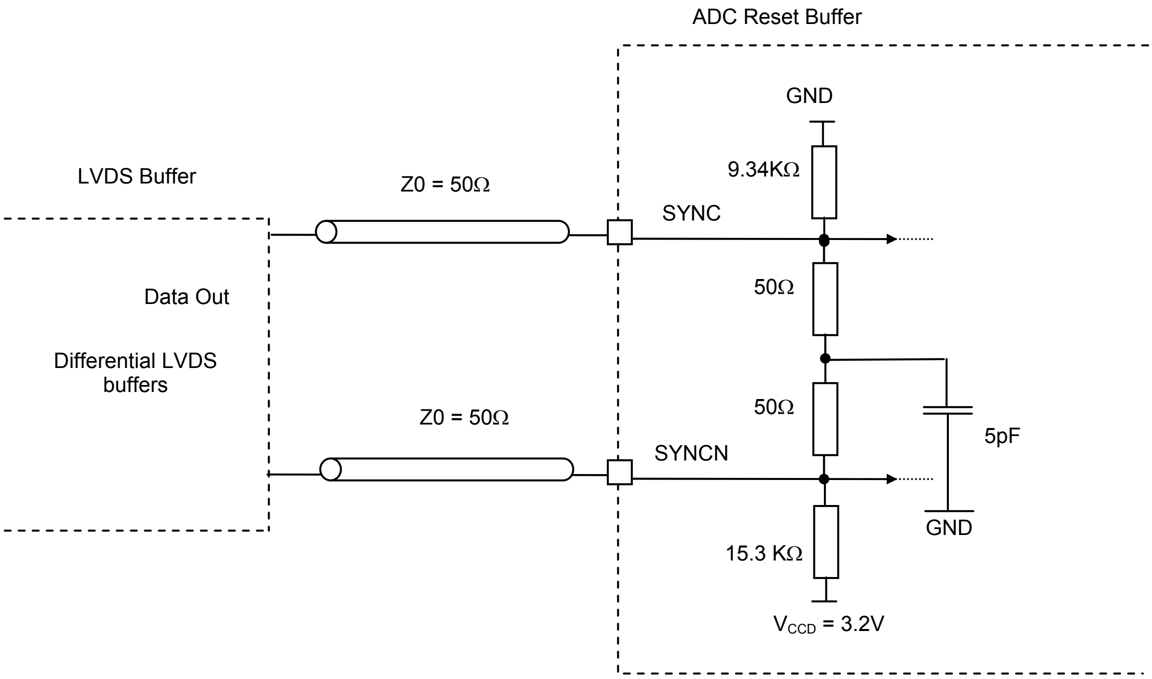


Each Digital output should always be terminated by 100Ω differential resistor placed as close as possible to differential receiver.
Note: If not used, leave the pins of the differential pair open.

7.6. Reset Buffer (SYNC, SYNCN)

The SYNC, SYNCN signal has LVDS electrical characteristics.

Figure 58. Reset Buffer (SYNC, SYNCN)



Note: If not used, leave the pins of the differential pair open

7.7. Procedure for synchronisation with FPGA

RSTN 10 µs minimum (active low state)

FLASH_LENGTH & RESET_LENGTH programming:
Write @01 0004 # Register : CHANNEL_SEL (all channels selected)
Write @66 00xx # Register : RESET_LENGTH (Duration of DataReady frozen to low level)
Write @69 00xx # Register : FLASH_LENGTH

Write @5D 0001 # TEST_MODE enabled

SYNC PULSE 10 ns minimum (active high state)
SYNC/SYNCN signal causes a stop of DataReady (see SYNC TIMING diagram on Figure 21), duration of stop is programmed in the RESET_LENGTH register. The 4 channels are now synchronous.

FLASH MODE & RAMP MODE:
Write @5D 000D # FLASH mode / ADC output is a flash pattern
Write @5D 0009 # RAMP mode / ADC output is now a ramp

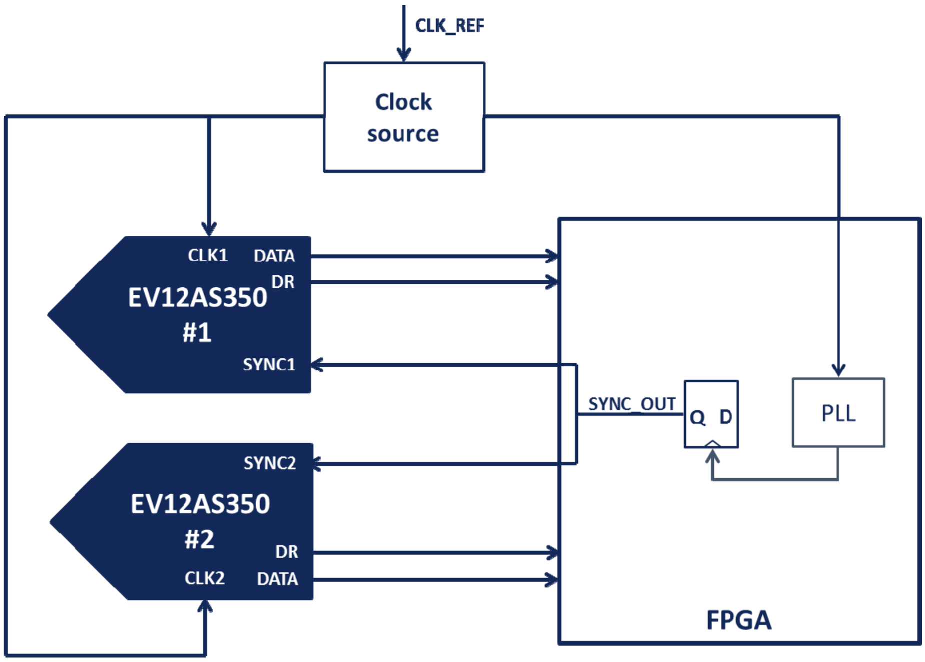
Return to functional mode:
Write @5D 0000 # TEST_MODE disabled / ADC output is in functional mode

7.8. Synchronization in multi-ADC application

For applications requiring multiple ADCs synchronization, the starting and the output data order has to be deterministic. For more details about deterministic behavior using synchronous SYNC signal, please refer to section 5.7.1. Figure 59 shows a simplified schematic of two ADCs using a synchronous SYNC signal.

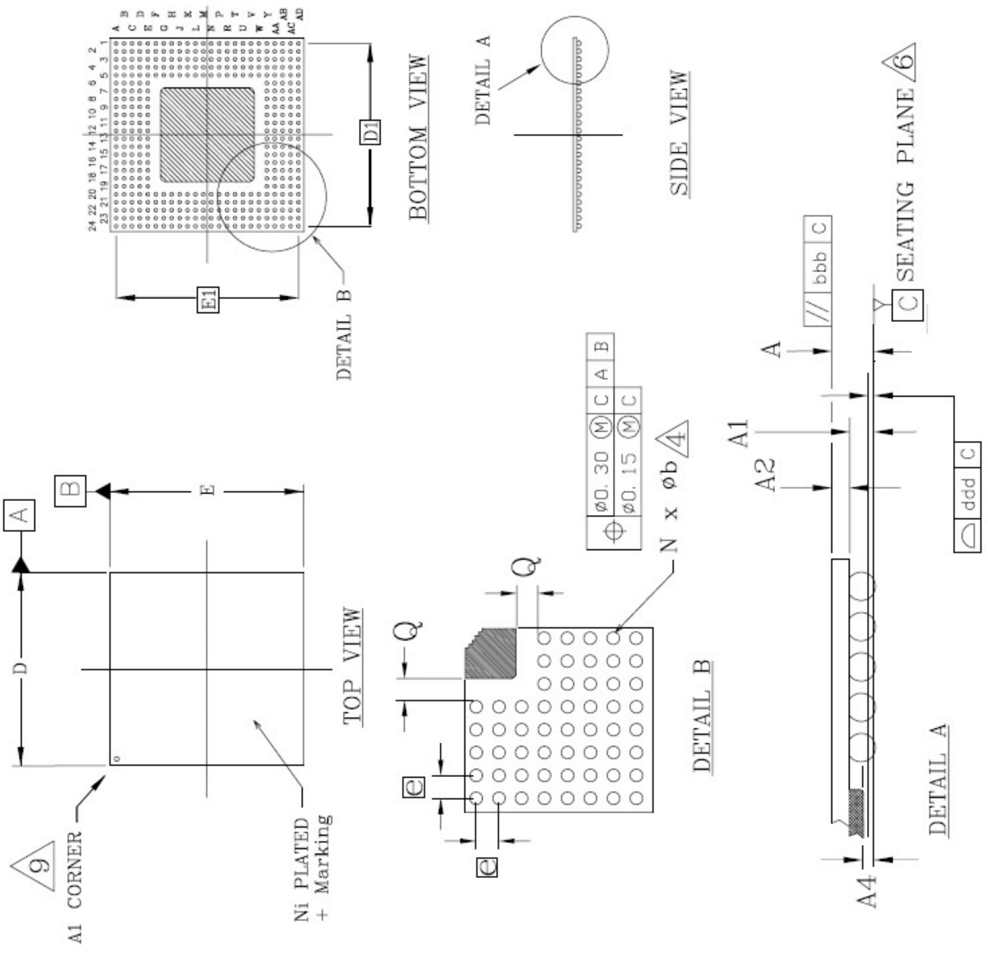
In case of synchronous sampling for both channels, CLK1 and CLK2 must be aligned at their respective ADC input. In case of interleaved channels to reach a sampling speed up to 10.8 GSps, CLK1 and CLK2 must have a phase delay of 180° at their respective ADC input.
The SYNC_OUT signal should be generated through a clock that has the same reference as the sampling clock input to the AD (for example a division by 16 or 32 of CLK1 (or CLK2)).
The SYNC_OUT to SYNC1 and SYNC_OUT to SYNC2 should have the same propagation time in case of synchronous channels. They should have a propagation time delay of half a CLK1 (or CLK2) period in case of interleaved channels.
To avoid metastable zone at the SYNC inputs of the ADCs (see section 3.6.3.), configurable delay can be added at SYNC output of the FPGA to shift the time of arrival of the SYNC signal at the ADCs inputs.

Figure 59. Example of multi-ADC synchronization using synchronous SYNC signals with 2 synchronous EV12AS350 ADCs



8 Package Information

8.1. Package outline

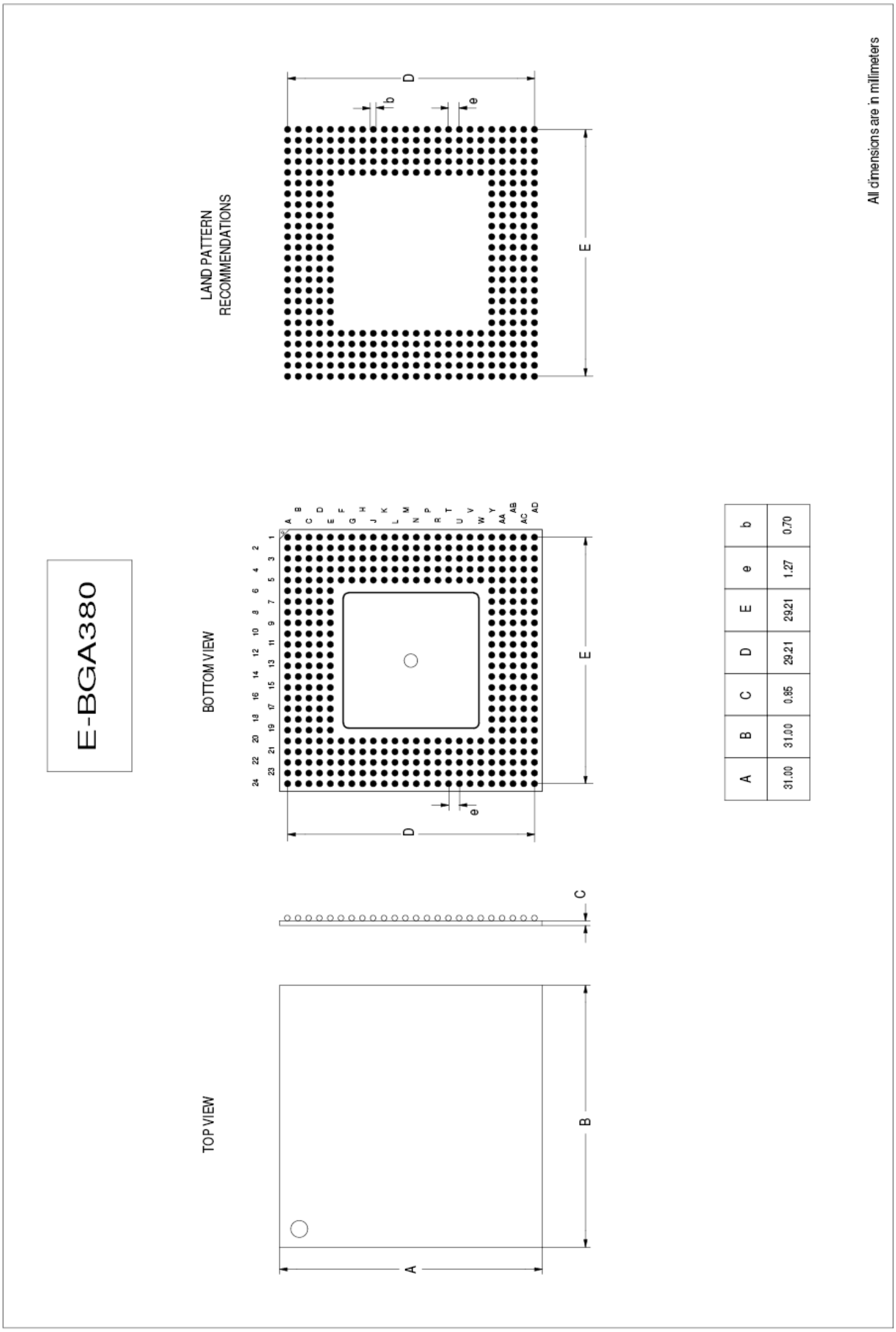


DIMENSIONAL REFERENCES			
REF.	MIN.	NOM.	MAX.
A	1.25	1.45	1.60
A1	0.50	0.60	0.70
D	30.80	31.00	31.20
D1	29.21 (BSC.)		
E	30.80	31.00	31.20
E1	29.21 (BSC.)		
b	0.70	0.80	0.90
A2	0.75	0.85	0.95
M	24		
N	380		
bbb			0.25
ddd			0.20
e	1.27 TYP.		
A4	0.15		
Q	1.1		
REF: JEDEC MS-034B VARIATION BAK-1			

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. "e" REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
3. "M" REPRESENTS THE BASIC SOLDER BALL MATRIX SIZE, AND SYMBOL "N" IS THE MAXIMUM ALLOWABLE NUMBER OF BALLS AFTER DEPOPULATING.
4. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM C.
5. DIMENSION "ddd" IS MEASURED PARALLEL TO PRIMARY DATUM C.
6. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
7. PACKAGE SURFACE SHALL BE Ni PLATED.
8. ENCAPSULANT SIZE MAY VARY WITH DIE SIZE.
9. SMALL ROUND DEPRESSION FOR PIN 1 IDENTIFICATION.
10. "A4" IS MEASURED AT THE EDGE OF ENCAPSULANT TO THE INNER EDGE OF BALL PAD.
11. DIMENSIONING AND TOLERANCING PER ASME Y14.5 1994
12. THIS DRAWING IS FOR QUALIFICATION PURPOSE ONLY.

8.2. EBGA380 Land Pattern Recommendations



A	B	C	D	E	e	b
31.00	31.00	0.85	29.21	29.21	1.27	0.70

8.3. Thermal Characteristics

Table 55. Thermal characteristics

Parameter	Symbol	Value	Unit	Note
Thermal resistance from junction to bottom of balls	$Rth_{\text{Junction to Bottom of balls}}$	6.8	°C/Watt	(1)(2)
Thermal resistance from junction to board (JEDEC JESD51-8)	$Rth_{\text{junction - board}}$	7.5	°C/Watt	(1)(2)
Thermal resistance from junction to top of case	$Rth_{\text{Junction – case}}$	4.42	°C/Watt	(1)(2)
Thermal resistance from junction to ambient (JEDEC standard)	$Rth_{\text{Junction – amb}}$	16.4	°C/Watt	(1)(3)
Delta temperature Hot spot – Temperature of diode		+7	°C	

Note
1. Rth are calculated at diode, not from average temperature of the die
   These figures are thermal simulation results (finite elements method) with nominal cases.
2. Assumptions : no air, pure conduction, no radiation
3. Assumptions:
   - Convection according to JEDEC
   - Still air
   - Horizontal 2s2p board
   - Board size 114.3 x 101.6 mm, 1.6 mm thickness

It is important to consider a heatspreader leading to a uniform dissipation on the whole surface of the package so that temperature of each quarter of the package remains as much as possible similar. Any temperature gradient on package is to be avoided. Without it, 4 ADC cores will not be at the same temperature and level of interleaving spurs may increase.

8.4. Moisture Characteristics

This device is sensitive to the moisture (MSL3 according to JEDEC standard).
Shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH).
After this bag is opened, devices that will be subjected to infrared reflow, vapor-phase reflow, or equivalent processing (peak package body temp. 220°C) must be:

- mounted within 168 hours at factory conditions of ≤30°C/60% RH, or
- stored at ≤10% RH

Devices require baking, before mounting, if Humidity Indicator is >20% when read at 23°C ± 5°C.
If baking is required, devices may be baked for:

- 13 days at 40°C + 5°C/-0°C and <5% RH for low temperature device containers, or
- 9 hours at 125°C ± 5°C for high-temperature device containers.

9 Ordering information

Table 56. Component Ordering information

<table>
<tr><th>Part Number</th><th>Package</th><th>Temperature Range</th><th>Screening Level</th><th>Comments</th></tr>
<tr><td>EVP12AS350TPY-V4</td><td>EBGA380 RoHS</td><td>Ambient</td><td>Beta Prototype</td><td>Contact sales for availability</td></tr>
<tr><td>EVX12AS350BTP</td><td>EBGA380</td><td>Ambient</td><td>Final Prototype</td><td>Contact sales for availability</td></tr>
<tr><td>EVX12AS350BTPY</td><td>EBGA380 RoHS</td><td>Ambient</td><td>Final Prototype</td><td>Contact sales for availability</td></tr>
<tr><td>EV12AS350BCTP</td><td>EBGA380</td><td>0°C < Tc, Tj < 100°C</td><td>Commercial “C” Grade</td><td>Pending availability</td></tr>
<tr><td>EV12AS350BVTP</td><td>EBGA380</td><td>-40°C < Tc, Tj < 125°C</td><td>Industrial “V” Grade</td><td>Pending availability</td></tr>
<tr><td>EV12AS350BCTPY</td><td>EBGA380 RoHS</td><td>0°C < Tc, Tj < 100°C</td><td>Commercial “C” Grade</td><td>Pending availability</td></tr>
<tr><td>EV12AS350BVTPY</td><td>EBGA380 RoHS</td><td>-40°C < Tc, Tj < 125°C</td><td>Industrial “V” Grade</td><td>Pending availability</td></tr>
<tr><td>EV12AS350BCTPX4 variants</td><td>EBGA380</td><td>0°C < Tc, Tj < 100°C</td><td>Commercial “C” Grade</td><td rowspan="4">These P/N include ADX4 software licenses. They are customer specific part numbers</td></tr>
<tr><td>EV12AS350BVTPX4 variants</td><td>EBGA380</td><td>-40°C < Tc, Tj < 125°C</td><td>Industrial “V” Grade</td></tr>
<tr><td>EV12AS350BCTPYX4 variants</td><td>EBGA380 RoHS</td><td>0°C < Tc, Tj < 100°C</td><td>Commercial “C” Grade</td></tr>
<tr><td>EV12AS350BVTPYX4 variants</td><td>EBGA380 RoHS</td><td>-40°C < Tc, Tj < 125°C</td><td>Industrial “V” Grade</td></tr>
</table>

Table 57. Board Ordering information

Part Number	Package	Temperature Range	Screening Level	Comments
EV12AS350BTPY-EB	EBGA380 RoHS	Ambient	Prototype	EV12AS350 Evaluation Board
EV12AS350B-ADX4EVM	EBGA380 RoHS	Ambient	Prototype	EV12AS350 Evaluation module pre-loaded with ADX4 and ADGLITCH.

10 Document revision history

This table provides revision history for this document.

Table 58. Revision history

Rev. No	Date	Substantive change(s)
1209A	September 2018	Initial revision for EV12AS350B
1209B	October 2018	§9 Ordering information updated

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