CCD47-10 NIMO Back Illuminated Compact Pack
High Performance CCD Sensor

FEATURES

- 1024 by 1024 Nominal (1056 by 1027 Usable Pixels)
- Image area 13.3 x 13.3mm
- Back Illuminated format for high quantum efficiency
- Full-Frame Operation
- 13µm Square Pixels
- Symmetrical anti-static gate protection
- Very low noise output amplifiers
- Gated Dump Drain on Output Register
- 100% Active area
- New Compact Footprint Package

APPLICATIONS

- Spectroscopy
- Scientific Imaging
- Star Tracking
- Medical Imaging

INTRODUCTION

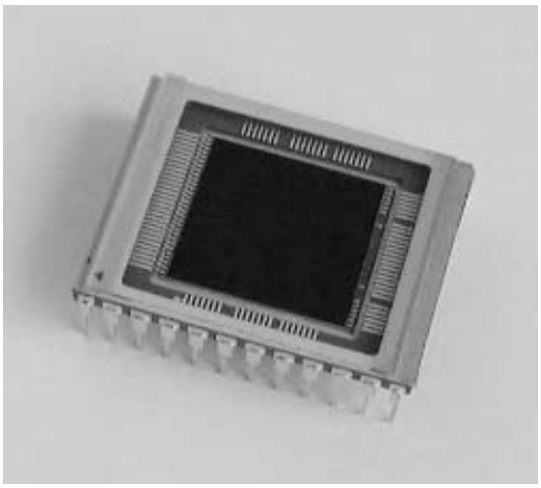
This version of the CCD47 family of CCD sensors has full-frame architecture. Back illumination technology, in combination with extremely low noise amplifiers, makes the device well suited to the most demanding scientific applications. To improve the sensitivity further, the CCD is manufactured without anti-blooming structures.

The device has a single serial output register. Separate charge detection circuits are incorporated at each end of the register, which is split so that a line of charge can be transferred to either output, or split between the two.

The register is provided with a drain and control gate along the outer edge of the channel for charge dump purposes.

Other variants of the CCD47-10 available are front illuminated format and inverted mode (MPP). In common with all e2v technologies CCD Sensors, the CCD47-10 is also available with a fibre-optic window or taper, or with a phosphor coating.

Designers are advised to consult e2v technologies should they be considering using CCD sensors in abnormal environments or if they require customised packaging.



TYPICAL PERFORMANCE

(Low noise mode)

Pixel readout frequency	5 MHz
Output amplifier sensitivity	4.5 µV/e^-
Peak signal	120 ke^-/pixel
Dynamic range @ 20 kHz	50000:1
Spectral range	200–1100 nm
Readout noise @ 20 kHz	2.0 e^- rms

GENERAL DATA

Format

Image area	13.3 x 13.3 mm
Active pixels	1056 (H) x 1027 (V)
Pixel size	13 x 13µm
Number of output amplifiers	2
Weight (approx., no window)	6g

Package

Package size	22.6 x 29.9 mm
Number of pins	24
Inter-pin spacing	2.54 mm
Window material	Quartz or Removable glass
Package type	Ceramic DIL array

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PERFORMANCE AT 243 K (–30 °C) UNLESS STATED OTHERWISE

		Min	Typical	Max	Units	Note
Peak charge storage		-	120,000	-	e^-/pixel	1
Peak output voltage (unbinned)		-	540	-	mV	1
Dark signal at 293 K	Standard Silicon	-	20,000	40,000	e^-/pixel/s	2, 3
	Deep Depleted Silicon		43,000	85,000		
Dynamic Range		-	50,000	-	-	4
Charge transfer efficiency	Parallel	-	99.9999	-	%	5
	Serial	-	99.9993	-	%	
Output amplifier responsivity	Low noise mode	3	4.5	6	$\mu V/e^-$	
Readout noise	Low noise mode	-	2	4	rms e^-	6
Maximum readout frequency		-	5.0	-	MHz	7
Dark signal non-uniformity at 293 K (std. deviation)	Standard Silicon	-	1000	2000	e^-/pixel/s	3, 8
	Deep Depleted Silicon		4300	8500		
Response non-uniformity (std. deviation)		--	3	10	%	

SPECTRAL RESPONSE AT 243 K (–30 °C)

Standard Silicon

Wavelength (nm)	Minimum Response (QE)			Maximum Response Non-uniformity (1σ)	
	Enhanced Process UV Coated	Basic Process Mid-band Coated	Basic Process Broadband Coated		
300	45	-	-		%
350	45	15	25	-	%
400	55	40	55	3	%
500	60	85	75	-	%
650	60	85	75	3	%
900(1)	30	30	30	5	%

(1) For Shielded Anti-Blooming (SAB) variants the minimum response at 900nm is reduced to 24%

Deep Depleted Silicon

Wavelength (nm)	Minimum Response (QE)			Maximum Response Non-uniformity (1σ)	
	Basic Process NIR Coated	Enhanced Process Multilayer 2 Coated	Basic Process Uncoated		
350	15	30	10	-	%
400	30	75	25	3	%
500	50	75	50	-	%
650	75	80	55	3	%
900	65	65	40	5	%

ELECTRICAL INTERFACE CHARACTERISTICS

Electrode Capacitances (Measured at mid-clock level)

	Min	Typical	Max	
I∅/I∅ interphase	-	1.5	-	nF
I∅/SS	-	5	-	nF
R∅/R∅ interphase	-	40	-	pF
R∅//SS		60		pF
R∅/(SS + DG + OD)	-	10	-	pF
Output impedance at typical operating conditions	-	300	-	Ω

NOTES

1. Signal level at which resolution begins to degrade. The typical values are those expected from design. Not measured as a production test.
2. The typical average (background) dark signal at any temperature T (kelvin) between 233 K and 293 K and V_{SS} + 9.5V may be estimated from:

   $Q_d/Q_{d0} = 122T^3e^{-6400/T}$

   Where Q_{d0} is the dark signal at 293 K.
3. Test carried out at 243 K and scaled to 293 K using the formula in note 2.
4. Dynamic range is the ratio of full-well capacity to readout noise.
5. CCD characterisation measurement using charge generated by X-ray photons of known energy. Not measured as a production test.
6. Measured at a pixel readout frequency of 18 KHz using a dual-slope integrator technique (i.e. correlated double sampling).
7. Readout above 5 MHz into a 15pF load can be achieved but performance to the parameters given cannot be guaranteed.
8. Excluding white defects.

BLEMISH SPECIFICATION

Traps Pixels where charge is temporarily held. Traps are counted if they have a capacity greater than 200 e^- at 243 K.

Black spots Are counted when they have a signal level of less than 80% of the local mean at a signal level of approximately half full-well at 243K.

White spots Are counted when they have a generation rate 20 times the specified maximum dark signal generation rate (measured at 243 K). The typical temperature dependence of white spot blemishes is the same as that of the average dark signal i.e.:

$$Q_d/Q_{d0} = 122T^3e^{-6400/T}$$

Column defects A column which contains at least 21 white or 21 black defects.

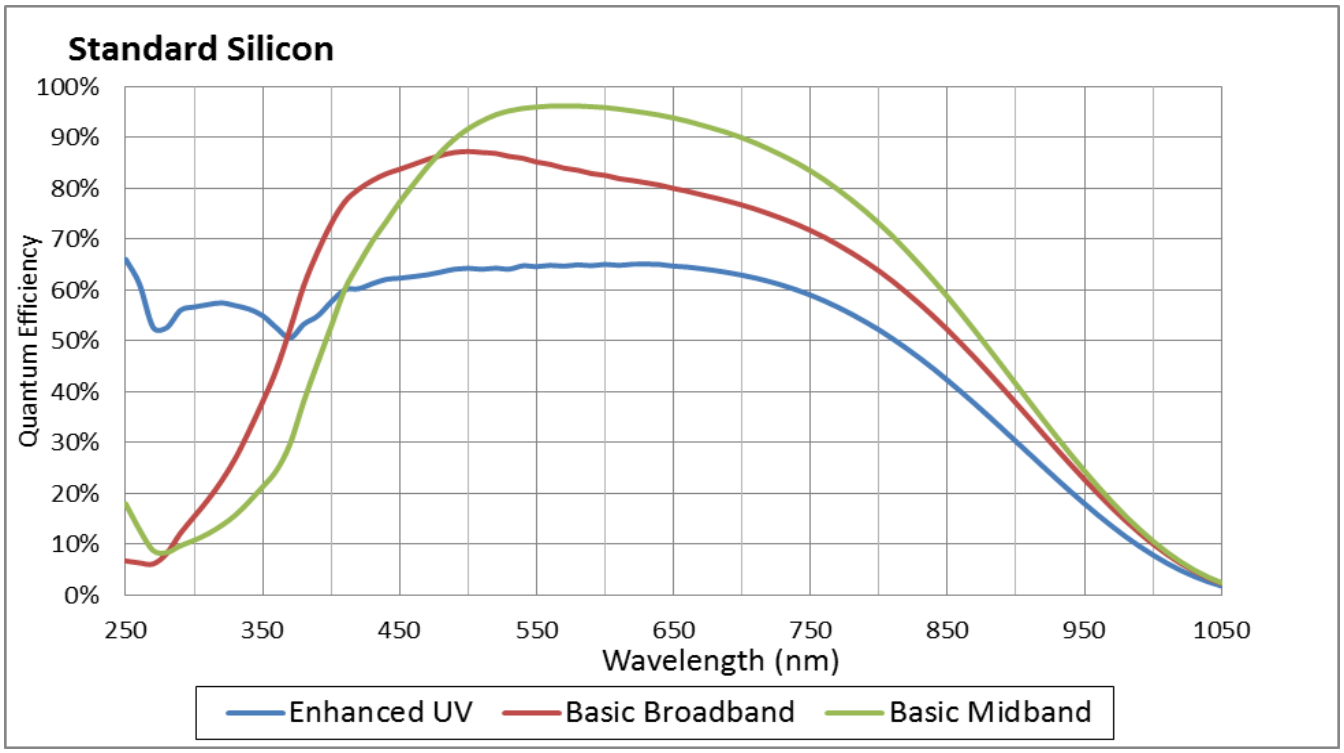
GRADE	**0**	**1**	**2**
Column defects; black or white	0	2	6
White	0	0	2
Black spots	50	100	200
Traps >200 e^-	2	5	12
White spots	50	80	100

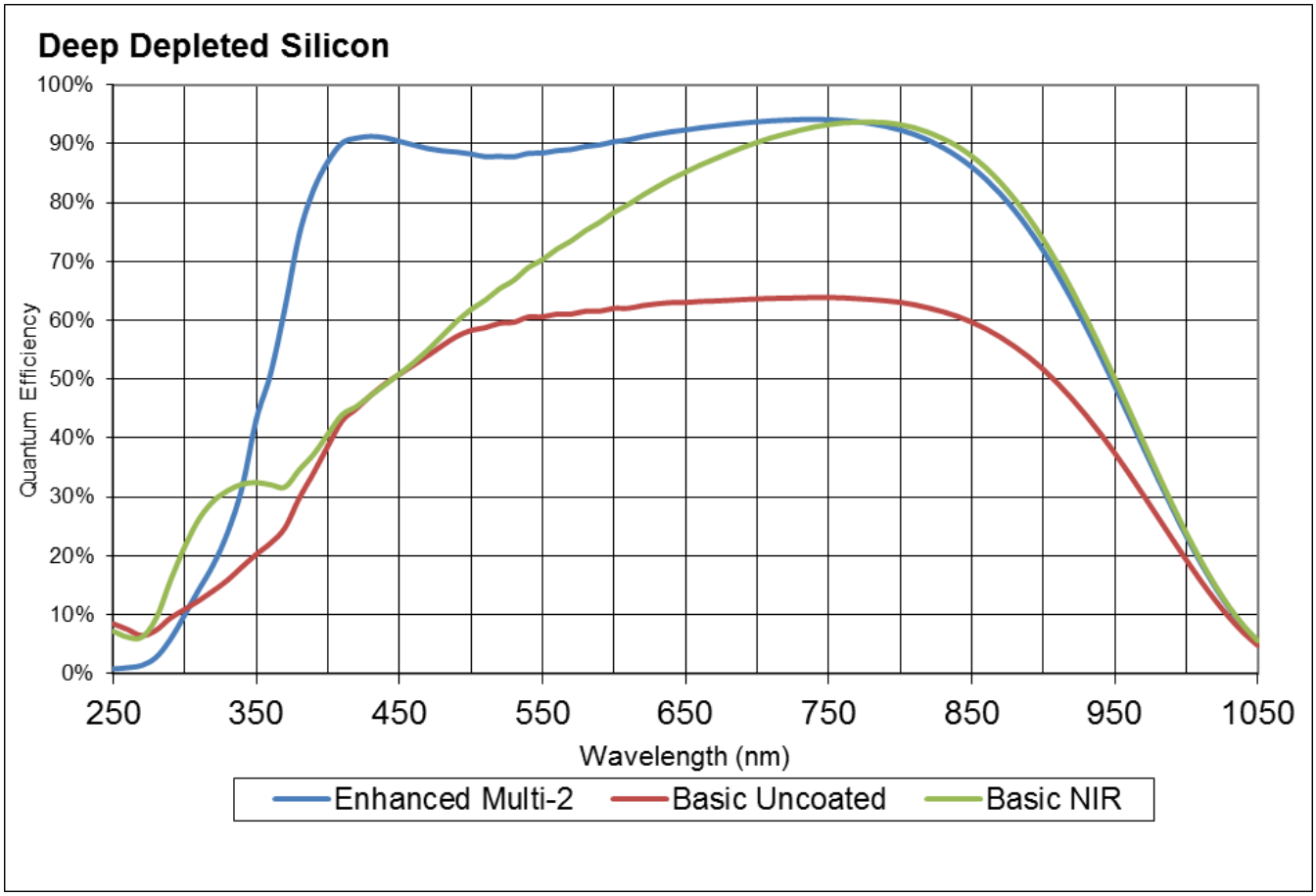
Grade 5 Devices which are fully functional, with image quality below that of grade 2, and which may not meet all other performance parameters.

Minimum separation between adjacent black columns – 50 Pixels

Note: The effect of temperature on defects is that traps will be observed less at higher temperatures but more may appear below 233 K. The amplitude of white spots and columns will decrease rapidly with temperature.

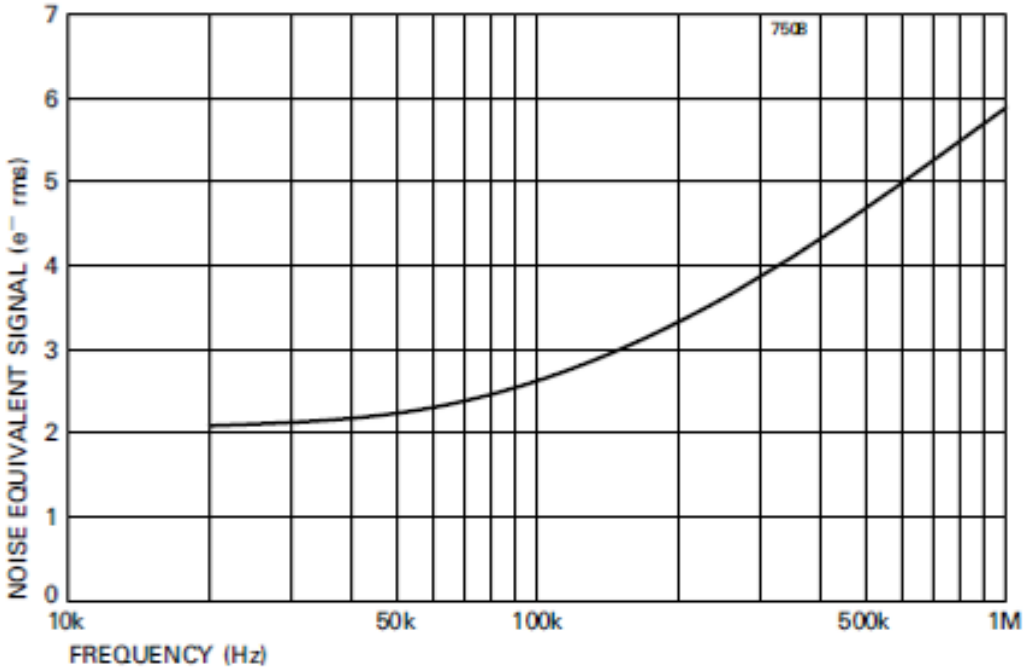
TYPICAL SPECTRAL RESPONSE (At –30 °C)



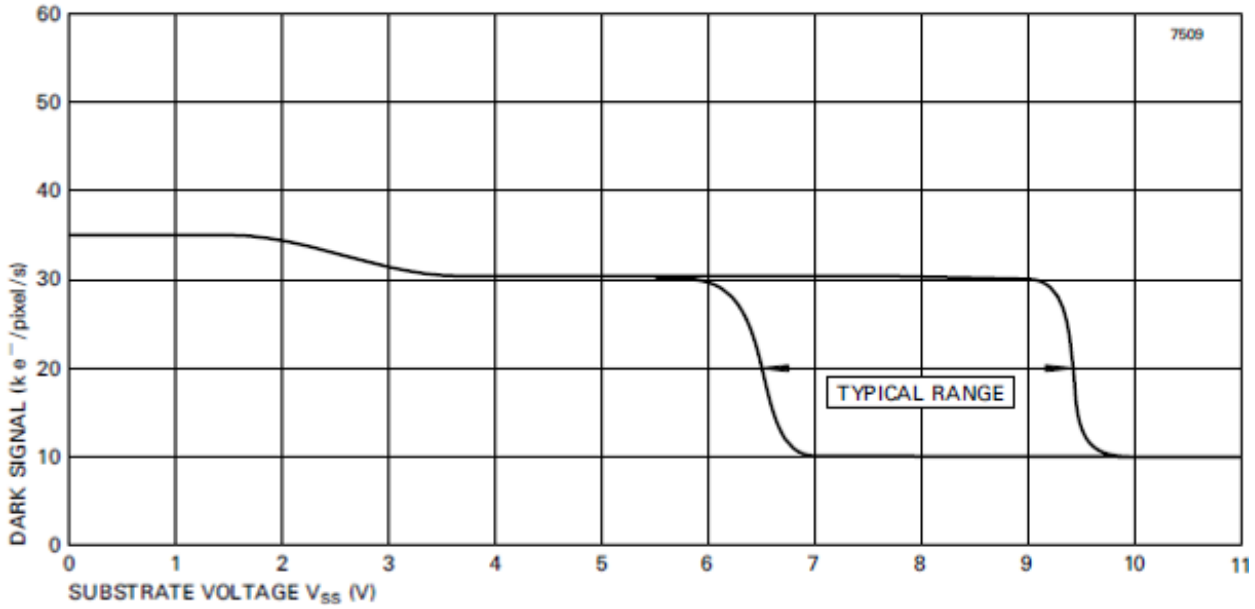


TYPICAL OUTPUT CIRCUIT NOISE (If Measured using clamp and sample)

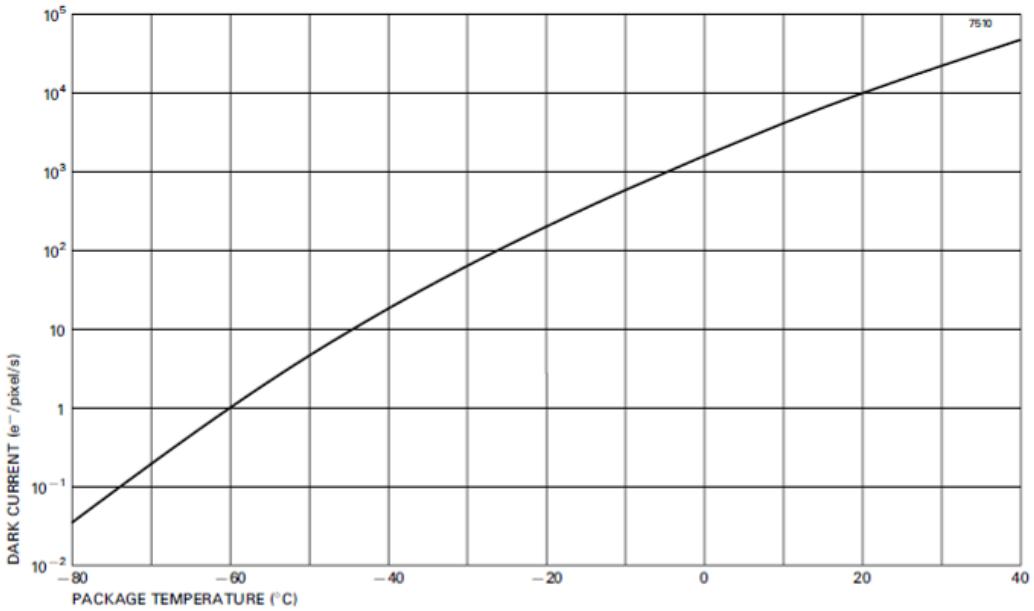
V_{SS} = 9.5 V V_{RD} = 17 V V_{OD} = 29 V



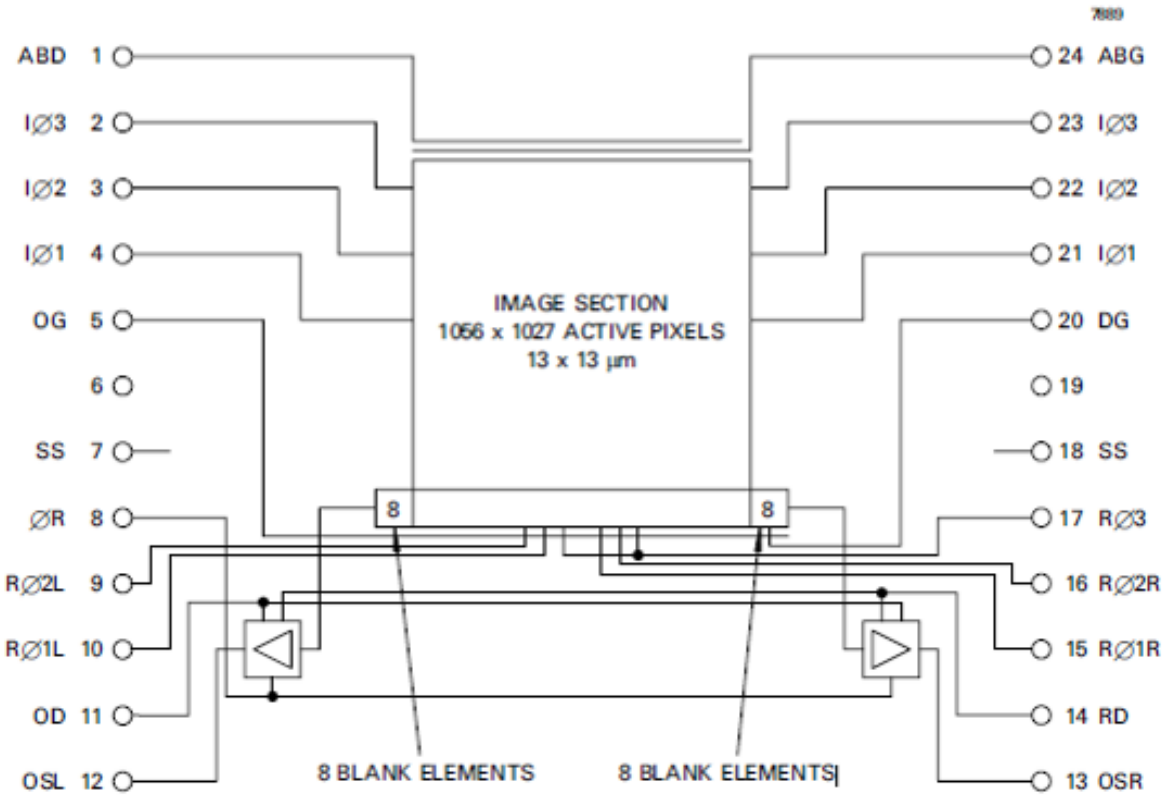
TYPICAL VARIATION OF DARK CURRENT WITH SUBSTRATE VOLTAGE



TYPICAL VARIATION OF DARK SIGNAL WITH TEMPERATURE



DEVICE SCHEMATIC



Note Pins 6 and 19 are not connected. For convenience, the CCD47-10 Compact Pack is pin compatible with the e2v technologies CCD57 sensors in the compact pack, except that OSL = pin 6, OSR = pin 19 and pins 12 and 13 are not connected in the CCD57.

CONNECTIONS, TYPICAL VOLTAGES AND ABSOLUTE MAXIMUM RATINGS

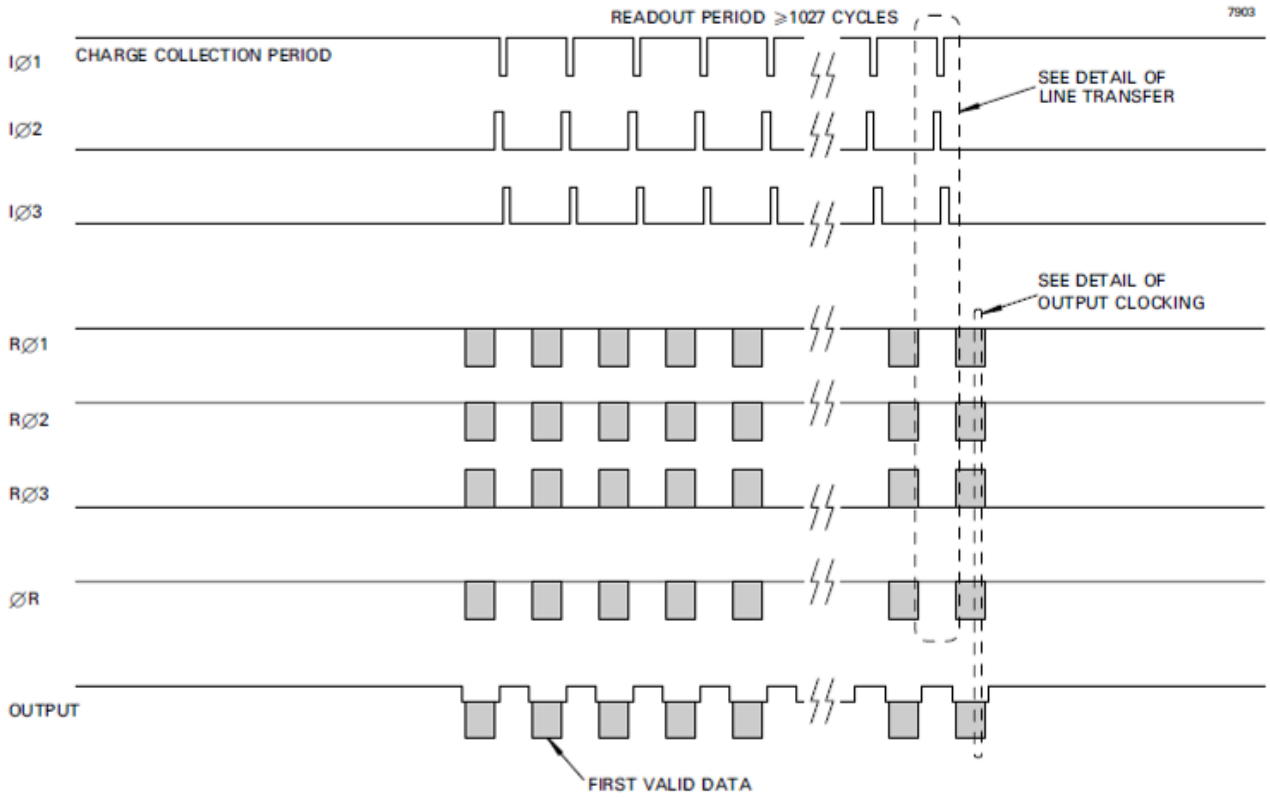
PIN	REF	DESCRIPTION	CLOCK HIGH OR DC LEVEL (V)			MAXIMUM RATINGS with respect to V_{SS}
			Min	Typical	Max	
1	ABD	Anti-blooming drain (see note 10)	VOD			-0.3 to +25V
2	I∅3	Image area clock	8	12	15	±20V
3	I∅2	Image area clock	8	12	15	±20V
4	I∅1	Image area clock	8	12	15	±20V
5	OG	Output Gate	1	2	5	±20V
6	-	No Connection		-		-
7	SS	Substrate	0	9	10	-
8	∅R	Output reset pulse (left and right amplifiers)	8	12	15	±20V
9	R∅2L	Output register clock (left section)	8	10	15	±20V
10	R∅1L	Output register clock (left section)	8	10	15	±20V
11	OD	Output transistor drain (left and right amplifiers)	27	29	32	-0.3 to +32V
12	OSL	Output transistor source (left amplifier)	See note 11			-0.3 to +25V
13	OSR	Output transistor source (right amplifier)	See note 11			-0.3 to +25V
14	RD	Reset transistor drain (left and right amplifiers)	15	17	19	-0.3 to +25V
15	R∅1R	Output register clock (right section)	8	10	15	±20V
16	R∅2R	Output register clock (right section)	8	10	15	±20V
17	R∅3	Output register clock (left and right sections)	8	10	15	±20V
18	SS	Substrate	0	9	10	-
19	-	No Connection		-		-
20	DG	Dump gate (see note 12)	-	0	-	±20V
21	I∅1	Image area clock	8	12	15	±20V
22	I∅2	Image area clock	8	12	15	±20V
23	I∅3	Image area clock	8	12	15	±20V
24	ABG	Anti-blooming gate	0	0	5	±20V

Maximum voltages between pairs of pins:
pin 12 (OSL) to pin 11 (OD).....±15 V
pin 11 (OD) to pin 13 (OSR) .....±15 V
Maximum output transistor current .....10 mA

NOTES

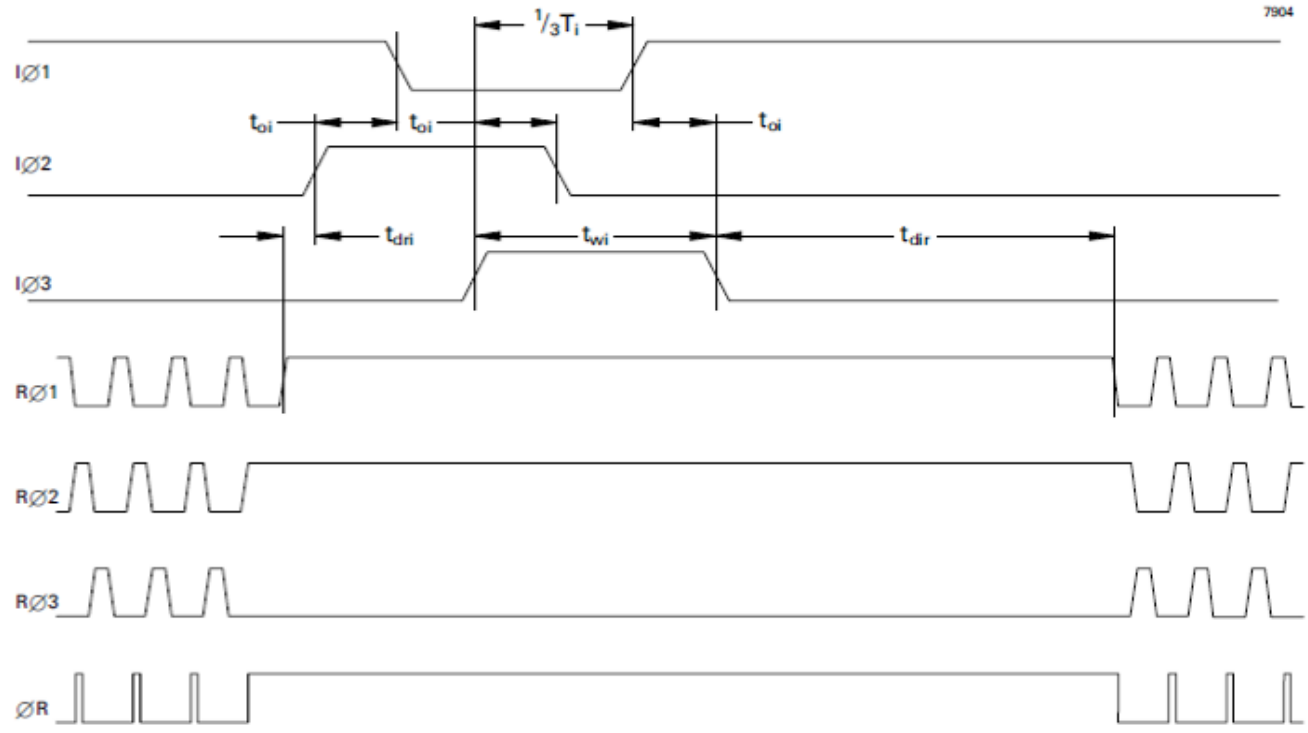
9. Readout register clock pulse low levels +1V; other clock low levels 0 ± 0.5V
10. Drain not incorporated, but bias is still necessary.
11. 3 to 5V below OD. Connect to ground using a 3 to 5 mA current source or appropriate load resistor (typically 5 to 10kΩ).
12. Non-charge dumping level shown. For operation in charge dumping mode, DG should be pulsed to 12 ± 2V
13. All devices will operate at the typical values given. However, some adjustment within the minimum to maximum range may be required to optimise performance for critical applications. It should be noted that conditions for optimum performance may differ from device to device.
14. With the R∅ connections shown, the device will operate through the right-hand output only. In order to operate from both outputs R∅1 (L) and R∅2 (L) should be reversed.

FRAME READOUT TIMING DIAGRAM

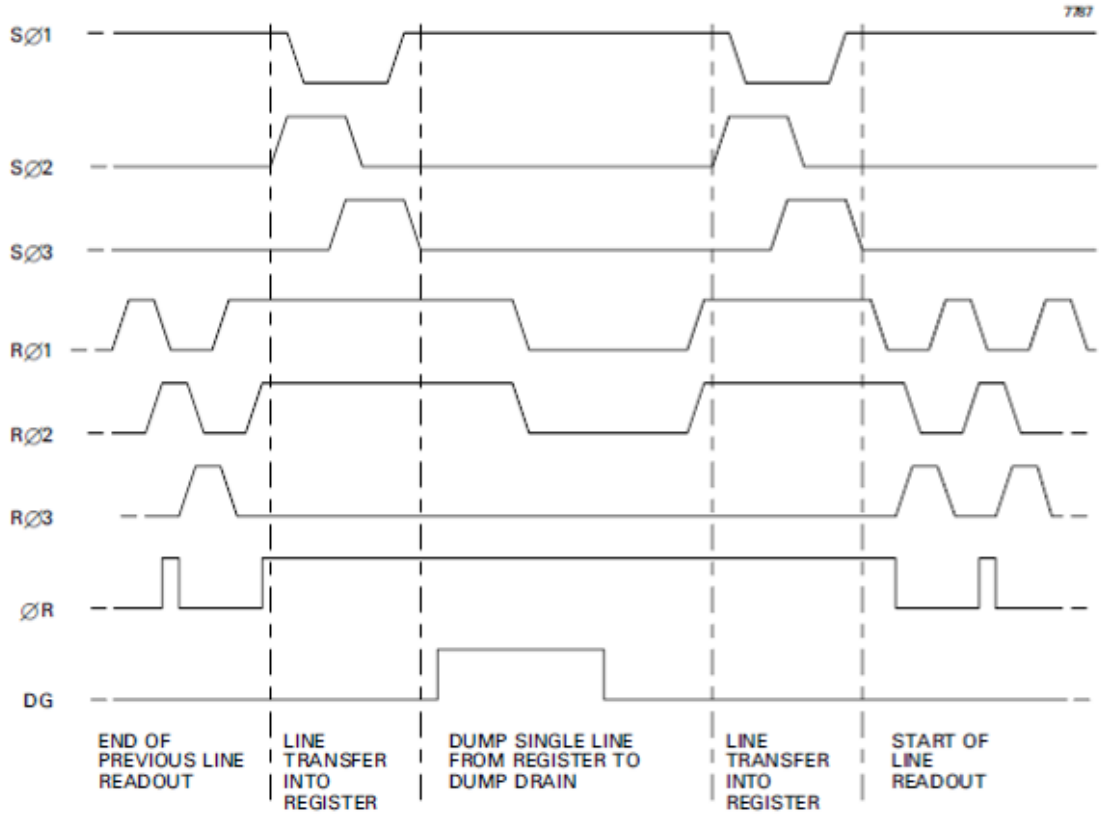


DETAIL OF LINE TRANSFER (Not to scale)

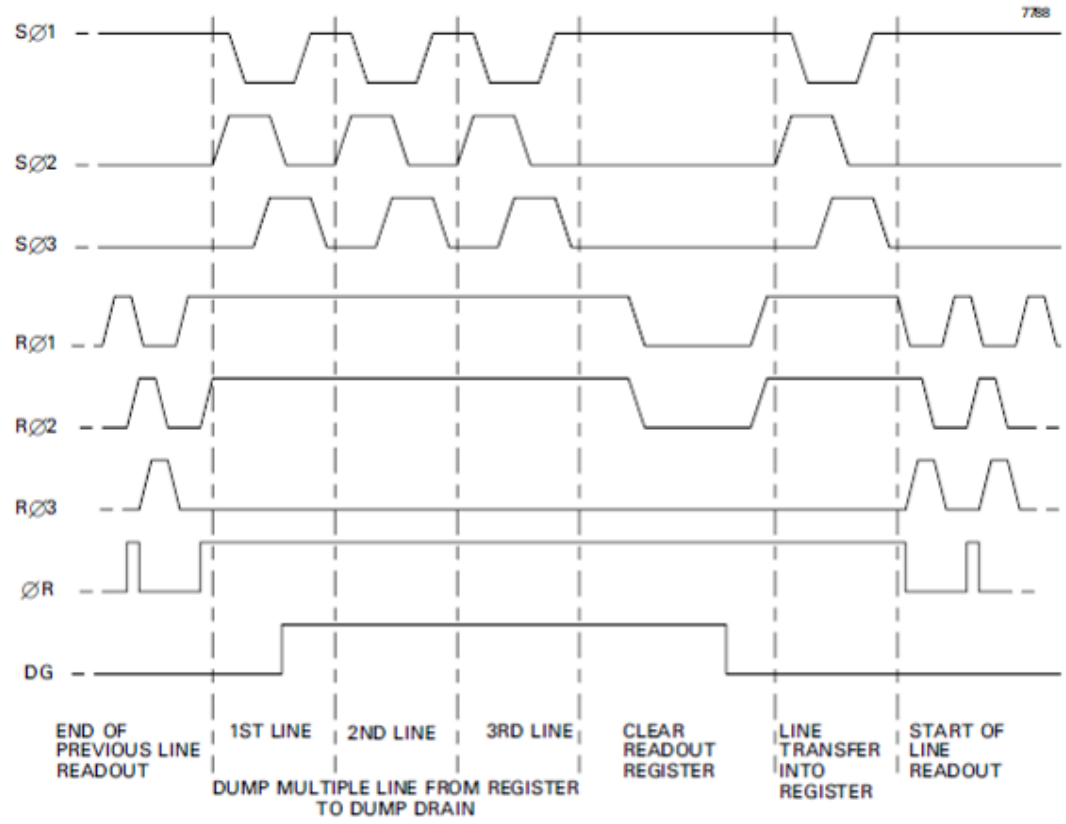
(For output from a single amplifier)



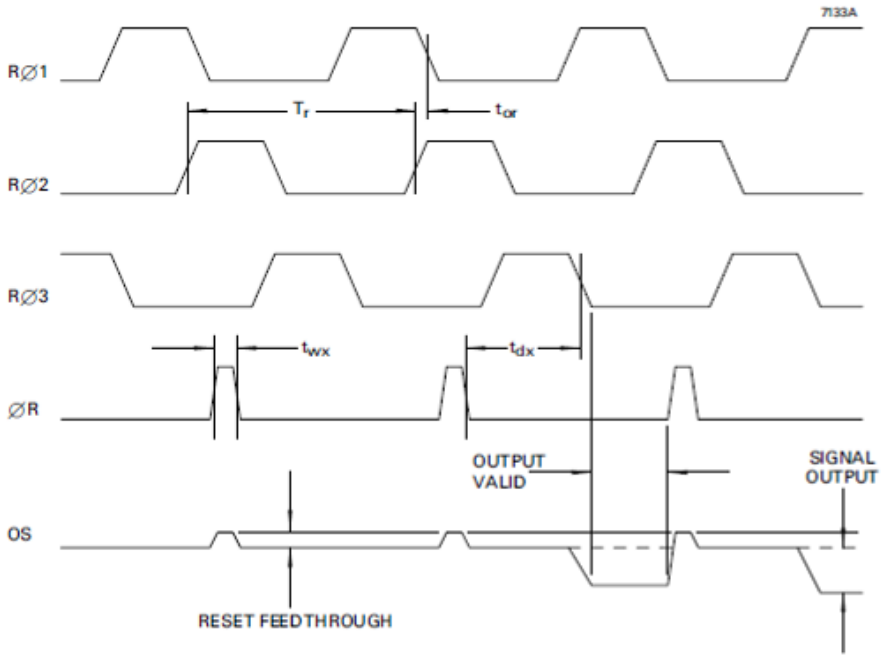
DETAIL OF VERTICAL LINE TRANSFER (Single line dump)



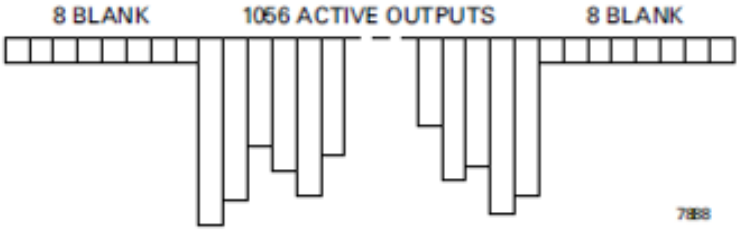
DETAIL OF VERTICAL LINE TRANSFER (Multiple line dump)



DETAIL OF OUTPUT CLOCKING



LINE OUTPUT FORMAT



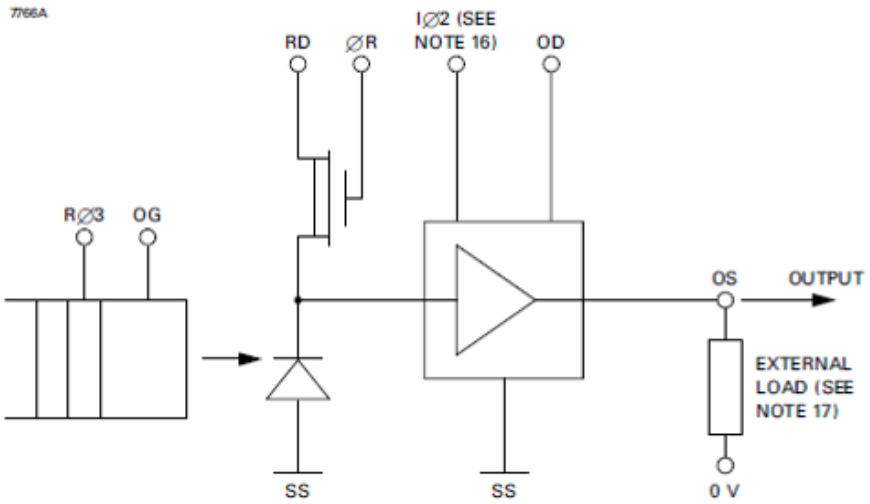
CLOCK TIMING REQUIREMENTS

Symbol	Description	Min	Typical	Max	
T_i	Image clock period	4	14	see note 15	µs
t_{wi}	Image clock pulse width	2	5	see note 15	µs
t_{ri}	Image clock pulse rise time (10 to 90%)	0.1	5	$T_i - 2t_{wi}$	µs
t_{fi}	Image clock pulse fall time (10 to 90%)	t_{ri}	t_{ri}	$T_i - 2t_{wi}$	µs
t_{oi}	Image clock pulse overlap	$(t_{ri} + t_{fi})/2$	0.6	$(3t_{wi} - T_i)/2$	µs
t_{dir}	Delay time, I∅ stop to R∅ start	1	2	see note 15	µs
t_{dri}	Delay time, R∅ stop to I∅ start	1	1	see note 15	µs
T_r	Output register clock cycle period	200	1000	see note 15	ns
t_{rr}	Clock pulse rise time (10 to 90%)	50	$0.1T_r$	$0.3T_r$	ns
t_{fr}	Clock pulse fall time (10 to 90%)	t_{rr}	$0.1T_r$	$0.3T_r$	ns
t_{or}	Clock pulse overlap	20	$0.5t_{rr}$	$0.1T_r$	ns
t_{wx}	Reset pulse width	30	$0.1T_r$	$0.3T_r$	ns
t_{rx}, t_{fx}	Reset pulse rise and fall times	$0.2t_{wx}$	$0.5t_{rr}$	$0.1T_r$	ns
t_{dx}	Delay time, ∅R low to R∅3 low	30	$0.5T_r$	$0.8T_r$	ns

NOTES

15.No maximum other than that necessary to achieve an acceptable dark signal at the longer readout times.

OUTPUT CIRCUIT



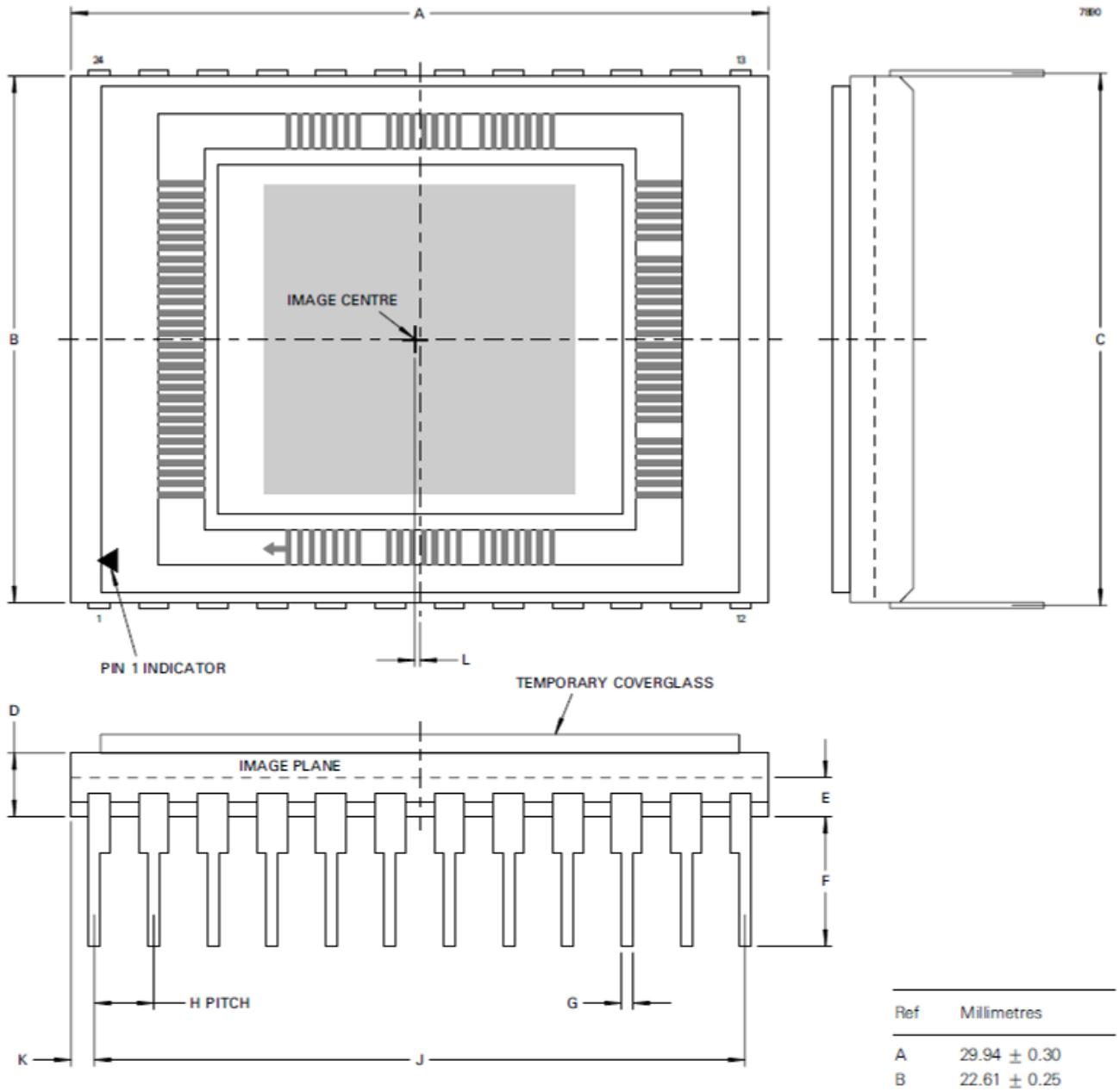
NOTES

16. The amplifier has a DC restoration circuit which is internally activated whenever I∅2 is high.

17. Not critical; can be a 3 to 5mA constant current supply or an appropriate load resistor.

OUTLINES (All dimensions in millimetres; dimensions without limits are nominal)

Standard Ceramic Package



Ref	Millimetres
A	29.94 ± 0.30
B	22.61 ± 0.25
C	22.86 ± 0.25
D	2.70 ± 0.27
E	1.65 ± 0.25
F	5.6 ± 0.5
G	0.46 ± 0.05
H	2.54 ± 0.13
J	27.94 ± 0.13
K	1.0 ± 0.3
L	0.2

ORDERING INFORMATION

Options include:

- Temporary quartz window
- Permanent quartz window
- Temporary glass window
- Permanent glass window
- Fibre-optic coupling
- UV coating
- X-ray phosphor coating

For further information on the performance of these and other options, contact e2v.

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full antistatic handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving socket pins to be positively grounded
- Unattended CCDs should not be left out of their conducting foam or socket.

Evidence of incorrect handling will invalidate the warranty. All devices are provided with internal protection circuits to the gate electrodes (pins 2, 3, 4, 5, 8, 9, 10, 15, 16, 17, 20, 21, 22, 23, 24) but not to the other pins.

HIGH ENERGY RADIATION

Device characteristics will change when subject to ionising radiation.

Users planning to use CCDs in a high radiation environment are advised to contact e2v.

TEMPERATURE LIMITS

	Min	Typical	Max	
Storage	73	-	373	K
Operating	73	243	323	K

Operation or storage in humid conditions may give rise to ice on the sensor surface on cooling, causing irreversible damage.

Maximum device heating/cooling.....5 K/min