EV10AS180A
Low Power L-Band 10-bit 1.5 GSps ADC
ANALOG to DIGITAL CONVERTER
Datasheet DS 60S 221991(G)

MAIN FEATURES

- Single Core ADC Architecture with 10-bit Resolution Integrating a Selectable 1:1/2/4 DEMUX
- 1.5 GSps Guaranteed Conversion Rate
- Differential Input Clock (AC Coupled)
- Analog Input Voltage: 500 mVpp Differential Full Scale (AC Coupled)
- Analog and Clock Input Impedance: 100Ω Differential
- LVDS Differential Output Data with Swing Adjustment and Data Ready
- Fine Adjustment of ADC Gain, Offset
- Fine Adjustment of Sampling Delay for Interleaving
- Static and Dynamic Test Mode for ADC and DEMUX
- Data Ready Common to the 4 Output Ports
- 1.75W Power Dissipation (1:2 Ratio with Standard LVDS Output Swing)
- Power Supply: 5.2V, 3.3V and 2.5V (Output Buffers)
- LGA255, Ci-CGA255 or CCGA255 Package

PERFORMANCES

- 2.250 GHz Full Power Input Bandwidth (–3 dB)
- Low Latency 2.5-5.5 Clock Cycles
- Gain Flatness:
  ~0.5 dB from 10 MHz to 750 MHz (1^{st} Nyquist)
  ~1.2 dB from 750 MHz to 1500 MHz (2^{nd} Nyquist)
  ~1.5 dB from 1500 MHz to 1800 MHz (L Band)
- Single Tone Performance:
  SFDR = –60 dBFS; ENOB = 8.4-Bit; SNR = 54 dBFS at Fin = 750 MHz @ –3 dBFS, Fs = 1.5 GSps
  SFDR = –59 dBFS; ENOB = 8.0-Bit; SNR = 52 dBFS at Fin = 1800 MHz @ –3 dBFS, Fs = 1.5 GSps
  SFDR = –62 dBFS; ENOB = 8.5-Bit; SNR = 55 dBFS at Fin = 750 MHz @ –12 dBFS, Fs = 1.5 GSps
  SFDR = –61 dBFS; ENOB = 8.4-Bit; SNR = 54 dBFS at Fin = 1800 MHz @ –12 dBFS, Fs = 1.5 GSps
- Broadband Performance:
  NPR = 44 dB at –13 dBFS Optimum Loading Factor in 1^{st} Nyquist
  NPR = 43 dB at –13 dBFS Optimum Loading Factor in L-band
- Radiation Tolerance: no Sensitivity up to 110 Krad TID (Low Dose Rate)

MAIN APPLICATION

- Direct L-band RF Down Conversion
- Defense Radar Systems
- Satellite Communication Systems

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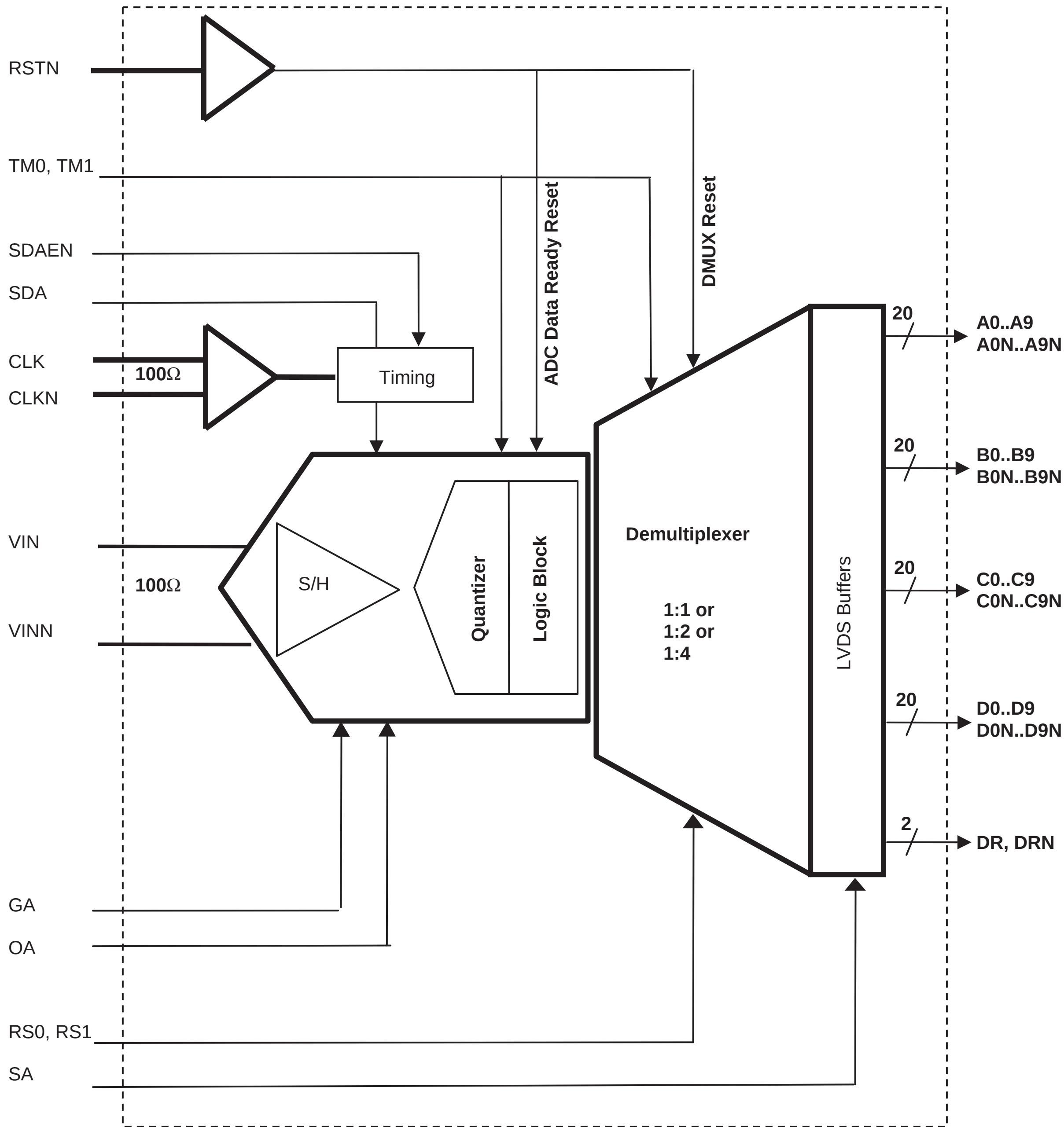
1. GENERAL DESCRIPTION

Figure 1-1. ADC with Integrated DEMUX Block Diagram



The EV10AS180A is a 10-bit 1.5 GSps ADC. The device includes a front-end Track and Hold stage (T/H), followed by an analog encoding stage (Analog Quantizer) which outputs analog residues resulting from analog quantization. Successive banks of latches regenerate the analog residues into logical levels before entering an error correction circuitry and a resynchronization stage followed by a DEMUX with 100Ω differential output buffers.

The EV10AS180A works in fully differential mode from analog inputs up to digital outputs.

It operates in the first Nyquist and L-Band (Fin ranging from DC to 1800 MHz).

DEMUX Ratio (1:1 or 1:2 or 1:4) can be selected with the 2 pins RS0, RS1.

DEMUX outputs are synchronous on each port.

A differential Data Ready output is available to indicate when the outputs are valid. The Data Ready DR, DRN is common to the 4 ports.

A power up reset ensures to synchronize internal signals and ensures output data to be properly ordered. An external Reset (RSTN) can also be used.

The gain control pin GA and offset control OA are provided to adjust the ADC gain and offset transfer function.

The swing of ADC output buffers can be lowered through the SA pin.

A Sampling Delay Adjust function (SDA) is provided to fine tune the ADC aperture delay, for applications

requesting the interleaving of multiple ADCs for example.

For debug and testability, the following functions are provided:

- a static test mode, used to test either V_{OL} or V_{OH} at the ADC outputs (all bits at “0” level or “1” level respectively),
- a dynamic built-In Test, providing series of “1”s and “0” in a checker board pattern fashion on all 4 ports.

A diode is provided to monitor the junction temperature, with both anode and cathode accessible.

2. CIRCUIT ELECTRICAL CHARACTERISTICS

2.1 Absolute Maximum Ratings

Table 2-1. Absolute Maximum ratings

Parameter	Symbol	Comments	Value	Unit
V_{CC5} supply voltage	V_{CC5}	see note (4)	GND to 6.0	V
V_{CC3} supply voltage	V_{CC3}	see note (4)	GND to 4.0	V
V_{CCO} supply voltage	V_{CCO}	see note (4)	GND to 3.0	V
Analog input voltages	V_{IN} or V_{INN}	Common Mode	Min 2.0 Max 4.0	V
Maximum difference between V_{IN} and V_{INN}	$\|V_{IN} – V_{INN}\|$		2.0 (4 Vpp = +13 dBm in 100Ω)	V
Clock input voltage	V_{CLK} or V_{CLKN}	Common Mode	Min 2.0 Max 4.0	V
Maximum difference between V_{CLK} and V_{CLKN}	$\|V_{CLK} – V_{CLKN}\|$		1.5 (3 Vpp)	V
Analog input settings	V_A	OA, GA, SDA, SA	–0.3 to V_{CC3} + 0.3	V
Control inputs	V_D	SDAEN, TM0, TM1, DECN, RS0, RS1, RSTN	–0.3 to V_{CC3} + 0.3	V
Junction Temperature	T_J		170	°C
Storage Temperature	Tstg		–65 to 150	°C
Electro-Static Discharge	ESD HBM	Human Body Model	1000	V

Notes:
1. Absolute maximum ratings are limiting values (referenced to GND = 0V), to be applied individually, while other parameters are within specified operating conditions. Exposure to maximum rating and beyond may damage the device.There is no guarantee of operation above specification defined in table 2.3
   All integrated circuits have to be handled with appropriate care to avoid damages due to ESD. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.
2. Maximum ratings enable active inputs with ADC powered off.
3. Maximum ratings enable floating inputs with ADC powered on.
4. The power-up of the 3 power supplies has to be completed within a limited time. Long exposure to partial powered ON supplies may damage the device.

2.2 Recommended Conditions Of Use

Table 2-2. Recommended Conditions of Use

Parameter	Symbol	Comments	Typ	Unit
Power supplies	V_{CC5}	No specific power supply sequencing required during power ON/OFF[(1)(2)]	5.2	V
	V_{CC3}		3.3	V
	V_{CCO}		2.5	V
Differential analog input voltage (Full Scale)	$V_{IN} – V_{INN}$	100Ω differential	500	mVpp
Clock input power level (Ground common mode)	$P_{CLK} – P_{CLKN}$	100Ω differential input	4	dBm
Operating Temperature Range	Tc, Tj	For functionality	Tc > –55 to Tj < 125	°C
Operating Temperature Range	Tc, Tj	For performances	Tc > –55 to Tj < 110	°C

Note: 1. To benefit of the internal power on reset, V_{CC3} should be applied before V_{CC5}. Please refer to Section 5.5 ”Power Up Reset” on page 28 for more details.

2. The power-up of the 3 power supplies has to be completed within a limited time. Long exposure to partial powered ON supplies may damage the device.

2.3 Electrical Characteristics

Unless otherwise stated, specifications apply over the full operating temperature range (for performance). V_{CC5} = 5.2V, V_{CC3} = 3.3V, V_{CCO} = 2.5V, typical SA and GA setting.

Table 2-3. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test level
RESOLUTION		10			bit	1,6
POWER REQUIREMENTS						
Power Supply voltage - Analog - Analog Core and Digital - Output buffers	 V_{CC5} V_{CC3} V_{CCO}	 5.0 3.15 2.4	 5.2 3.3 2.5	 5.5 3.45 2.6	 V V V	1,6
Power Supply current in 1:1 DEMUX Ratio - Analog - Analog Core and Digital - Output buffers	I_V_{CC5} I_V_{CC3} I_V_{CCO}		 71 300 100	 85 330 110	 mA mA mA	1,6
Power Supply current in 1:2 DEMUX Ratio - Analog - Analog Core and Digital - Output buffers	I_V_{CC5} I_V_{CC3} I_V_{CCO}		 71 312 137	 85 335 160	 mA mA mA	1,6
Power Supply current in 1:4 DEMUX Ratio - Analog - Analog Core and Digital - Output buffers	I_V_{CC5} I_V_{CC3} I_V_{CCO}		 71 325 216	 85 355 240	 mA mA mA	1,6
Power dissipation - 1:1 Ratio with standard LVDS output swing - 1:2 Ratio with standard LVDS output swing - 1:4 Ratio with standard LVDS output swing	 PD PD PD		 1.6 1.75 1.9	 1.9 2.0 2.3	 W W W	1,6

Table 2-3. Electrical Characteristics (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test level
LVDS Data and Data Ready Outputs						
Logic compatibility		LVDS differential				
Output Common Mode[(1)]	V_{OCM}	1.125	1.25	1.375	V	1,6
Differential output[(1)(2)]	V_{ODIFF}	250	350	450	mVp	1,6
Output level "High"[(3)]	V_{OH}	1.25	–	–	V	1,6
Output level "Low"[(3)]	V_{OL}	–	–	1.25	V	1,6
Output data format		Binary				1,6
ANALOG INPUT						
Input type		AC coupled				
Analog Input Common Mode (for DC coupled input)			3.1		V	
Full scale input voltage range (differential mode)	V_{IN} V_{INN}		±125 ±125		mVp mVp	1,6
Full scale analog input power level	P_{IN}		–5		dBm	1,6
Analog input capacitance (die only)	C_{IN}		0.3		pF	5
Input leakage current (VIN = VINN = 0V)	I_{IN}		50		µA	5
Analog Input resistance (Differential)	R_{IN}	94	100	106	Ω	4
CLOCK INPUT (CLK, CLKN)						
Input type		DC or AC coupled				
Clock Input Common Mode (for DC coupled clock)	V_{ICM}		2		V	1,6
Clock Input power level (low phase noise sinewave input) at 1.5 GHz	P_{CLK}	0	4	+7	dBm	4
Clock input swing (differential voltage) at 1.5 GHz	V_{CLK} V_{CLKN}	±447	±708	±1000	mVp	4
Clock input capacitance (die only)	C_{CLK}		0.3		pF	4
Clock Input resistance (Differential)	R_{CLK}	94	100	106	Ω	4
RSTN (active low)						
Logic compatibility		2.5V CMOS compatible				
Input level "High"	V_{IH} $\lvert I_{IH}\rvert$	2.0		 200	V µA	1,6 5
Input level "Low"	V_{IL} $\lvert I_{IL}\rvert$			0.4 500	V µA	1,6 5
DIGITAL INPUTS (RS0, RS1, DECN, SDAEN, TM1, TM0)						
Logic low - Resistor to ground - Voltage level - Input current	 R_{IL} V_{IL} I_{IL}	 0 – –		 10 0.5 450	 Ω V µA	 1 4 5

Table 2-3. Electrical Characteristics (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test level
Logic high - Resistor to ground - Voltage level - Input current	 R_{IH} V_{IH} I_{IH}	 10k 2.0 –		 infinite – 150	 Ω V µA	 1 4 5
OFFSET, GAIN & SAMPLING DELAY ADJUST SETTINGS (OA, GA, SDA)						
Min voltage for minimum Gain, Offset or SDA	Analog_min	$2*V_{CC3}/3 – 0.5$			V	1,6
Max voltage for maximum Gain, Offset or SDA	Analog_max			$2*V_{CC3}/3 + 0.5$	V	1,6
Input current for nominal setting	I_{nom}			50	µA	5
ANALOG SETTINGS (SA)						
SA voltage for default swing value	S_{max}			$2*V_{CC3}/3$		1,6
SA voltage for minimum swing value	S_{min}	$2*V_{CC3}/3 – 0.5$				5
Input current (low) for default swing value	I_{min}			50	µA	5
Input current (high) for min swing value	I_{max}			150	µA	5

Notes: 1. Assuming 100Ω termination ASIC load.
2. V_{ODIFF} can be lowered down to 100 mV with SA pin to reduce power consumption.
3. V_{OH} min and V_{OL} max can never be 1.25V at the same time when V_{ODIFF}min.

2.4 Converter Characteristics

Unless otherwise stated, specifications apply over the full operating temperature range (for performance). V_{CC5} = 5.2V, V_{CC3} = 3.3V, V_{CCO} = 2.5V, typical SA and GA setting.

Table 2-4. DC Converter Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test level
Resolution			10		bit	
DC ACCURACY						
Differential Non Linearity (for information only)	DNL+		0.5		LSB	1,6
Integral Non Linearity (for information only)	INL+		1.0		LSB	1,6
Integral Non Linearity (for information only)	INL-		–1.0		LSB	1,6
Gain central value @10 MHz [(1)]	ADCGAIN	0.95	1.0	1.05		1,6
Gain error drift vs temperature			±10		%	4
ADC offset[(2)]	ADCOFFSET			±10	LSB	1,6

Notes: 1. The ADC Gain center value can be tuned thanks to Gain adjust function.
2. The ADC offset can be tuned to mid code 512 thanks to Offset adjust function.

2.5 Dynamic Performance

Unless otherwise stated, specifications apply over the full operating temperature range (for performance) assuming an external clock jitter of 225 fs rms (corresponds to Teledyne e2v testbench value). ADC internal clock jitter is 200 fs rms. V_{CC5} = 5.2V, V_{CC3} = 3.3V, V_{CCO} = 2.5V, typical GA and SA setting.

Table 2-5. Dynamic Performance

Parameter	Symbol	Min	Typ	Max	Unit	Test level
AC Analog Inputs						
Full power Input Bandwidth (–3 dB)	FPBW		2.25		GHz	4
Gain Flatness (from 10 to 750 MHz)			0.5		dB	4
Gain Flatness (from 750 to 1500 MHz)			1.2		dB	4
Gain Flatness (from 1500 to 1800 MHz)			1.5		dB	4
Deviation from linear phase (1st Nyquist)			5		°	5
Deviation from linear phase (2nd Nyquist)			1		°	5
Deviation from linear phase (L-band up to 2.25 GHz)			2		°	5
Input voltage standing Wave Ratio up to 1.8 GHz (unpowered device)	VSWR			1.2:1		4
AC Performance in 1st Nyquist –12 dBFS differential input mode, 50% clock duty cycle, +4 dBm differential clock, external jitter = 225 fs rms max						
Signal to Noise And Distortion Ratio FS = 1.5 GSps Fin = 750 MHz	SINAD	48.7	53		dBFS	1,6
Effective Number of Bits FS = 1.5 GSps Fin = 750 MHz	ENOB	7.8	8.5		Bit FS	1,6
Signal to Noise Ratio FS = 1.5 GSps Fin = 750 MHz	SNR	52	55		dBFS	1,6
Total Harmonic Distortion (25 harmonics) FS = 1.5 GSps Fin = 750 MHz	|THD|	49	60		dBFS	1,6
Spurious Free Dynamic Range FS = 1.5 GSps Fin = 750 MHz	|SFDR|	52	62		dBFS	1,6
Noise Power Ratio Notch centered on 50 MHz, notch width 500 KHz on 20 MHz –700 MHz band 1.5 GSps at optimum loading factor of –13.1 dBFS	NPR		44.0		dB	4
Noise Power Ratio Notch centered on 350 MHz, notch width 500 KHz on 20 MHz –700 MHz band 1.5 GSps at optimum loading factor of –13.1 dBFS	NPR		44.0		dB	4
Noise Power Ratio Notch centered on 657 MHz, notch width 500 KHz on 20 MHz –700 MHz band 1.5 GSps at optimum loading factor of –13.1 dBFS	NPR		44.0		dB	4
IMD3 differential **(2Fin1 – Fin2, 2Fin2 – Fin1, unfilterable 3rd order Intermodulation products)** At –7 dBFS Fin1 = 790 MHz Fin2 = 800 MHz	IMD3		–63		dBc	4
AC Performance in 2nd Nyquist –12 dBFS differential input mode, 50% clock duty cycle, +4 dBm differential clock, external jitter = 225 fs rms max						

Table 2-5. Dynamic Performance (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test level
Noise Power Ratio Notch centered on 800 MHz, notch width 500 KHz on 770 MHz –1450 MHz band 1.5 GSps at optimum loading factor of –13.1 dBFS	NPR		44.0		dB	5
Noise Power Ratio Notch centered on 1100 MHz, notch width 500 KHz on 770 MHz –1450 MHz band 1.5 GSps at optimum loading factor of –13.1 dBFS	NPR		44.0		dB	5
Noise Power Ratio Notch centered on 1407 MHz, notch width 500 KHz on 770 MHz –1450 MHz band 1.5 GSps at optimum loading factor of –13.1 dBFS	NPR		44.0		dB	5
AC Performance in LBAND –12 dBFS differential input mode, 50% clock duty cycle, +4 dBm differential clock, external jitter = 225 fs rms max						
Signal to Noise And Distortion Ratio FS = 1.5 GSps Fin = 1800 MHz	SINAD	48.7	52		dBFS	1,6
Effective Number of Bits FS = 1.5 GSps Fin = 1800 MHz	ENOB	7.8	8.4		Bit FS	1,6
Signal to Noise Ratio FS = 1.5 GSps Fin = 1800 MHz	SNR	52	54		dBFS	1,6
Total Harmonic Distortion (25 harmonics) FS = 1.5 GSps Fin = 1800 MHz	|THD|	49	58		dBFS	1,6
Spurious Free Dynamic Range FS = 1.5 GSps Fin = 1800 MHz	|SFDR|	52	61		dBFS	1,6
Noise Power Ratio Notch centered on 1550 MHz, notch width 500 KHz on 1520 MHz –2200 MHz band 1.5 GSps at optimum loading factor of –13.1 dBFS	NPR		43		dB	5
Noise Power Ratio Notch centered on 1850 MHz, notch width 500 KHz on 1520 MHz –2200 MHz band 1.5 GSps at optimum loading factor of –13.1 dBFS	NPR		43		dB	5
Noise Power Ratio Notch centered on 2157 MHz, notch width 500 KHz on 1520 MHz –2200 MHz band 1.5 GSps at optimum loading factor of –13.1 dBFS	NPR		42		dB	5
IMD3 differential **(2Fin1 – Fin2, 2Fin2 – Fin1, unfilterable 3rd order Intermodulation products)** At –7 dBFS Fin1 = 1550 MHz Fin2 = 1560 MHz	IMD3		–55		dBc	4
AC Performance in 1st Nyquist –3 dBFS differential input mode, 50% clock duty cycle, +4 dBm differential clock, external jitter = 225 fs rms max						
Signal to Noise And Distortion Ratio FS = 1.5 GSps Fin = 750 MHz	SINAD	46.3	52		dBFS	1,6
Effective Number of Bits FS = 1.5 GSps Fin = 750 MHz	ENOB	7.4	8.4		Bit FS	1,6

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Table 2-5. Dynamic Performance (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test level
Signal to Noise Ratio FS = 1.5 GSps Fin = 750 MHz	SNR	50	54		dBFS	1,6
Total Harmonic Distortion (25 harmonics) FS = 1.5 GSps Fin = 750 MHz	|THD|	48	56		dBFS	1,6
Spurious Free Dynamic Range FS = 1.5 GSps Fin = 750 MHz	|SFDR|	50	60		dBFS	1,6
AC Performance in L Band –3 dBFS differential input mode, 50% clock duty cycle, +4 dBm differential clock, external jitter = 225 fs rms max						
Signal to Noise And Distortion Ratio FS = 1.5 GSps Fin = 1800 MHz	SINAD	45.1	50		dBFS	1,6
Effective Number of Bits FS = 1.5 GSps Fin = 1800 MHz	ENOB	7.2	8.0		Bit FS	1,6
Signal to Noise Ratio FS = 1.5 GSps Fin = 1800 MHz	SNR	49	52		dBFS	1,6
Total Harmonic Distortion (25 harmonics) FS = 1.5 GSps Fin = 1800 MHz	|THD|	47	56		dBFS	1,6
Spurious Free Dynamic Range FS = 1.5 GSps Fin = 1800 MHz	|SFDR|	50	59		dBFS	1,6

2.6 Sensitivity to Radiations

2.6.1 Total Dose

The component is not sensitive to 110Krad with very low dose rate (36rad / hr)

2.6.2 Heavy Ions

It was concluded that the devices under test (P/N EV10AS180A) have:

- No SEL (SEL measured up to a LET of 80.72 MeV-cm^2/mg at 125degC with a tilt and up to 67.7 MeVcm^2/mg at 125degC without tilt),
- No SEFI
- No permanent error
- Low LET threshold of 0.7 to 1.6 MeV.cm^2/mg -> device may be sensitive to proton
- Saturated cross-section in the range of 3.8E-5 to 2.1 E-04 cm^2
- Worst case long SEU/SET duration is 48 consecutive corrupted data
- For a geostationary satellite:
  - SEE of 2.48E-04 to 8.24E-02/device.day
  - Worst case Multiconversion errors is 1.27E-02/device/day (MTBF > 78 days)
  - Worst case Single conversion errors 8.24E-02/device.day (MTBF > 12 days)

2.6.3 Proton Tests

It was concluded that the devices under test (P/N EV10AS180A) have:

- No SEL (up to 184 MeV),
- No SEFI
- No permanent error
- Energy threshold is lower than 20 MeV
- Saturated cross-section in the range of 1E-10 to 1.3E-09 cm^2
- Worst case long SEU/SET duration is 5 consecutive corrupted data
- For a geostationary satellite:
  – SEE of 4.47E-05 to 7.83E-03/device.day
  – Worst case Multiconversion errors is 1.16E-03/device/day (MTBF> 862 days)
  – Worst case Single conversion errors of 7.83E-03/device.day (MTBF>127 days)
- For a LEO JASON satellite:
  – SEE of 7.12E-04 to 8.94E-02/device.day
  – Worst case Multiconversion errors is 1.36E-02/device/day (MTBF > 73 days)
  – Worst case Single conversion errors of 8.94E-02/device.day (MTBF >11 days)

2.7 Timing Characteristics and Switching Performances

Unless otherwise stated, specifications apply over the full operating temperature range (for performance).

See Section 3. ”Definition of Term” on page 17.

Table 2-6. Timing Characteristics and Switching Performances

Parameter	Symbol	Min	Typ	Max	Unit	Test level
SWITCHING PERFORMANCE AND CHARACTERISTICS						
Maximum clock frequency (1) 1:1 DEMUX Ratio 1:2 DEMUX Ratio 1:4 DEMUX Ratio		700 1500 1500			MHz	1,6
Clock frequency range(1)		300		1500	MHz	4
Maximum Output Rate per port (Data) 1:1 DEMUX Ratio 1:2 DEMUX Ratio 1:4 DEMUX Ratio		700 750 375			Msps	4
Analog input frequency		DC		1800	MHz	4
BER @ 1.5GSps @ –12 dBFS				10^{-9}	Error/sample	5
TIMING						
ADC settling time (VIN-VINN = 400 mV pp) (±2%)	TS		770		ps	4
ADC step response (10% to 90%)			160		ps	4
Clock duty cycle		40	50	60	%	4
Minimum clock pulse width (high)	TC1	0.25		0.375	ns	4

Table 2-6. Timing Characteristics and Switching Performances (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test level
Minimum clock pulse width (low)	TC2	0.25		0.375	ns	4
Aperture delay [(1)(6)]	TA		250		ps	4
Aperture delay adjustment	SDA	–42		+42	ps	4
Aperture jitter added by the ADC[(1)(6)]			200		fs rms	4
Output rise/fall time for DATA (20% to 80%)[(3)]	TR/TF	320	400	480	ps	4
Output rise/fall time for DATA READY (20% to 80%)[(3)]	TR/TF	510	700	890	ps	4
Data output delay[(4)] DMUX 1:1 DMUX 1:2 and 1:4	TOD	 3.1	 3 3.4	 3.7	 ns ns	4
Data Ready output delay[(4)] DMUX 1:1 DMUX 1:2 and 1:4	TDR	 3.4	 3.7 3.7	 4.0	 ns ns	4
DMUX 1:1 DMUX 1:2 DMUX 1:4	TDR –TOD		0.9 0.6 0.3		ns	4
Output Data to Data Ready propagation delay[(5)] DMUX 1:1 @ 750 MSps sampling rate DMUX 1:2 @ 1.5 GSps sampling rate DMUX 1:4 @ 1.5 GSps sampling rate	TD1	 1.08 0.84 1.45	 1.13 1 1.5	 1.20 1.10 1.55	 ns ns ns	4
Data Ready to Output Data propagation delay[(5)] DMUX 1:1 @ 750 MSps sampling rate DMUX 1:2 @ 1.5 GSps sampling rate DMUX 1:4 @ 1.5 GSps sampling rate	TD2	 0.16 0.31 1.1	 0.2 0.44 1.2	 0.24 0.49 1.25	 ns ns ns	4
Output Data Pipeline delay						
1:1 DEMUX Ratio						
Port A	TPDOA		3.5			
1:2 DEMUX Ratio						
Port A	TPDOA		3.5			
Port B	TPDOB		2.5		Clock cycles	4
1:4 DEMUX Ratio						
Port A	TPDOA		5.5			
Port B	TPDOB		4.5			
Port C	TPDOC		3.5			
Port D	TPDOD		2.5			
Data Ready Pipeline delay 1:1 DEMUX Ratio 1:2 DEMUX Ratio 1:4 DEMUX Ratio	TPDR		 4 4.5 7.5		Clock cycles	4
RSTN to DR, DRN	TRDR			10	ns	4
RSTN min pulse duration		4			ns	4

Notes: 1. See Definition Of Terms.

2. Data Ready outputs are active on both rising and falling edges (DR/2 mode)
3. L_{LOAD} = 5 nH, C_{LOAD} = 5 pF termination (for each single-ended output).
4. TOD and TDR propagation times are defined at package input/outputs. They are given for reference only.
5. Values for TD1 and TD2 are given for a 1.5 GSps external clock frequency (50% duty cycle). For different sampling rates, apply the following formula: TD1 = T/2 +(|TOD-TDR|) and TD2 = T/2 – (|TOD–TDR|), where T= clock period.
   Note: Due to the off centre edge of the data ready signal, this formula is an approximation.
6. Aperture delay and aperture jitter measured with SDA = OFF (default setting at RESET)

2.8 Timing Diagrams

Figure 2-1. Principle of Operation, DMUX 1:1

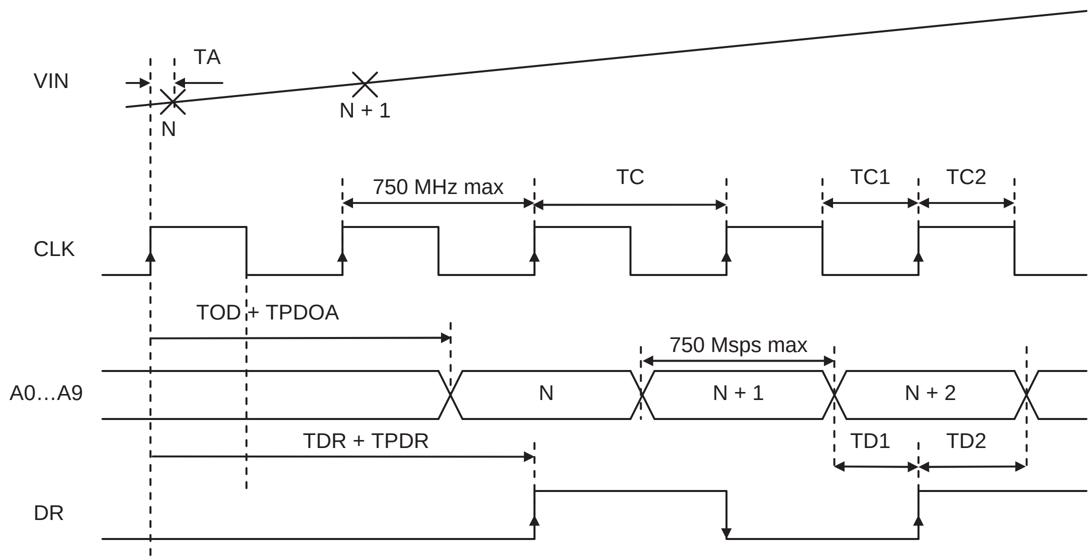


Figure 2-2. Principle of Operation, DMUX 1:2

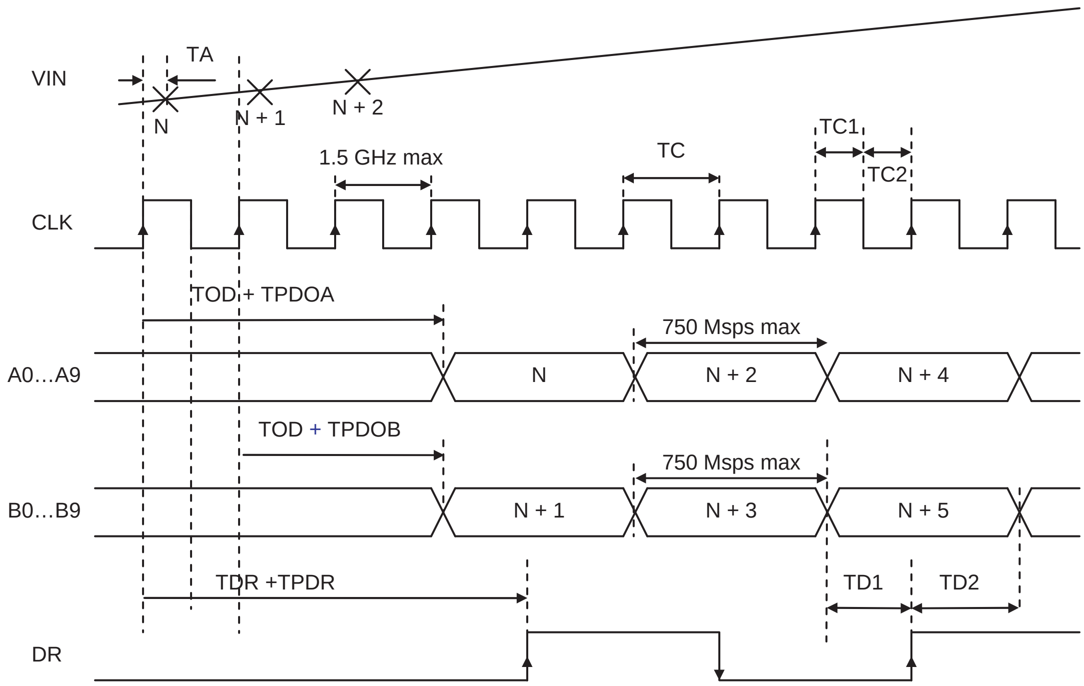


Figure 2-3. Principle of Operation, DMUX 1:4

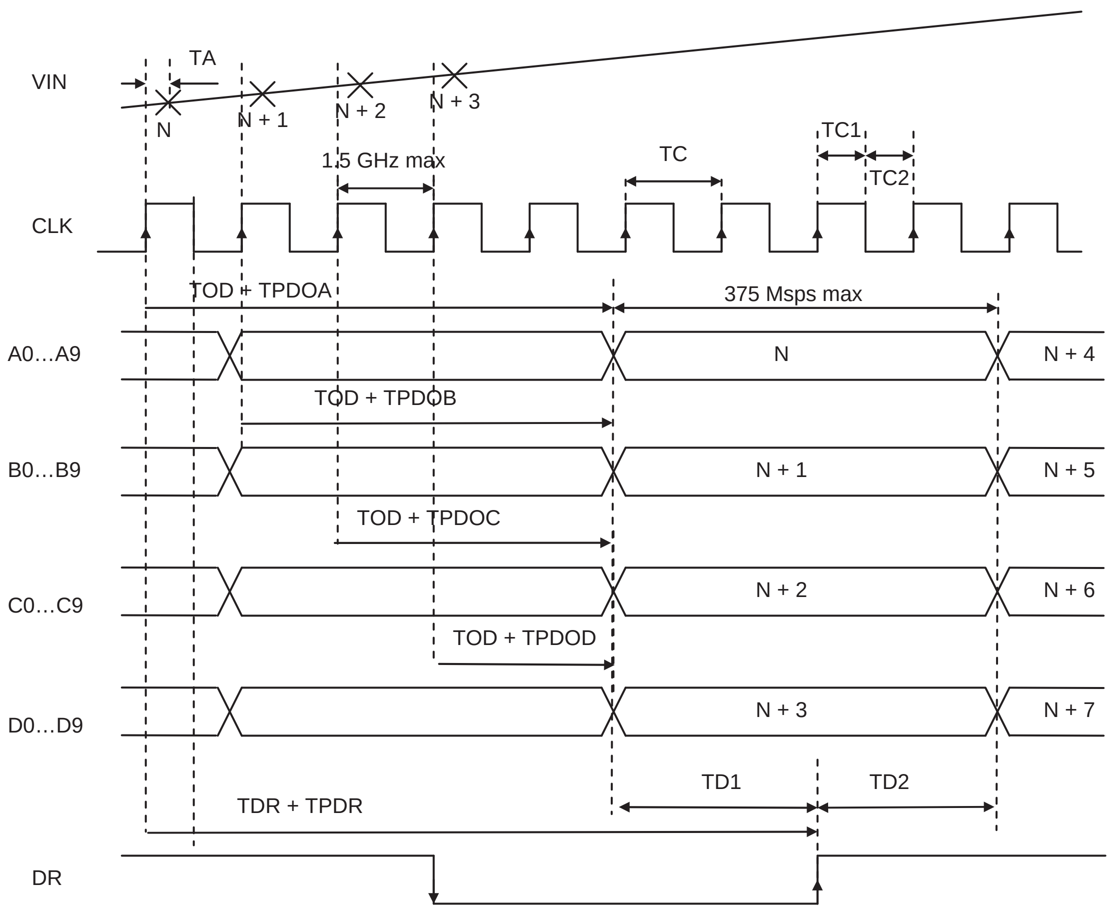
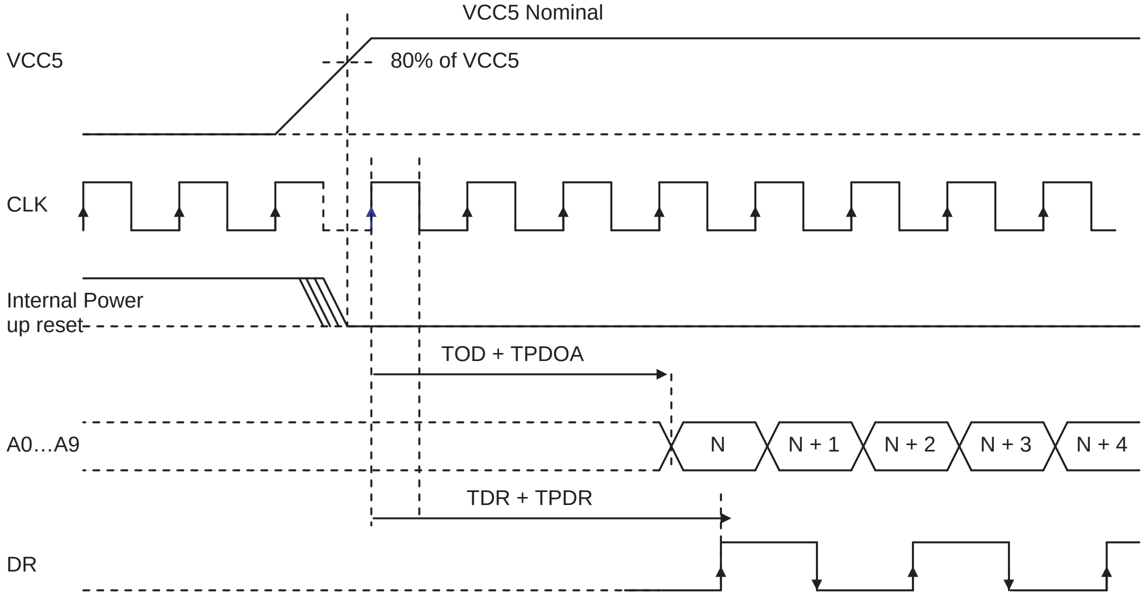
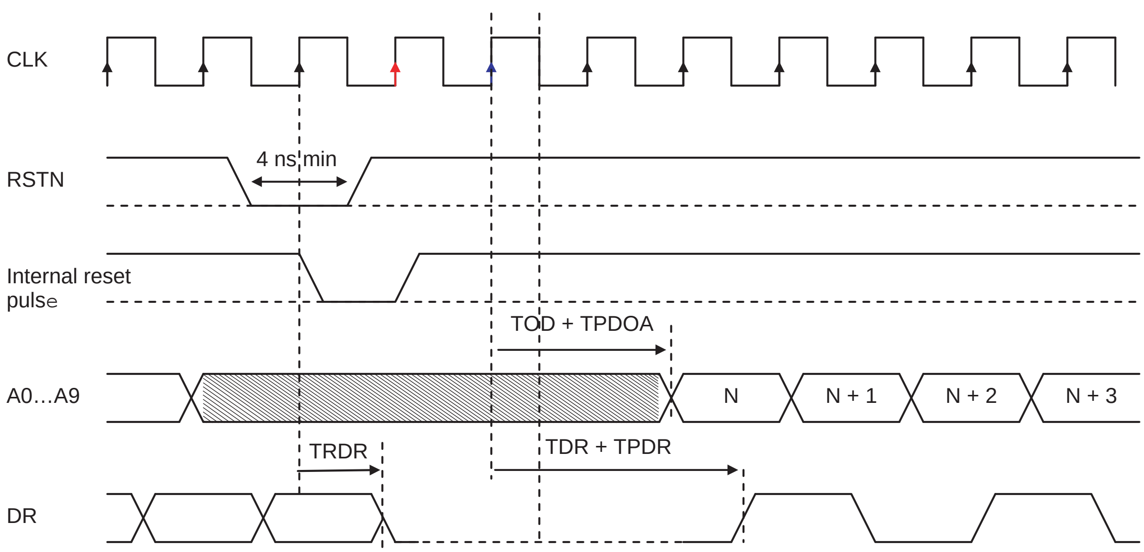


Figure 2-4. Power up Reset Timing Diagram (1:1 DMUX)



Note: assuming V_{CC3} is already switched on.

Figure 2-5. External Reset Timing Diagram (1:1 DMUX)



2.9 Explanation of Test Levels

1	100% production tested at +25°C[(1)].
2	100% production tested at +25°C[(1)], and sample tested at specified temperatures.
3	Sample tested only at specified temperatures.
4	Parameter is guaranteed by design and characterization testing (thermal steady-state conditions at specified temperature).
5	Parameter is a typical value only guaranteed by design only.
6	100% production tested over specified temperature range (for D/T and Space Grade[(2)]).

Note: Only MIN and MAX values are guaranteed (typical values are issuing from characterization results).

Notes: 1. Unless otherwise specified.

2. If applicable, please refer to “Ordering Information”

2.10 Coding

Table 2-7. ADC Coding Table

Differential analog input	Voltage level	Digital output Binary MSB (bit 9)…................LSB (bit 0)
> + 250.25 mV	>Top end of full scale + ½ LSB	1 1 1 1 1 1 1 1 1 1
+ 250.25 mV + 249.75 mV	Top end of full scale + ½ LSB Top end of full scale – ½ LSB	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0
+ 125.25 mV + 124.75 mV	3/4 full scale + ½ LSB 3/4 full scale – ½ LSB	1 1 0 0 0 0 0 0 0 0 1 0 1 1 1 1 1 1 1 1
+ 0.25 mV – 0.25 mV	Mid scale + ½ LSB Mid scale – ½ LSB	1 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1
–124.75 mV –124.25 mV	1/4 full scale + ½ LSB 1/4 full scale – ½ LSB	0 1 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1
–249.75 mV –250.25 mV	Bottom end of full scale + ½ LSB Bottom end of full scale – ½ LSB	0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0
< –250.25 mV	< Bottom end of full scale – ½ LSB	0 0 0 0 0 0 0 0 0 0

3. DEFINITION OF TERM

(Fs max)	*Maximum Sampling Frequency*	Performances are guaranteed up to Fs max
(Fs min)	*Minimum Sampling frequency*	Performances are guaranteed for Fs higher than Fs min.
(BER)	*Bit Error Rate*	Probability to exceed a specified error threshold for a sample at maximum specified sampling rate. An error code is a code that differs by more than ± 32 LSB from the correct code.
(AIF)	*Analog Input Frequency*	Analog input frequency range for which performances are guaranteed
(FPBW)	*Full power input bandwidth*	Analog input frequency at which the fundamental component in the digitally reconstructed output waveform has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis) for input at Full Scale –1 dB (–1 dBFS).
(SSBW)	*Small Signal Input bandwidth*	Analog input frequency at which the fundamental component in the digitally reconstructed output waveform has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis) for input at Full Scale –10 dB (–10 dBFS).
(SINAD)	*Signal to noise and distortion ratio*	Ratio expressed in dB of the RMS signal amplitude, set to 1dB below Full Scale (–1 dBFS), to the RMS sum of all other spectral components, including the harmonics except DC.
(SNR)	*Signal to noise ratio*	Ratio expressed in dB of the RMS signal amplitude, set to 1 dB below Full Scale, to the RMS sum of all other spectral components excluding the twenty five first harmonics.
(THD)	*Total harmonic distortion*	Ratio expressed in dB of the RMS sum of the first twenty five harmonic components, to the RMS input signal amplitude, set at 1 dB below full scale. It may be reported in dB (i.e, related to converter –1 dB Full Scale), or in dBc (i.e, related to input signal level).
(SFDR)	*Spurious free dynamic range*	Ratio expressed in dB of the RMS signal amplitude, set at 1 dB below Full Scale, to the RMS value of the highest spectral component (peak spurious spectral component). The peak spurious component may or may not be a harmonic. It may be reported in dB (i.e., related to converter –1 dB Full Scale), or in dBc (i.e, related to input signal level).
(ENOB)	*Effective Number Of Bits*	$ENOB = \frac{SINAD - 1.76 + 20\log(A/FS/2)}{6{,}02}$ Where A is the actual input amplitude and FS is the full scale range of the ADC under test
(DNL)	*Differential non linearity*	The Differential Non Linearity for an output code i is the difference between the measured step size of code i and the ideal LSB step size. DNL (i) is expressed in LSBs. DNL is the maximum value of all DNL (i). DNL error specification of less than 1 LSB guarantees that there are no missing output codes and that the transfer function is monotonic.
(INL)	*Integral non linearity*	The Integral Non Linearity for an output code i is the difference between the measured input voltage at which the transition occurs and the ideal value of this transition. INL (i) is expressed in LSBs, and is the maximum value of all |INL (i)|.
(TA)	*Aperture delay*	Delay between the rising edge of the differential clock inputs (CLK, CLKN) (zero crossing point), and the time at which (V_{IN}, V_{INN}) is sampled.

(JITTER)	*Aperture uncertainty*	Sample to sample variation in aperture delay. The voltage error due to jitter depends on the slew rate of the signal at the sampling point.
(TS)	*Settling time*	Time delay to achieve 0.2 % accuracy at the converter output when a 80% Full Scale step function is applied to the differential analog input.
(ORT)	*Overvoltage recovery time*	Time to recover 0.2 % accuracy at the output, after a 150 % full scale step applied on the input is reduced to midscale.
(TOD)	*Digital data Output delay*	Delay from the rising edge of the differential clock inputs (CLK, CLKN) (zero crossing point) to the next point of change in the differential output data (zero crossing) with specified load, excluding TPDO pipeline delay.
(TDR)	*Data ready output delay*	Delay from the rising edge of the differential clock inputs (CLK, CLKN) (zero crossing point) to the next point of change in the differential output clock (zero crossing) with specified load, exluding TPDR pipeline delay.
(TD1)	*Time delay from Data transition to Data Ready*	Time delay between Data transition to output clock (Data Ready). If output clock is in the middle of the Data, TD1=Tdata/2
(TD2)	*Time delay from Data Ready to Data*	Time delay between output clock (Data Ready) to Data transition. If output clock is in the middle of the Data, TD2=Tdata/2
(TD1-TD2)		The difference TD1-TD2 gives an information if the output clock is centered on the output data. If output clock is the middle of the data, TD1 = TD2 = Tdata/2
(TC)	*Encoding clock period*	TC1 = Minimum clock pulse width (high) TC = TC1 + TC2 TC2 = Minimum clock pulse width (low)
(TPDO)	*Output Data pipeline delay*	Number of clock cycles between the sampling edge of an input data and the associated output data being made available, (not taking in account the TOD).
(TPDR)	*Output Data Ready pipeline delay*	Number of clock cycles between the sampling edge of an input data and the associated output data ready rising edge (not taking into account the TDR).
(TRDR)	*Data Ready reset delay*	After a falling edge of the RSTN, delay between the sampling edge if an input data and the reset to digital zero transition of the Data Ready output signal DR
(TR)	*Rise time*	Time delay for the output DATA signals to rise from 20% to 80% of delta between low level and high level.
(TF)	*Fall time*	Time delay for the output DATA signals to fall from 20% to 80% of delta between low level and high level.
(PSRR)	*Power supply rejection ratio*	Ratio of input offset variation to a change in power supply voltage.
(NRZ)	*Non return to zero*	When the input signal is larger than the upper bound of the ADC input range, the output code is identical to the maximum code and the Out of Range bit is set to logic one. When the input signal is smaller than the lower bound of the ADC input range, the output code is identical to the minimum code, and the Out of range bit is set to logic one. (It is assumed that the input signal amplitude remains within the absolute maximum ratings).
(IMD)	*InterModulation Distortion*	The two tones intermodulation distortion (IMD) rejection is the ratio of either input tone to the worst third order intermodulation products.
(NPR)	*Noise Power Ratio*	The NPR is measured to characterize the ADC performance in response to broad bandwidth signals. When applying a notch-filtered broadband white-noise signal as the input to the ADC under test, the Noise Power Ratio is defined as the ratio of the average out-of-notch to the average in-notch power spectral density magnitudes for the FFT spectrum of the ADC output sample test.
(VSWR)	*Voltage Standing Wave Ratio*	The VSWR corresponds to the ADC input insertion loss due to input power reflection. For example a VSWR of 1.2 corresponds to a 20 dB return loss (ie. 99% power transmitted and 1% reflected).

4. PIN DESCRIPTION

Figure 4-1. Pin Mapping (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A		VCCO	NC (DGND)	B4	B5	B7	B8	NC (DGND)	DR	C8	C7	C5	C4	NC (DGND)	VCCO	DGND
B	DGND	VCCO	NC (DGND)	B4N	B5N	B7N	B8N	NC (DGND)	DRN	C8N	C7N	C5N	C4N	NC (DGND)	VCCO	DGND
C	NC (DGND)	NC (DGND)	VCCO	DGND	B6N	B6	B9	B9N	C9N	C9	C6	C6N	DGND	VCCO	NC (DGND)	NC (DGND)
D	B3	B3N	DGND	VCCO	VCCO	DGND	DGND	DGND	DGND	DGND	DGND	VCCO	VCCO	DGND	C3N	C3
E	B2	B2N	B1	DGND	DGND	DGND	VCCO	VCCO	VCCO	VCCO	DGND	DGND	DGND	C1	C2N	C2
F	B0	B0N	B1N	DGND	VCCO	DGND	DGND	VCCO	VCCO	DGND	DGND	VCCO	DGND	C1N	C0N	C0
G	NC (DGND)	NC (DGND)	A9N	DGND	VCCO	VCCO	AGND	AGND	AGND	AGND	VCCO	VCCO	DGND	D9N	NC (DGND)	NC (DGND)
H	A8	A8N	A9	DGND	DGND	VCCO	AGND	AGND	AGND	AGND	VCCO	DGND	DGND	D9	D8N	D8
J	A7	A7N	A6N	DGND	DGND	VCC3	AGND	AGND	AGND	AGND	VCC3	DGND	DGND	D6N	D7N	D7
K	A5	A5N	A6	VCC3	VCC3	VCC3	AGND	AGND	AGND	AGND	VCC3	VCC3	VCC3	D6	D5N	D5
L	A4	A4N	A3	DGND	DGND	DGND	VCC5	VCC5	VCC5	VCC5	DGND	DGND	DGND	D3	D4N	D4
M	A2	A2N	A3N	DGND	DGND	NC (DGND)	AGND	VCC5	AGND	VCC5	NC (DGND)	NC (DGND)	DGND	D3N	D2N	D2
N	A1	A1N	DIODE C	OA	DGND	NC (DGND)	AGND	VCC5	AGND	VCC5	DGND	DGND	DGND	DECN	D1N	D1
P	A0	A0N	DIODE A	GA	DGND	AGND	AGND	AGND	AGND	AGND	AGND	DGND	DGND	SA	D0N	D0
R	DGND	DGND	DGND	NC (DGND)	NC (DGND)	CLKN	AGND	AGND	AGND	AGND	AGND	SDAEN	RS1	TM1	DGND	DGND
T	DGND	DGND	DGND	RSTN	NC (DGND)	CLK	AGND	AGND	VIN	VINN	AGND	SDA	RS0	TM0	DGND	DGND

Note: Pin A1 is not populated.

Table 4-1. Pin Description

Signal Name	Pin Number	Description	Direction	Equivalent Simplified Schematics
POWER SUPPLIES				
V_{CC5}	L7, L8, L9, L10, M8, M10, N8, N10	5.2V analogue supply (Front-end Track & Hold circuitry). Referenced to AGND.	N/A	
V_{CC3}	J6, J11, K4, K5, K6, K11, K12, K13	3.3V power supply (ADC Core, Regeneration and Logic, DEMUX circuitry and Timing circuitry). Referenced to AGND.	N/A	

Table 4-1. Pin Description (Continued)

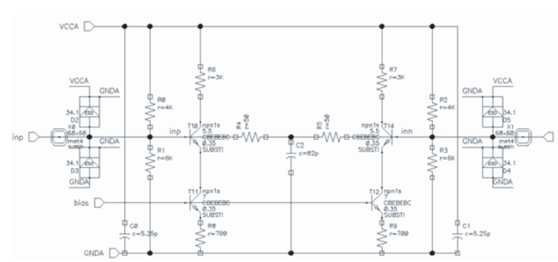
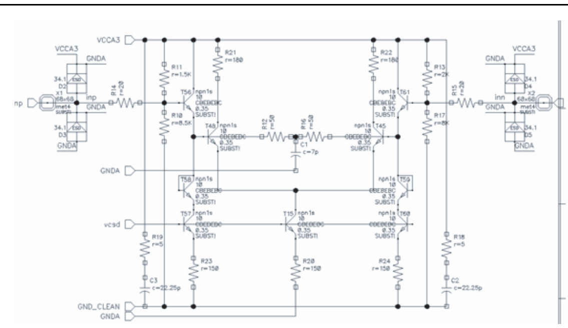
Signal Name	Pin Number	Description	Direction	Equivalent Simplified Schematics
V_{CC0}	A2, A15, B2, B15, C3, C14, D4, D5, D12, D13, E7, E8, E9, E10, F5, F8, F9, F12, G5, G6, G11, G12, H6, H11	2.5V digital power supply (output buffers). Referenced to DGND.	N/A	
AGND	G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10, M7, M9, N7, N9, P6, P7, P8, P9, P10, P11, R7, R8, R9, R10, R11, T7, T8, T11	Analogue Ground. AGND plane should be separated from DGND on the board (the two planes can be connected by 0Ω resistors).	N/A	
DGND	A16, B1, B16, C4, C13, D3, D6, D7, D8, D9, D10, D11, D14, E4, E5, E6, E11, E12, E13, F4, F6, F7, F10, F11, F13, G4, G13, H4, H5, H12, H13, J4, J5, J12, J13, L4, L5, L6, L11, L12, L13, M4, M5, M13, N5, N11, N12, N13, P5, P12, P13, R1, R2, R3, R15, R16, T1, T2, T3, T15, T16	Digital Ground for output buffers. DGND plane should be separated from AGND on the board (the two planes can be connected by 0Ω resistors).	N/A	
ANALOGUE INPUTS				
VIN VINN	T9 T10	Analogue input (differential) with internal common mode at 3.1V. It should be driven in AC coupling. Analogue input is sampled and converted (10-bit) on each positive transition of the CLK input. Equivalent internal differential 100Ω input resistor.	I	
CLOCK INPUTS				
CLK CLKN	T6 R6	Master sampling clock input (differential) with internal common mode. It should be driven in AC coupling. Equivalent internal differential 100Ω input resistor.	I	

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Table 4-1. Pin Description (Continued)

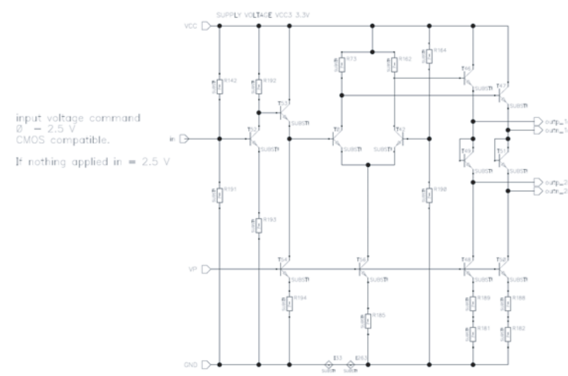
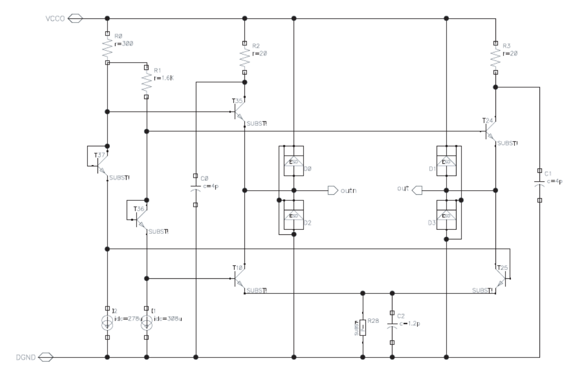
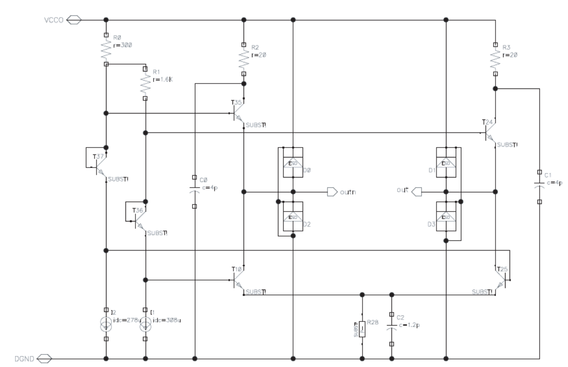
Signal Name	Pin Number	Description	Direction	Equivalent Simplified Schematics
RESET INPUT				
RSTN	T4	Reset input (single-ended). It is available in case it is necessary to reset the ADC during operation (it is not mandatory to perform an external reset on the ADC for proper operation of the ADC as a power up reset is already implemented). This reset is Asynchronous, it is 2.5 V CMOS compatible. It is active low. Refer to Section 2.8 and Section 5.4	I	
DIGITAL OUTPUTS				
A0, A0N A1, A1N A2, A2N A3, A3N A4, A4N A5, A5N A6, A6N A7, A7N A8, A8N A9, A9N	P1, P2 N1, N2 M1, M2 L3, M3 L1, L2 K1, K2 K3, J3 J1, J2 H1, H2 H3, G3	In-phase (Ai) and inverted phase (AiN) digital outputs on DEMUX Port A (with i = 0…9). Differential LVDS signal. A0 is the LSB, A9 is the MSB. The differential digital output data is transmitted at clock rate divided by the DMUX ratio (refer to RS0 and RS1 settings). Each of these outputs should be terminated by a 100Ω differential resistor placed as close as possible to the differential receiver.	O	
B0, B0N B1, B1N B2, B2N B3, B3N B4, B4N B5, B5N B6, B6N B7, B7N B8, B8N B9, B9N	F1, F2 E3, F3 E1, E2 D1, D2 A4, B4 A5, B5 C6, C5 A6, B6 A7, B7 C7, C8	In-phase (Bi) and inverted phase (BiN) digital outputs on DEMUX Port B (with i = 0…9). Differential LVDS signal. B0 is the LSB, B9 is the MSB. The differential digital output data is transmitted at clock rate divided by the DMUX ratio (refer to RS0 and RS1 settings). Each of these outputs should be terminated by a 100Ω differential resistor placed as close as possible to the differential receiver.	O	

Table 4-1. Pin Description (Continued)

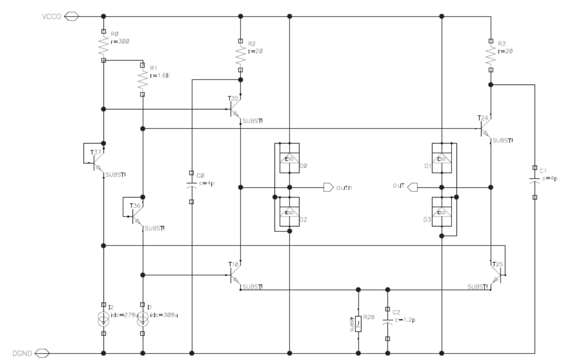
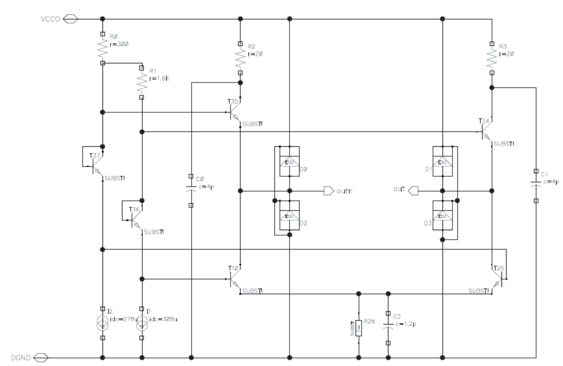
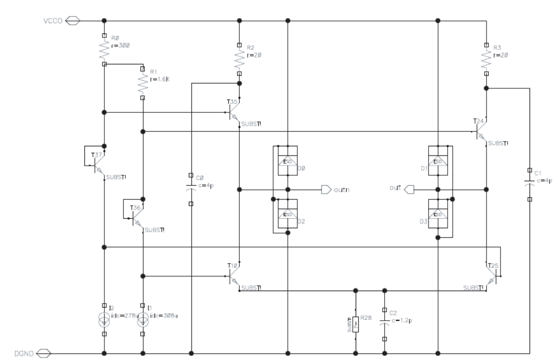
Signal Name	Pin Number	Description	Direction	Equivalent Simplified Schematics
C0, C0N C1, C1N C2, C2N C3, C3N C4, C4N C5, C5N C6, C6N C7, C7N C8, C8N C9, C9N	F16, F15 E14, F14 E16, E15 D16, D15 A13, B13 A12, B12 C11, C12 A11, B11 A10, B10 C10, C9	In-phase (Ci) and inverted phase (CiN) digital outputs on DEMUX Port C (with i = 0…9). Differential LVDS signal. C0 is the LSB, C9 is the MSB. The differential digital output data is transmitted at clock rate divided by the DMUX ratio (refer to RS0 and RS1 settings). Each of these outputs should be terminated by a 100Ω differential resistor placed as close as possible to the differential receiver.	O	
D0, D0N D1, D1N D2, D2N D3, D3N D4, D4N D5, D5N D6, D6N D7, D7N D8, D8N D9, D9N	P16, P15 N16, N15 M16, M15 L14, M14 L16, L15 K16, K15 K14, J14 J16, J15 H16, H15 H14, G14	In-phase (Di) and inverted phase (DiN) digital outputs on DEMUX Port D (with i = 0…9). Differential LVDS signal. D0 is the LSB, D9 is the MSB. The differential digital output data is transmitted at clock rate divided by the DMUX ratio (refer to RS0 and RS1 settings). Each of these outputs should be terminated by a 100Ω differential resistor placed as close as possible to the differential receiver.	O	
DR DRN	A9 B9	In-phase (DR) and inverted phase (DRN) global data ready digital output clock. Differential LVDS signal. The differential digital output clock is used to latch the output data on rising and falling edge. The differential digital output clock rate is (CLK/2) divided by the DMUX ratio (provided by RS0 and RS1 pins). This differential digital output clock should be terminated by a 100Ω differential resistor placed as close as possible to the differential receiver.	O	

Table 4-1. Pin Description (Continued)

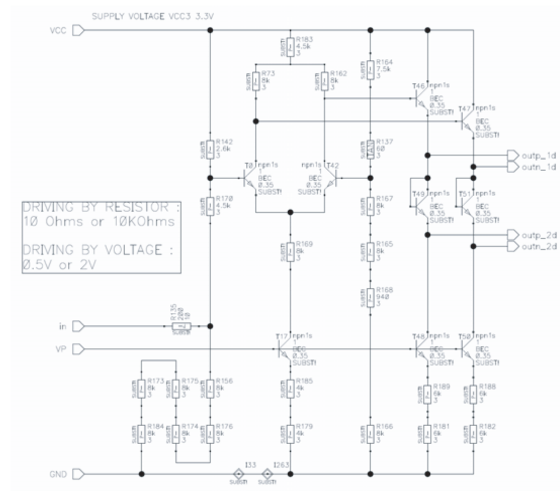
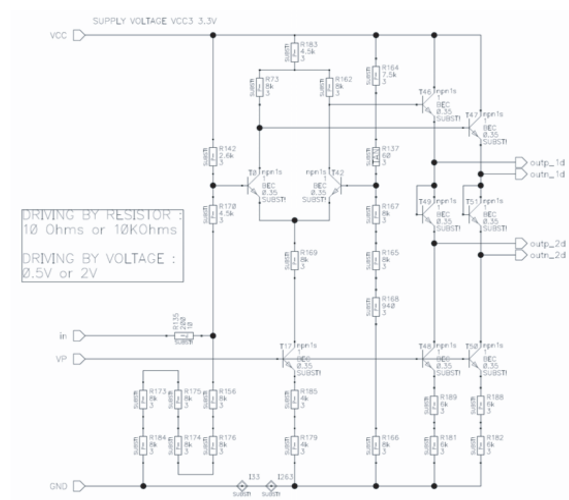
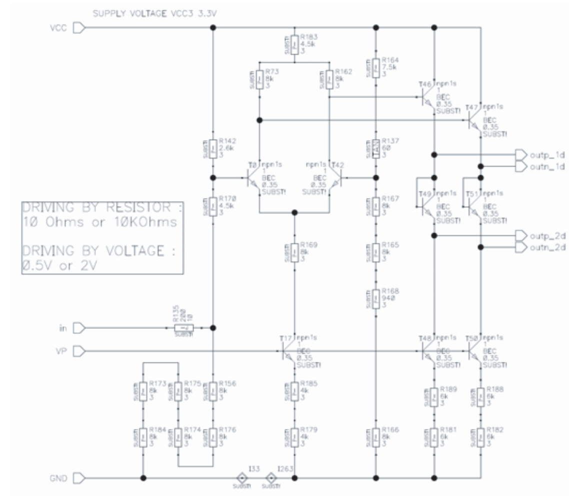
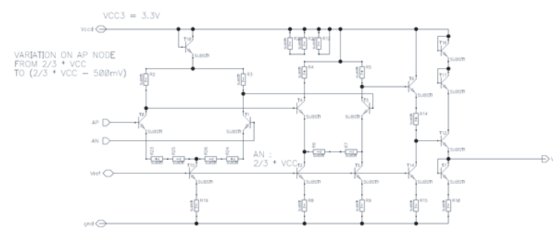
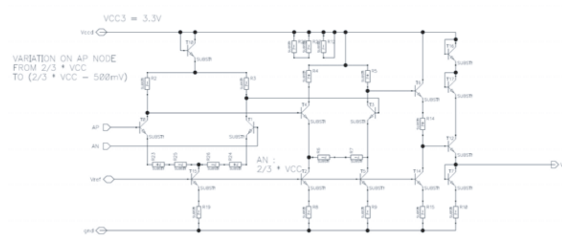
Signal Name	Pin Number	Description	Direction	Equivalent Simplified Schematics
ADDITIONAL FUNCTIONS				
DECN	N14	Decimation Function Enable (single-ended). Active low. Refer to Section 5.9 for more information.	I	
TM0, TM1	T14, R14	Test Mode. Refer to Section 5.3 for more information.	I	
RS0, RS1	T13, R13	DEMUX Ratio Selection. Refer to Section 5.2 for more information.	I	

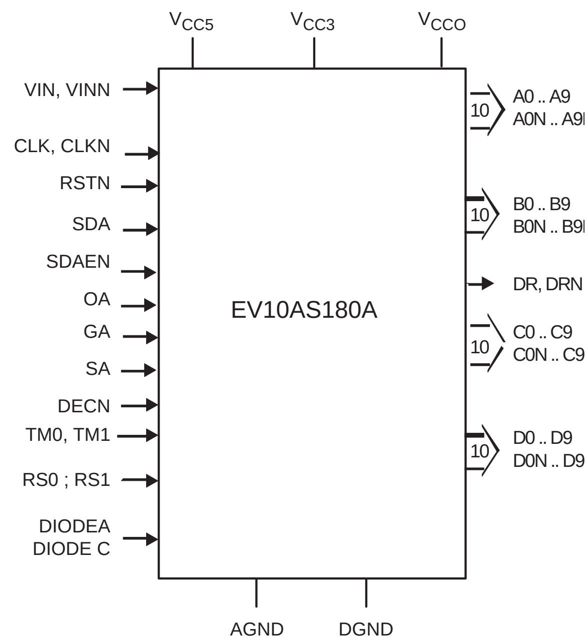
Table 4-1. Pin Description (Continued)

Signal Name	Pin Number	Description	Direction	Equivalent Simplified Schematics
SDAEN	R12	SDAEN = Sampling delay adjust enable. SDA = Sampling delay adjust. Please refer to Section 5.10 for more information.	I	
SDA	T12	SDAEN = Sampling delay adjust enable. SDA = Sampling delay adjust. Please refer to Section 5.10 for more information.	I	
GA	P4	**Gain Adjust.** Refer to Section 5.6 for more information.	I	
OA	N4	**Offset Adjust.** Refer to Section 5.7 for more information.	I	
SA	P14	**Swing adjust.** Refer to Section 5.8 for more information.	I	
DIODEA	P3	**Die Junction temperature monitoring** (DIODEA = anode, DIODEC = cathode). Please refer to Section 5.11 for more information.	I	
DIODEC	N3		O	
NC	A3, A8, A14 B3, B8, B14 C1, C2, C15, C16 G1, G2, G15, G16 M6, M11, M12 N6 R4, R5, T5	Not connected pins, connect to ground (DGND).	N/A	

5. FUNCTIONAL DESCRIPTION

Table 5-1. Function Descriptions

Name	Function
V_{CC5}	5.2V Power supply
V_{CC3}	3.3V Power supply
V_{CC0}	2.5V Power supply
AGND	Analog Ground
DGND	Digital Ground
V_{IN},V_{INN}	Differential Analog Input
CLK,CLKN	Differential Clock Input
[A0:A9] [A0N:A9N]	Differential Output Data on port A
[B0:B9] [B0N:B9N]	Differential Output Data on port B
[C0:C9] [C0N:C9N]	Differential Output Data on port C
[D0:D9] [D0N:D9N]	Differential Output Data on port D
DR,DRN	Global Differential Data Ready
SA	Analog tuning to adjust output swing
RS0; RS1	DEMUX Ratio select
RSTN	External reset
TM0, TM1	Test Mode pins
SDA	Sampling Delay Adjust input
SDAEN	Sampling Delay Adjust Enable
GA	Gain Adjust input.
OA	Offset adjust input
DECN	Decimation enable
DIODEA, DIODEC	Diode for die junction temperature monitoring



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5.1 Control Signal Settings

The RS0, RS1, TM0, TM1, SDAEN and DECN control signals use the same static input buffer.

Logic “1” (10 KΩ to Ground, or tied to V_{CC3} = 3.3V, or left floating) was chosen for the default modes:

a. 1:2 DMUX (RS1 = RS0 = “1”), please refer to section 3.2 for more information,
b. Test Mode off (TM0 = TM1 = “1”), please refer to section 3.3 for more information,
c. decimation off (please refer to section 3.8 for more information),
d. SDA off (please refer to section 3.9 for more information).

Figure 5-1. Control Signal Settings

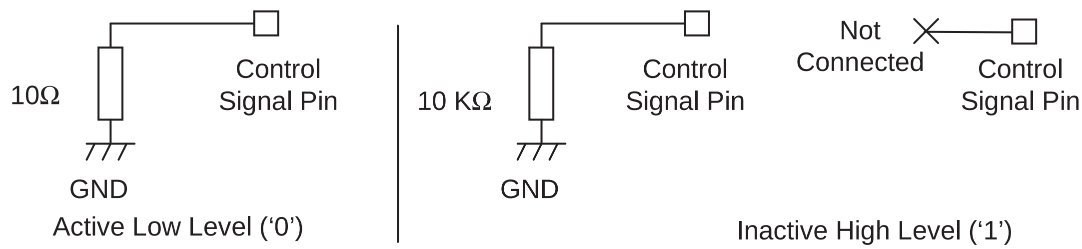


Table 5-2. ADC Mode Settings – Summary

Function	Logic Level	Electrical Level	Description
SDAEN	0	10Ω to ground or 0.5V	Sampling delay adjust enabled
	1	10 KΩ to ground or 2V	Sampling delay adjust disabled
		N/C	
DECN	0	10Ω to ground or 0.5V	Decimation by 8
	1	10 KΩ to ground or 2V	Normal conversion (no decimation)
		N/C	
RS<1:0>	01	RS1 : 10Ω to ground or 0.5V RS0 : 10 KΩ to ground or NC or 2V	1:1 DEMUX Ratio (Port A)
	11	RS1 : 10 KΩ to ground or NC or 2V RS0 : 10 KΩ to ground or NC or 2V	1:2 DEMUX Ratio (Ports A and B)
	10	RS1 : 10 KΩ to ground or NC or 2V RS0 : 10Ω to ground or 0.5V	1:4 DEMUX Ratio (Ports A, B, C and D)
	00	RS1 : 10Ω to ground or 0.5V RS0 : 10Ω to ground or 0.5V	Not used
TM<1:0>	01	TM1 : 10Ω to ground or 0.5V TM 0 : 10 KΩ to ground or NC or 2V	Static Test (all “0”s at the output for V_{OL} test)
	11	TM 1 : 10 KΩ to ground or NC or 2V TM 0 : 10 KΩ to ground or NC or 2V	Normal conversion mode (default mode)
	10	TM 1 : 10 KΩ to ground or NC or 2V TM 0 : 10Ω to ground or 0.5V	Static Test (all “1”s at the output for V_{OH} test)
	00	TM1 : 10Ω to ground or 0.5V TM0 : 10Ω to ground or 0.5V	Dynamic test (checker board pattern = all bits toggling from “0” to “1” or “1” to “0” every cycle with 1010101010 or 0101010101 patterns)

5.2 DEMUX Ratio Select (RS0, RS1) Function

Three DEMUX Ratios can be selected thanks to pins RS0 and RS1 according to the table below.

Table 5-3. Ratio Select Coding

RS<1:0>	01	1:1 DEMUX Ratio (Port A)
	11	1:2 DEMUX Ratio (Ports A and B)
	10	1:4 DEMUX Ratio (Ports A, B, C and D)
	00	Not used

ADC in 1:1 Ratio

Input Words: 1, 2, 3, 4, 5, 6, 7, 8...

1:1

Output Words:

Port A	1 2 3 ...
Port B	Not used
Port C	Not used
Port D	Not used

ADC in 1:2 Ratio

Input Words: 1, 2, 3, 4, 5, 6, 7, 8...

1:2

Output Words:

Port A	1 3 5 ...
Port B	2 4
Port C	Not used
Port D	Not used

ADC in 1:4 Ratio

Input Words: 1, 2, 3, 4, 5, 6, 7, 8...

1:4

Output Words:

Port A	1 5 9...
Port B	2 6
Port C	3 7
Port D	4 8

Notes:
1. Data of the different ports are synchronous: they appear at the same instant on each port.
2. Any used port should be terminated by a 100Ω differential resistor. Refer to Section 7.5 ”Digital Outputs” on page 38 for more information.
3. Any unused port can be left open (no external termination required).

5.3 Test Mode (TM0, TM1) Function

Two test modes are made available in order to test the 10-bit digital outputs of the ADC:

- a static test mode, where one can choose to output only “1”s or only “0”s;
- a dynamic test mode, where all bits toggle from “1” to “0” or from “0” to “1” every cycle, used to test the output transitions.

The coding table for the Test mode is given in Table 5-4.

Table 5-4. Test Mode Coding

TM<1:0>	01	Static Test (all “0”s at the 10-bit output for V_{OL} test)
	11	Normal conversion mode (default mode)
	10	Static Test (all “1”s at the 10-bit output for V_{OH} test)
	00	Dynamic test (checker board pattern = all 10 bits toggling from “0” to “1” or “1” to “0” every cycle with 1010101010 or 0101010101 patterns)

Note: The sequence should start with on port A, whatever the DMUX mode is.

Table 5-5. Test Mode

Cycle	DR	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0
N		0	1	0	1	0	1	0	1	0	1
N+1		1	0	1	0	1	0	1	0	1	0
N+2		0	1	0	1	0	1	0	1	0	1
N+3		1	0	1	0	1	0	1	0	1	0
N+4		0	1	0	1	0	1	0	1	0	1

5.4 External Reset (RSTN)

An external reset (RSTN) is available in case it is necessary to reset the ADC during operation (it is not mandatory to perform an external reset on the ADC for proper operation of the ADC as a power up reset is already implemented). This reset is 2.5V CMOS compatible. It is active low.

5.5 Power Up Reset

A power up reset ensures to synchronise internal signals and ensures output data to be properly ordered.

It is generated internally by the digital section of the ADC (on V_{CC3} power supply) and is de-activated when V_{CC5} reaches 80% of its steady state value. No sequencing is required on V_{CCO}.
If V_{CC3} is not applied before V_{CC5}, RSTN reset is strongly recommended to properly synchronise ADC signals.

Please refer to Section 2.8 ”Timing Diagrams” on page 13, Figure 2-4 for more information.

5.6 Gain Adjust (GA) Function

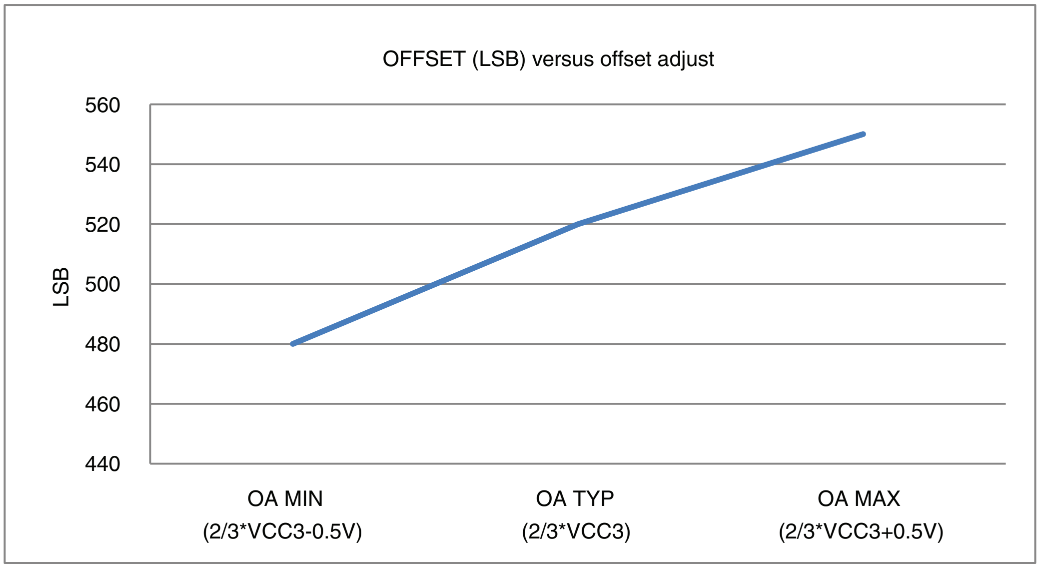
This function allows to adjust ADC Gain so that it can always be tuned to 1.0.
The ADC Gain can be tuned by ±10 % by tuning the voltage applied on GA by ±0.5V around $2*V_{CC3}/3$.

5.7 Offset Adjust (OA) Function

This function allows to adjust ADC Offset so that it can always be tuned to mid-code 512.

The ADC Offset can be tuned by ±40 LSB (±20mV) by tuning the voltage applied on OA by ±0.5V around 2*V_{CC3}/3.

Figure 5-2. Offset Versus Voltage Applied on OA



5.8 Swing Adjust (SA) Function

This function allows to reduce the nominal swing of the ADC in order to reduce power consumption in digital output buffers.

The nominal LVDS swing (250 to 450 mV) can be lowered (continuous tuning) to at least 100 mV by reducing the voltage applied on SA by –0.5V from middle value 2*V_{CC3}/3 (When SA is set at 2*V_{CC3}/3, the swing is a standard LVDS swing around 300 mV, when SA is set to 2*V_{CC3}/3 –0.5V, then swing is reduced to about 100 mV).

5.9 Decimation (DECN) Function

The decimation function has to be used for debug of the ADC at initial stages, and must not be used for standard operation. This function indeed allows to reduce the ADC output rate by 8 (assuming a 1:1 DEMUX Ratio), thus allowing for a quick debug phase of the ADC at max speed rate and is compatible with industrial testing environment.
When active, this function makes the ADC output only 1 out of 8 data, thus resulting in a data rate which is 8 times slower than the clock rate. In addition, DEMUX Ratio can be chosen in order to divide the data rate by 16 (1:2 mode) or by 32 (1:4 mode).

Note: the ADC Decimation Test mode is different from the Test Mode function, which can be used to check the ADC outputs

DECN is active at low level.

To deactivate the decimation mode, connect DECN to a high level by connecting it to V_{CC3} or by leaving DECN pin floating.

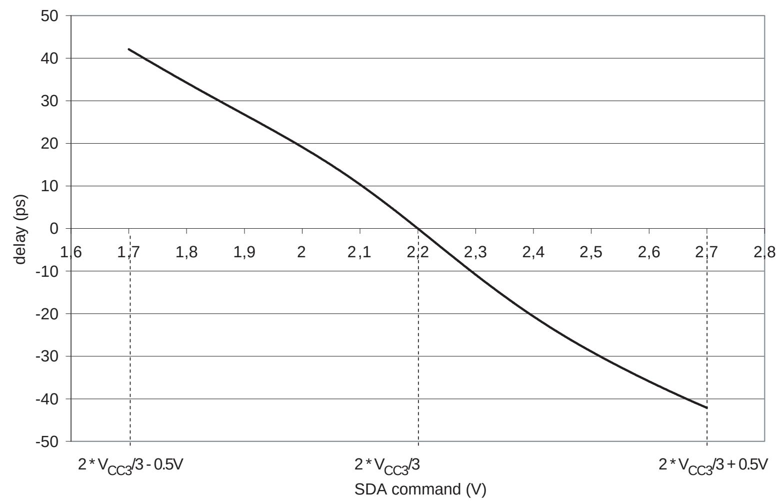
5.10 Sampling Delay Adjust (SDA) Function

Sampling delay adjust (SDA pin) allows to fine tune the sampling ADC aperture delay TA around its nominal value. This functionality is enabled thanks to the SDAEN signal, which is active at low level (when tied to ground) and inactive at high level (10 KΩ to Ground, or tied to V_{CC3} = 3.3V, or left floating).

This feature is particularly interesting for interleaving ADCs to increase sampling rate.

The variation of the delay around its nominal value as a function of the SDA voltage is shown in the following graph (simulation result):

Figure 5-3. Typical Tuning Range is ±40 ps for Applied Control Voltage Varying between ±0.5V around 2*V_{CC3}/3 on SDA Pin.



The variation of the delay in function of the temperature is negligible.

5.11 Temperature DIODE Function

A diode for die junction temperature monitoring is available in this ADC. It is constituted by an ESD diode. Both Anode and cathode of the diode are accessible externally.

In order to monitor the die junction temperature of the ADC, a current of 1mA has to be applied on the DIODEA pin (anode of the diode). The voltage across the DIODEA pin and the DIODEC pin provides the junction temperature of the die thanks to the intrinsic diode characteristics provided in Figure 5-5.

It is recommended to use three protection diodes to avoid any damage due to over-voltages to the internal diode.
The recommended implementation is provided in Figure 5-4.

Figure 5-4. Temperature DIODE Implementation

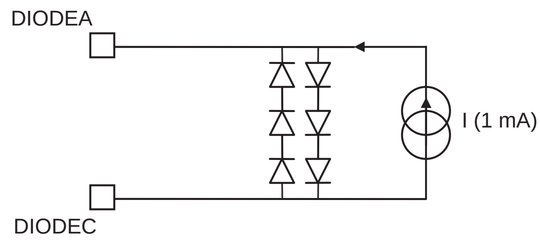
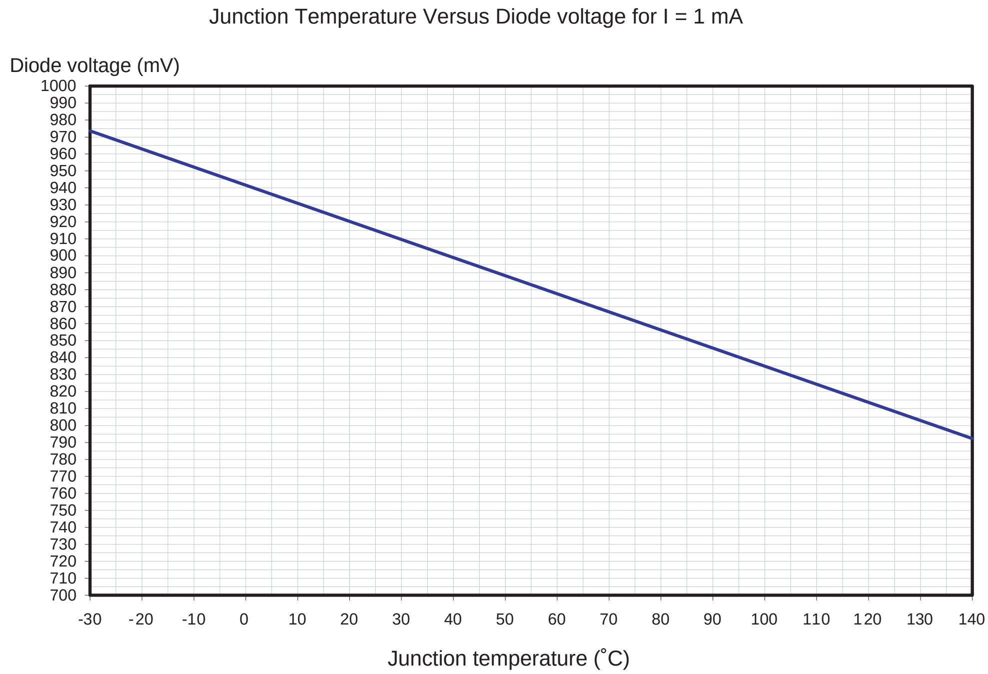
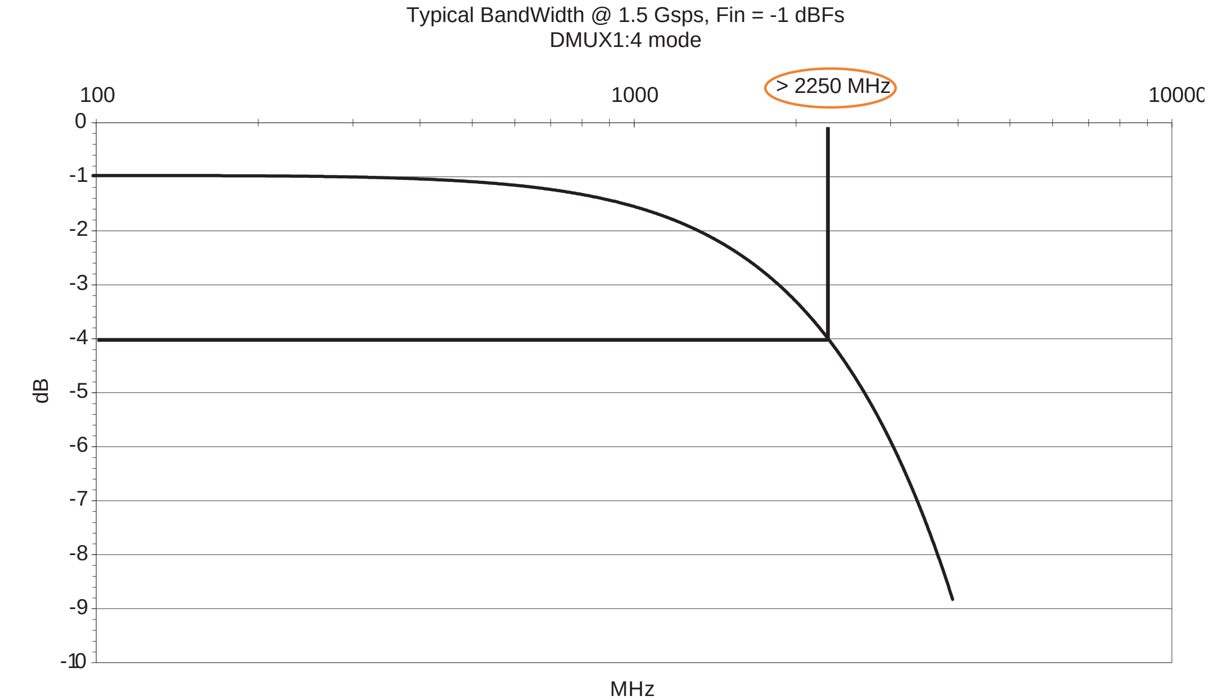


Figure 5-5. Temperature DIODE Characteristics

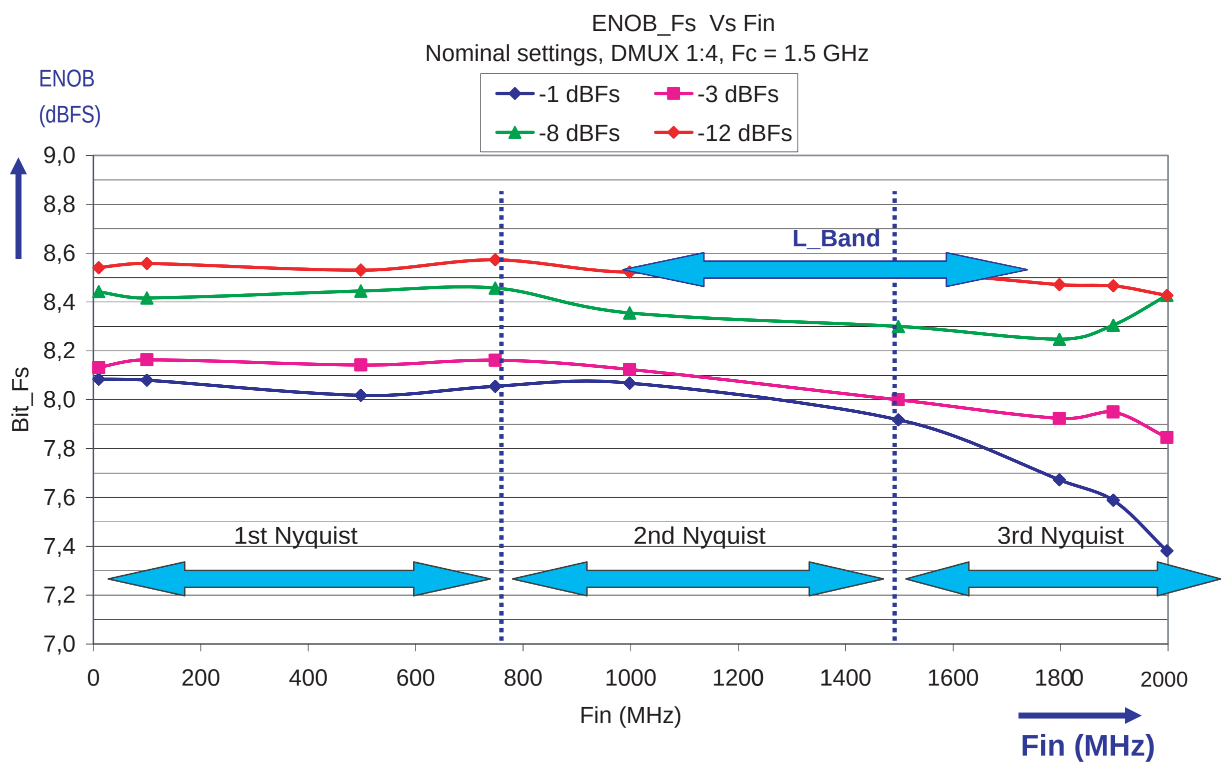


6. CHARACTERIZATION RESULTS

6.1 Input Bandwidth @ Fs = 1.5 GSps



6.2 Single Tone FFT Computation Versus Fin @ 1.5GSps



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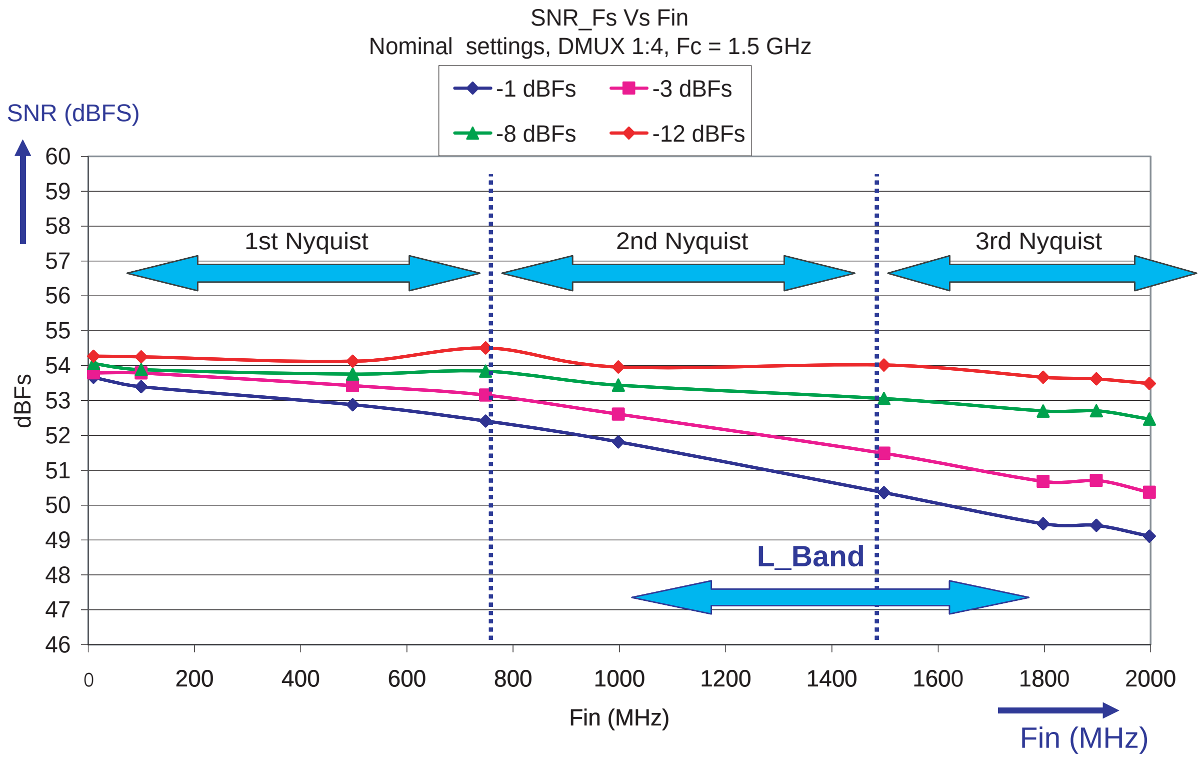
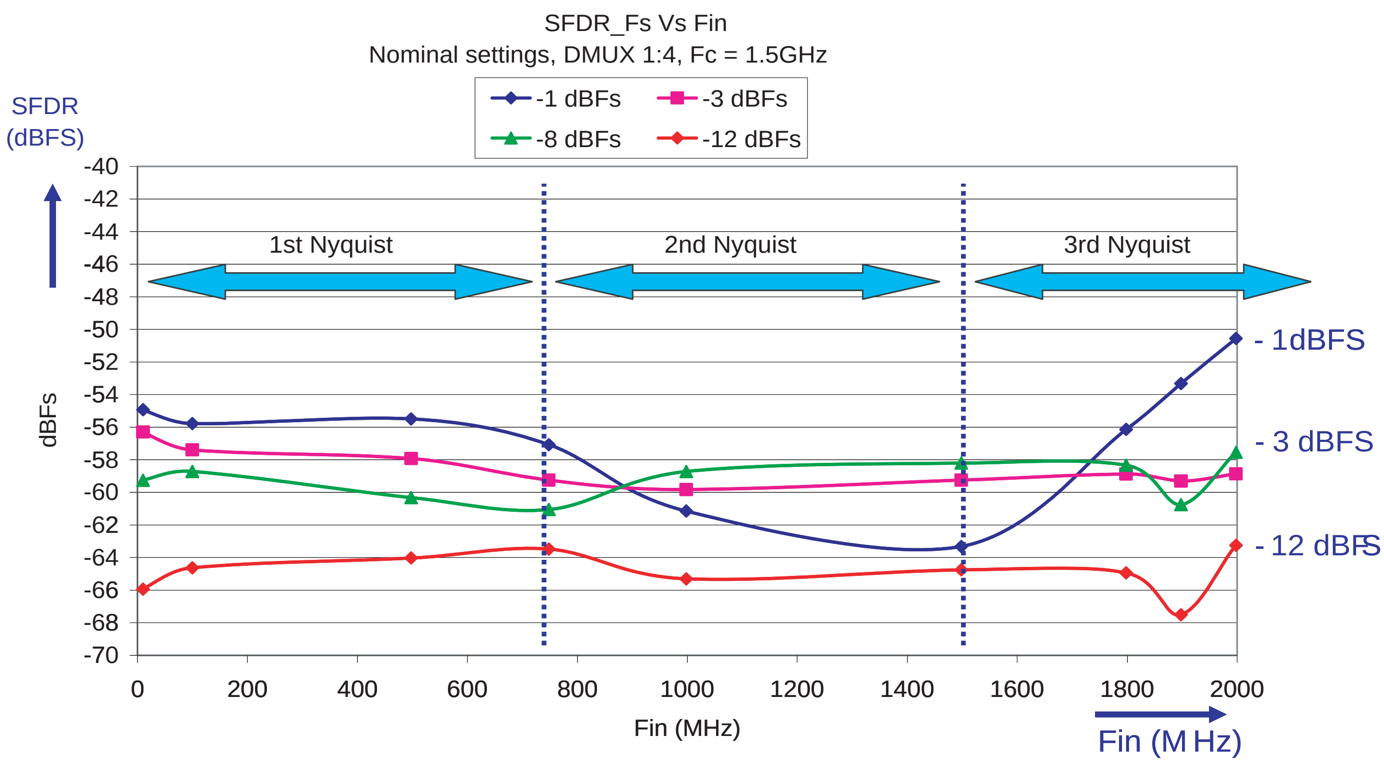
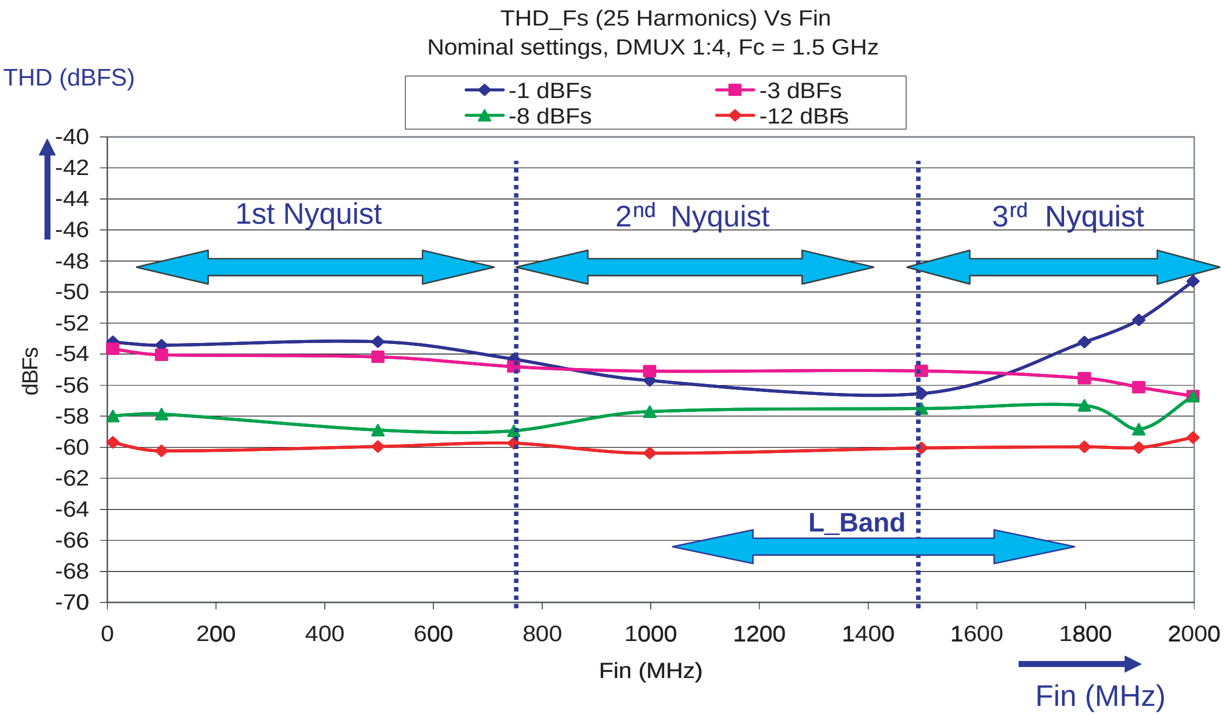
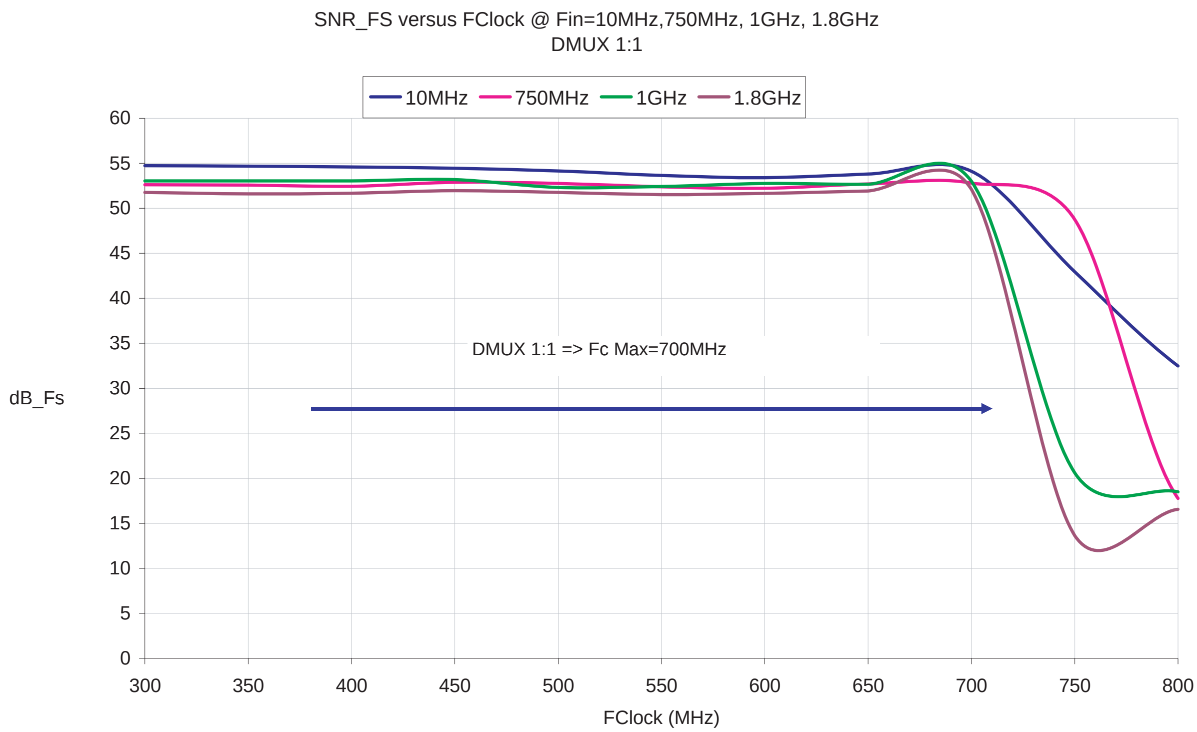
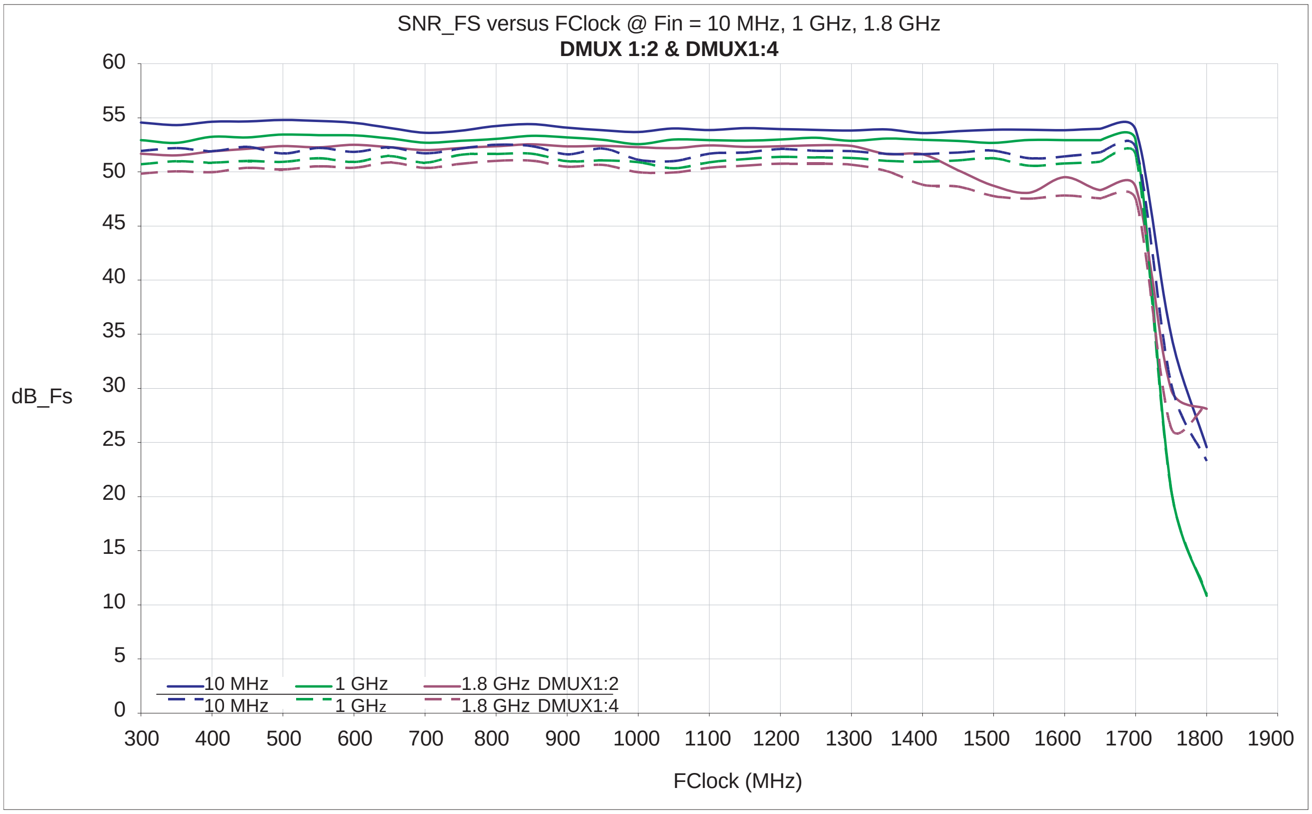

SNR_Fs Vs Fin
Nominal settings, DMUX 1:4, Fc = 1.5 GHz
-1 dBFs
-3 dBFs
-8 dBFs
-12 dBFs
SNR (dBFS)
dBFs
1st Nyquist
2nd Nyquist
3rd Nyquist
L_Band
Fin (MHz)
Fin (MHz)


SFDR_Fs Vs Fin
Nominal settings, DMUX 1:4, Fc = 1.5GHz
-1 dBFs
-3 dBFs
-8 dBFs
-12 dBFs
SFDR
(dBFS)
dBFs
1st Nyquist
2nd Nyquist
3rd Nyquist
- 1dBFS
- 3 dBFS
- 12 dBFS
Fin (MHz)
Fin (M Hz)



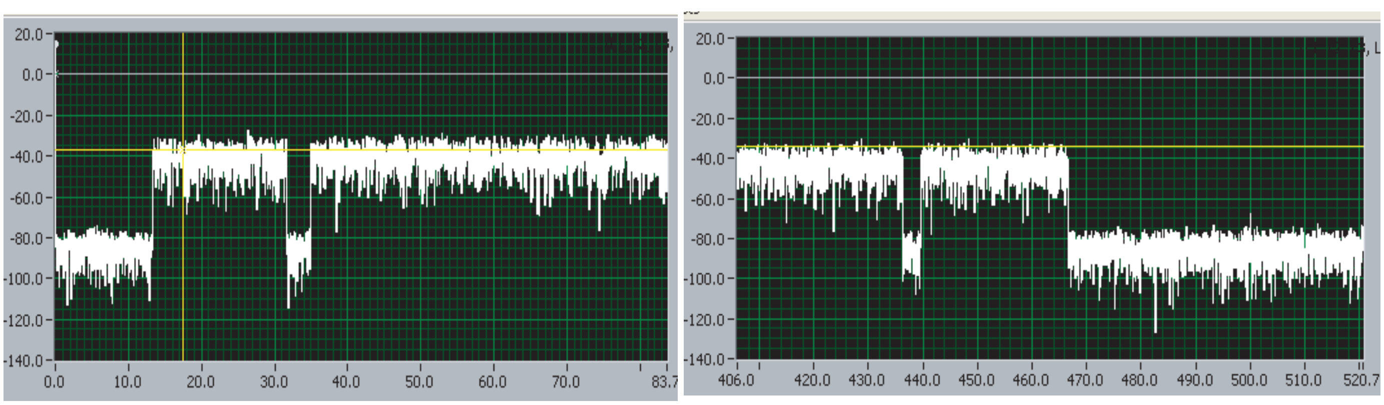
6.3 Single Tone FFT Computation Versus Fs





6.4 Broadband Performances, Noise Power Ratio

1,5 GSps 1st Nyquist NPR at Optimum loading factor –13 dBFS (450 MHz Pattern, 5 MHz Notch around 33 MHz & 438 MHz : NPR = 44 dB

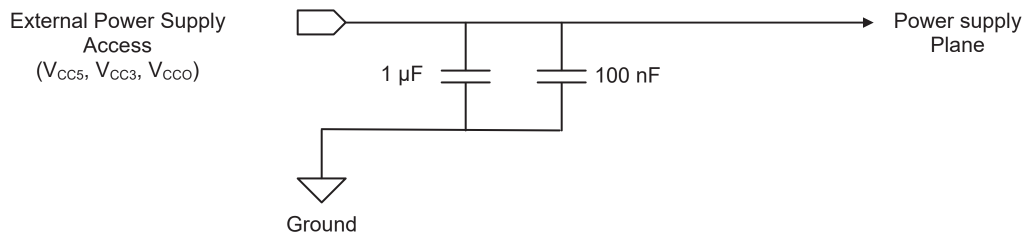


7. APPLICATION INFORMATION

7.1 Bypassing, Decoupling and Grounding

All power supplies have to be decoupled to ground as close as possible to the signal accesses to the board by 1 µF in parallel to 100 nF.

Figure 7-1. EV10AS180A Power Supplies Decoupling and Grounding Scheme

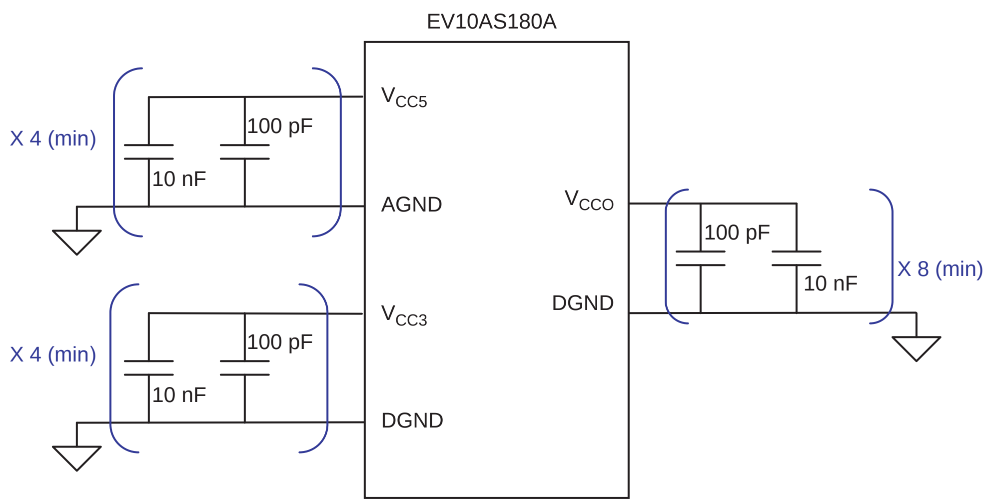


Each group of neighboring power supply pins attributed to the same value should be bypassed with at least one pair of 100 pF in parallel to 10 nF capacitors. These capacitors should be placed as close as possible to the power supply package pins.

The minimum required number of pairs of capacitors by power supply type is:

4 for V_{CC5}
4 for V_{CC3}
8 for V_{CCO}

Figure 7-2. EV10AS180A Power Supplies Bypassing Scheme



Each power supply has to be bypassed as close as possible to its source or access by 100 nF in parallel to 1 µF capacitors.

7.2 Power-up Sequencing

In case the power supplies implemented do not short their outputs to GND during their power-up, no power-up sequence on the ADC is required.

In case the power supplies implemented are shorting their outputs to GND during their power-up, power-up sequence is required for the ADC and the following two power-up sequences are possible:

- VCC3 -> VCCO -> VCC5
- VCC3 -> VCC5 -> VCCO

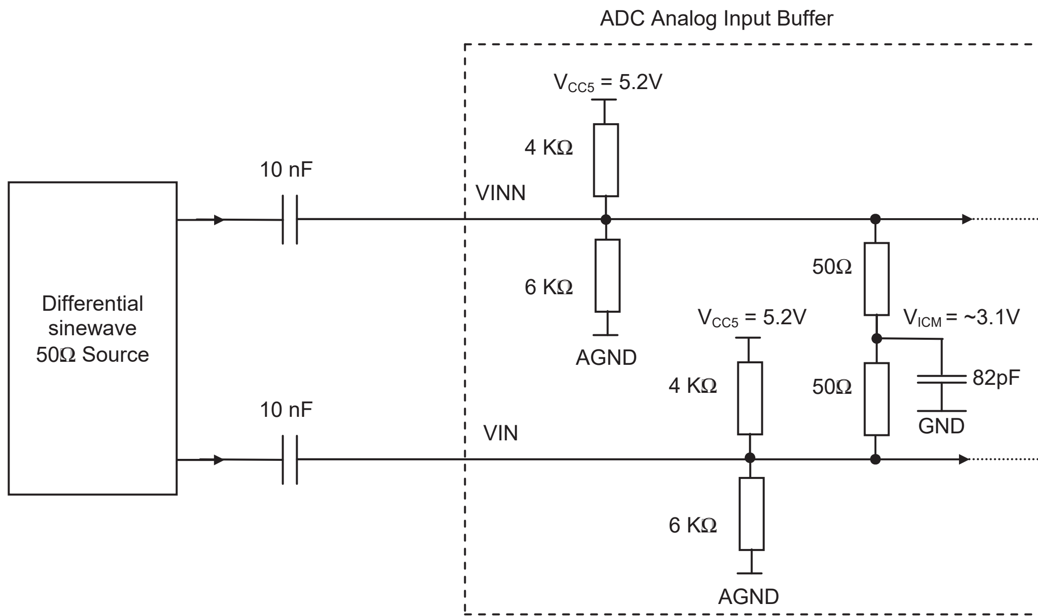
7.3 Analog Inputs (VIN/VINN)

The analog input should be used in differential mode. If a single-ended source is used, then a balun (transformer) should be implemented to convert the signal to a differential signal at the input of the ADC.

7.3.1 Differential Analog Input

The analog input should be AC coupled as described in Figure 7-3.

Figure 7-3. Differential Analog Input Implementation (AC Coupled)

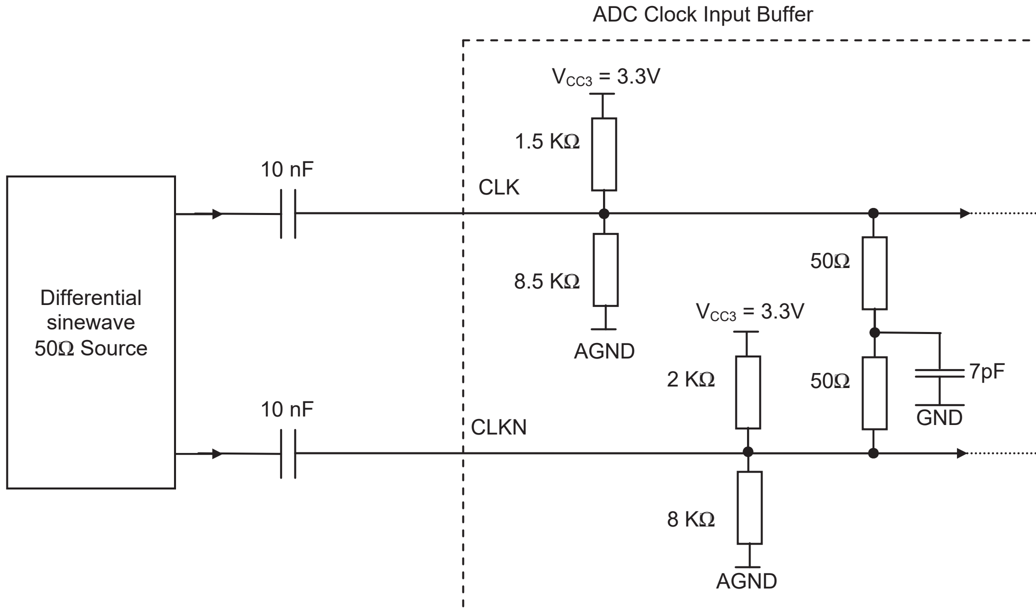


7.4 Clock Inputs (CLK/CLKN)

Differential mode is the recommended input scheme. Single-ended clock input is not recommended due to performance limitations. If a single-ended source is used, then a balun (transformer) should be implemented to convert the signal to a differential signal at the input of the ADC.

We recommend to AC couple the input clock as described in Figure 7-4.

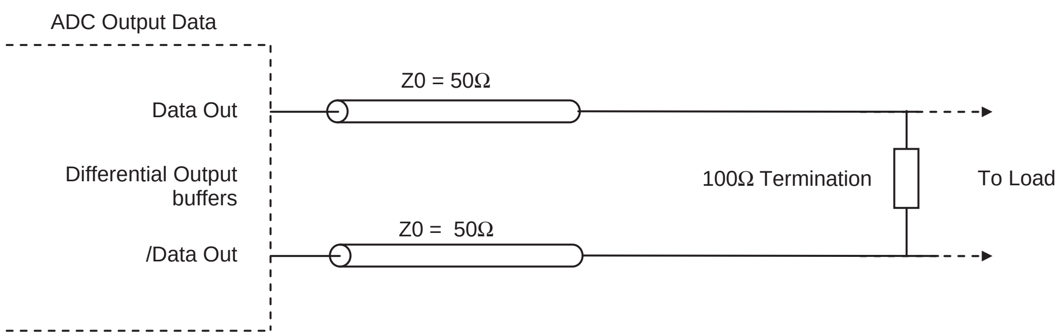
Figure 7-4. Differential Clock Input Implementation (AC Coupled)



7.5 Digital Outputs

The digital outputs are LVDS compatible. They have to be 100Ω differentially terminated.

Figure 7-5. Differential Digital Outputs Terminations (100Ω LVDS)



If the ADC is used in 1:1 or 1:2 DMUX modes, the unused ports can be left open (no external termination required).

8. THERMAL CHARACTERISTICS

Typical Assumptions

- Die thickness = 300 µm
- No convection
- Pure conduction
- No radiation

R_{TH}	Heating zone	Ci CGA	CCGA	Unit
Junction-> Bottom of columns	18% die area : 4820x4820 µm	10.5	11.7	°C/W
Junction-> Board (JEDEC JESD51-8) Boad size = 39x39mm, 1.6 mm Thickness)		13.7	15.2	°C/W
Junction -> Top of Lid		16.0	18.4	°C/W
$T_{jhot\ spot} – T_{Jdiode}$		2.2	2.2	°C/W

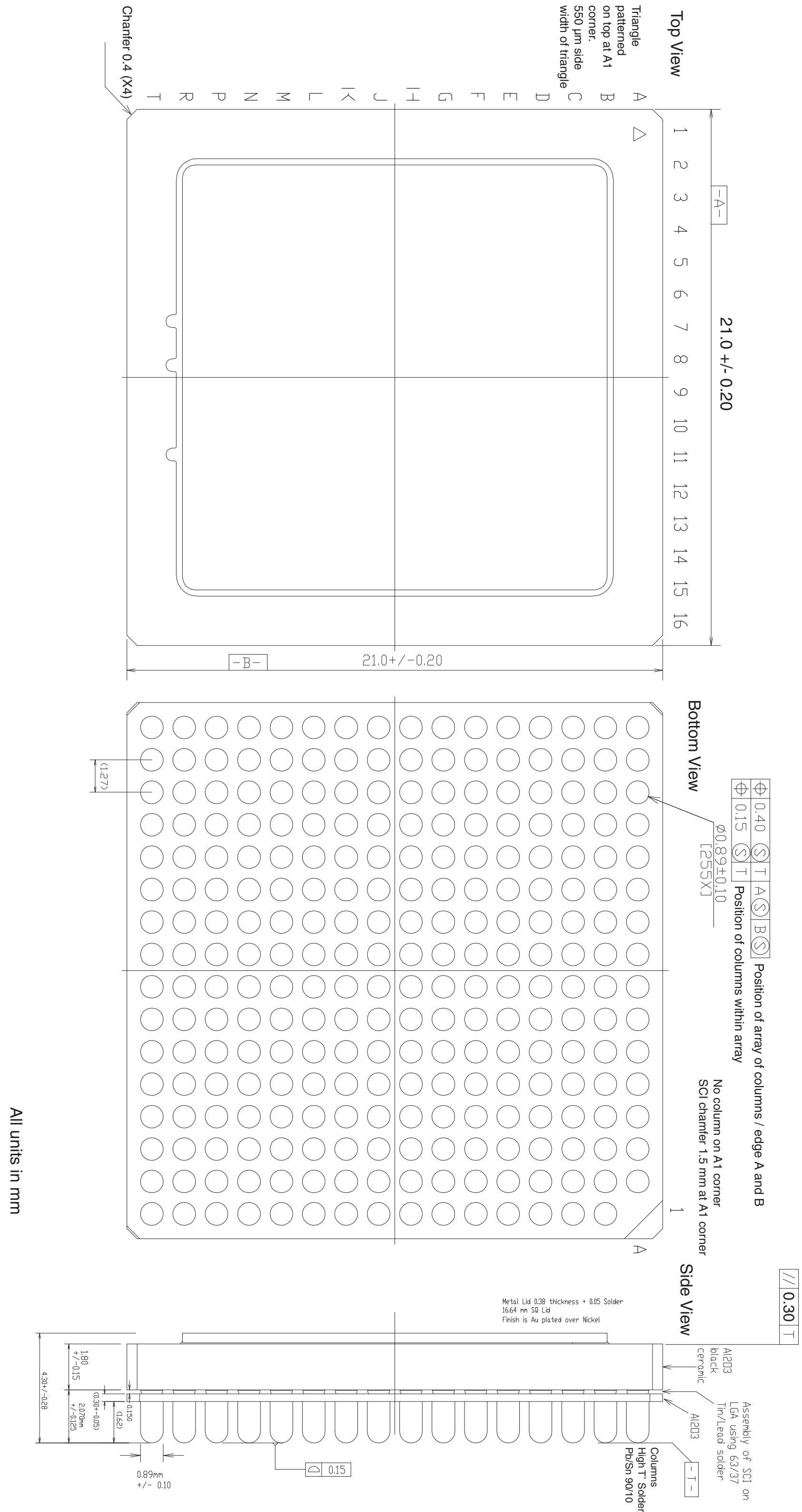
Typical Assumptions:

- Convection according to JEDEC
- Still air
- Horizontal 2s2p board
- Board size 114.3 × 76.2 mm, 1.6 mm thickness

R_{TH}	Heating zone	Ci CGA	CCGA	Unit
Junction -> Ambient	18% die area : 4820x4820 µm	26.0	26.0	°C/W
$T_{jhot\ spot} – T_{Jdiode}$		2.2	2.2	°C/W

9. PACKAGE DESCRIPTION

9.1 Ci-CGA255 Outline



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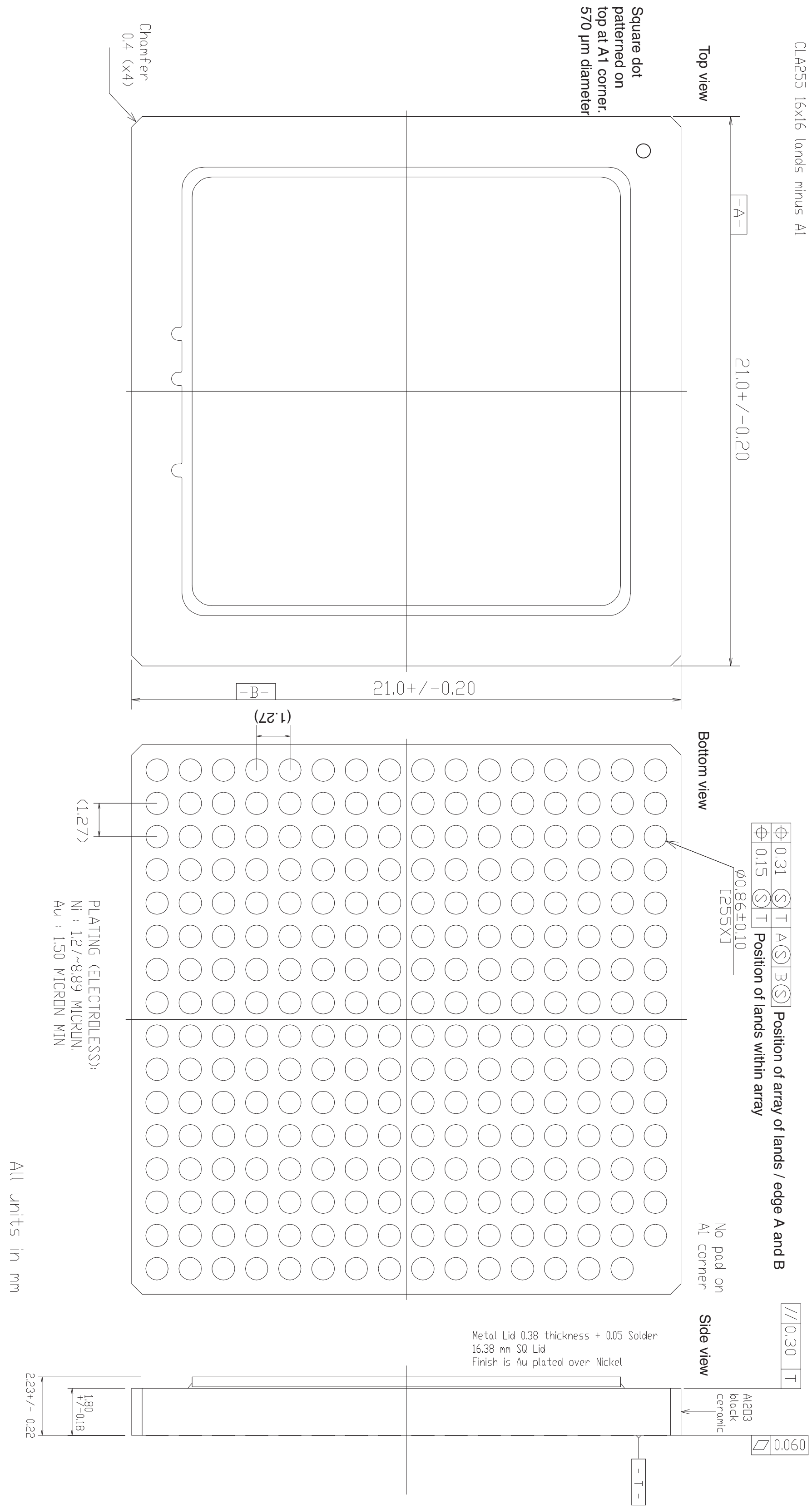
9.2 CLGA255 Outline



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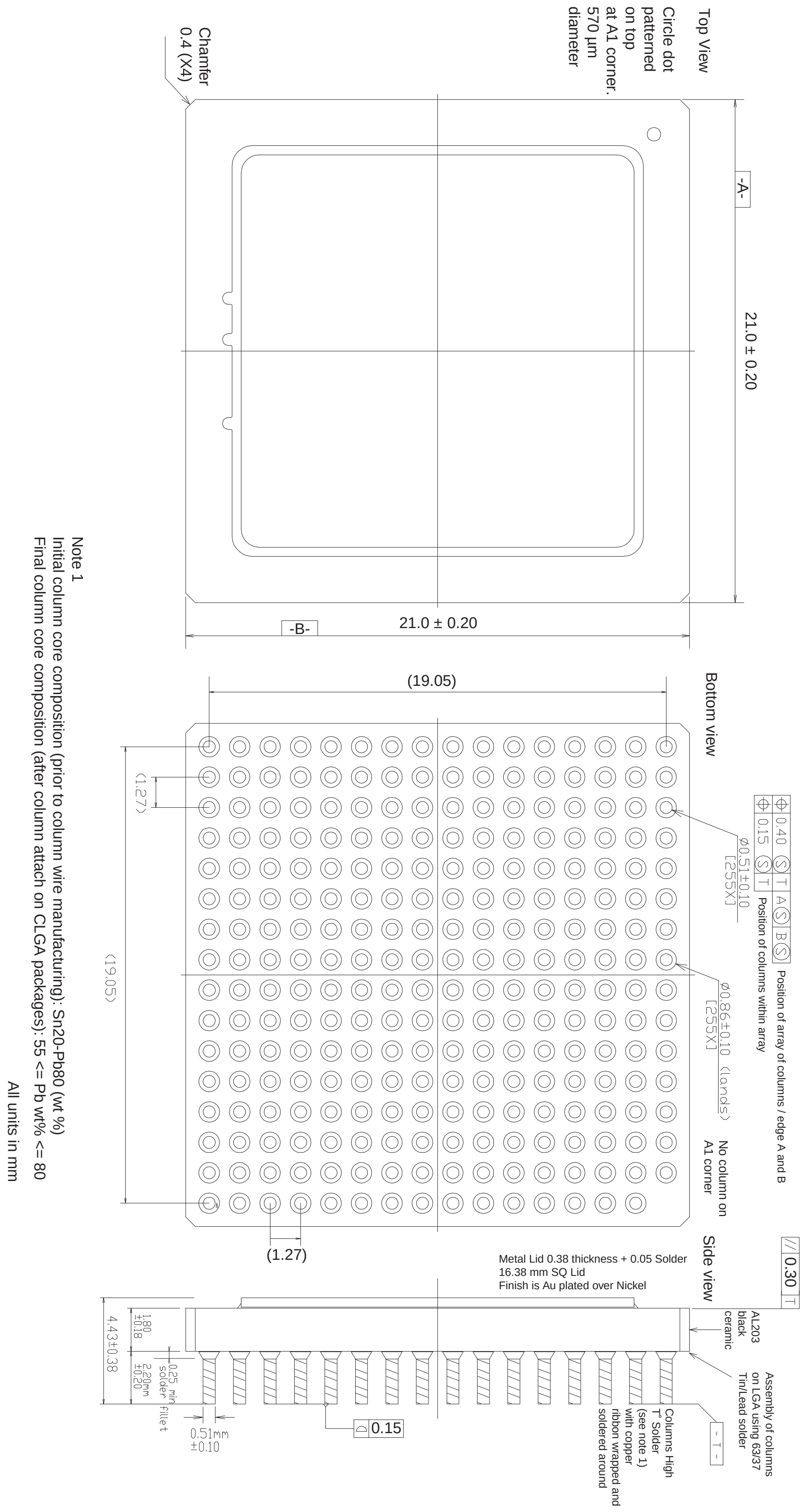
9.3 CCGA255 Outline



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10. ORDERING INFORMATION

Table 10-1. Ordering Information

Part Number	SMD Number	Package	Temperature Range	Screening Level	Comments
EVX10AS180AGS		CI-CGA255	Ambient	Prototype	
EV10AS180AMGSD/T		CI-CGA255	–55°C < Tc, Tj < 125°C	D/T Grade	
EV10AS180AMGS9NB1		CI-CGA255	–55°C < Tc, Tj < 125°C	Space Grade	
EV10AS180AGS-EB		CI-CGA255	Ambient	Prototype	Evaluation board
EVX10AS180ALG		LGA255	Ambient	Prototype	
EV10AS180AMLGD/T		LGA255	–55°C < Tc,Tj < 125°C	D/T Grade	
EV10AS180AMLG9NB1		LGA255	–55°C < Tc,Tj < 125°C	Space Grade	
EVX10AS180AGC		CCGA255	Ambient	Prototype	
EV10AS180AMGCD/T		CCGA255	–55°C < Tc,Tj < 125°C	D/T Grade	
EV10AS180AMGC9NB1		CCGA255	–55°C < Tc,Tj < 125°C	Space Grade	
EV10AS180AMLG-V	5962-1522301VXC	LGA255	–55°C < Tc,Tj < 125°C	QML-V Grade MIL PRF 38535	
EV10AS80AMGS-V	5962-1522301VYF	CI-CGA255	–55°C < Tc,Tj < 125°C	QML-V Grade MIL PRF 38535	
EV10AS180AMGC-V	5962-1522301VZF	CCGA255	–55°C < Tc,Tj < 125°C	QML-V Grade MIL PRF 38535S	

11. DOCUMENT REVISION HISTORY

Table 11-1. Document Revision History

Revision Number	Date	Substantive Change(s)
DS 60S 221991(G)	04/22	Change of the document reference Section ”” on page 42 Updated
F	06/19	Add Section 7.2 ”Power-up Sequencing” on page 37
E	11/15	Introduction of QML-V grade
D	06/14	- Correction of typo - Modification of limits for RIN & RCLK - INL and DNL have only typical values - Section 2.1 on page 4 and Section 2.2 on page 5: add duration about power-up sequencing - Section 2.6 on page 10: remove information about ELDRS - Section 2.7 on page 11: modification of TOD-TDR values - Section 2.7 on page 11: TDR is maximum value - Section 2.8 on page 13: corrections of some typo in timing diagrams - Section 3. on page 17: Modification of TD1 & TD2, TOD & TDR definitions - Section 3. on page 17: add TRDR definition - Section 5.7 on page 29: insertion of a figure - Section 9.3 on page 42: add note about column composition
C	07/13	Section 9. ”Package Description” on page 40: add CCGA and LGA package description and part number
B	03/13	Section 8. ”Thermal Characteristics” on page 39 updated Table 2-6, “Timing Characteristics and Switching Performances,” on page 11 updated
A	01/13	Initial revision

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Mailing Address: Teledyne e2v Semiconductors SAS, Avenue de Rochepleine, 38120 Saint Egrève, France.

Telephone: +33 4 76 58 30 00

e-mail: hotline-std@teledyne.com