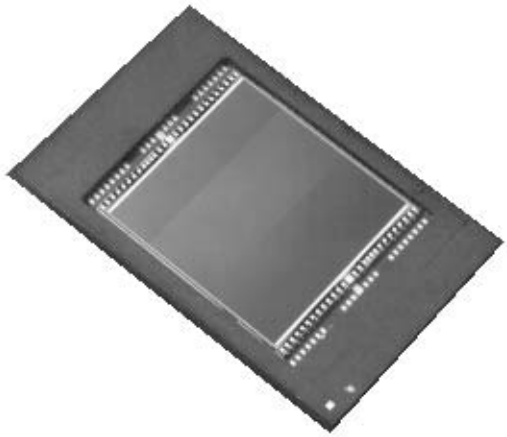
e2v technologies

CCD55-30 Inverted Mode Sensor
High Performance CCD Sensor

FEATURES

- 1252 (H) by 1152 (V) Pixel Format
- 28 by 26 mm Active Area
- Visible Light and X-Ray Sensitive
- New Improved Very Low Noise Amplifier for Slow-Scan Systems and Large Signal Amplifier for Binned Operation
- Symmetrical Anti-Static Gate Protection
- Radiation Tolerant
- Advanced Inverted Mode Operation
- Gated Dump Drain on Output Register



INTRODUCTION

The CCD55-30 is one of the CCD55 range of very large area CCD image sensors primarily intended to suit the requirements of astronomy, medical diagnostic and scientific measuring instruments. Standard three-phase clocking and buried channel charge transfer are employed. The device operates in the inverted mode for minimum dark current. The readout register has a high performance low noise amplifier at one end for slow-scan applications and a high speed amplifier at the other end. The image area is split into two sections which can be clocked separately for frame transfer operation.

The CCD55-30 is an upgraded version of the CCD05-30 with improved output amplifiers and is also available in backthinned format. The CCD55-30 is pin compatible with the CCD05-30, except that the top two amplifiers are not provided.

The CCD55-30 scientific image sensor is primarily specified for operation in a full-frame imaging mode with slow-scan readout from the whole image area through the low noise amplifier and is tested at a temperature of approximately 253 K.

Other operating modes are also possible, including use of the large signal amplifier (but at higher noise) and pixel binning. Potential users are invited to discuss their applications with e2v technologies to ensure optimum performance.

In common with all other e2v technologies CCD sensors, the CCD55-30 is available with a fibre-optic window or taper, a UV coating or a phosphor coating for hard X-ray detection.

Designers are advised to consult e2v technologies should they be considering using CCD sensors in abnormal environments or if they require customised packaging.

TYPICAL PERFORMANCE
(Low noise amplifier)

Pixel readout frequency	20 – 6000	kHz
Output amplifier sensitivity	3	$\mu V/e^-$
Peak signal	400	ke^-/pixel
Dynamic range	133 000:1	
Spectral range	420 – 1060	nm
Readout noise (at 253 K, 20 kHz)	3	e^- rms
Q.E. at 700 nm	45	%
Peak output voltage	1.2	V

GENERAL DATA

Format

Image region (section A)	1252(H) x 576(V)	pixels
Image region (section B)	1252(H) x 576(V)	pixels
Image area (sections A + B)	28.17 x 25.92	mm
Pixel pitch (row and column)	22.5 x 22.5	µm

Package

Outline dimensions	53.3 x 33.0 mm
Number of pins	44
Inter-pin spacing	2.54 mm
Inter-row spacing	2.54 mm
Inner row spacing (across sensor)	43.18 mm
Window	removable glass
Mounting position	any

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411/9572

PERFORMANCE

	Min	Typical	Max	
Peak charge storage (see note 1)	300k	400k	-	e^-/pixel
Peak output voltage (unbinned):				
low noise amplifier	-	1.2	-	V
large signal amplifier	-	0.48	-	V
Dark signal at 293 K (see notes 2 and 3)	-	200	400	e^-/pixel/s
Charge transfer efficiency (see note 4):				
parallel	-	99.9999	-	%
serial	-	99.9993	-	%
Output amplifier sensitivity:				
low noise amplifier	2.0	3.0	4.0	$\mu V/e^-$
large signal amplifier	0.8	1.2	1.6	$\mu V/e^-$
Readout noise at 253 K (see notes 3 and 5)				
low noise amplifier, A2	-	3	5	rms e^-/pixel
large signal amplifier, A1	-	8	-	rms e^-/pixel
Readout frequency (see note 6):				
low noise amplifier	-	50	6000	kHz
large signal amplifier	-	1000	6000	kHz
Response non-uniformity (std. deviation)	-	1	3	% of mean
Dark signal non-uniformity at 293 K (see notes 3 and 7) (std. deviation, σ)	-	80	160	e^-/pixel/s
Output node capacity:				
low noise amplifier, A2	-	600	-	ke^-
large signal amplifier, A1	-	1300	-	ke^-

ELECTRICAL INTERFACE CHARACTERISTICS

	Min	Typical	Max	
Electrode capacitances (measured at mid-clock level):				
A∅ or B∅ interphase	-	4.2	-	nF
C∅ interphase	-	110	-	pF
A∅1, B∅1 to SS	-	21	-	nF
A∅2, A∅3, B∅2, B∅3 to SS	-	8.4	-	nF
C∅, each phase to SS/DD/DG (see note 8)	-	300	-	pF
Output impedances:				
Low noise amplifier (A2)	-	400	-	Ω
Large signal amplifier (A1)	-	250	-	Ω

NOTES

1. Signal level at which resolution begins to degrade.
2. The typical average (background) dark signal at any temperature T (kelvin) between 230 and 300 K is given by:

   $$Q_d/Q_{d0} = 1.14 \times 10^6 T^3 e^{-9080/T}$$

   where Q_{d0} is the dark current at 293 K. Note that this is typical performance and some variation may be seen between devices. Below 230 K additional dark current components with a weaker temperature dependence may become significant.
3. This test is carried out on all CCD55-30 sensors.
4. CCD characterisation measurements made using charge generated by X-ray photons of known energy.
5. Measured using a dual-slope integrator technique (i.e. correlated double sampling) with a 10 μs integration period.
6. Readout above the values specified may be achieved but performance to the parameters given cannot be guaranteed.
7. Measured between 253 and 293 K, excluding white defects.
8. Capacitances when $V_{SS} > 8$ V.

BLEMISH SPECIFICATION

Traps Pixels where charge is temporarily held. Traps are counted if they have a capacity greater than 200 e^- at 253 K.

Slipped columns Are counted if they have an amplitude greater than 200 e^-.

Black spots $>10\%$ contrast at half saturation, 253 K.

White spots Are counted when they have a generation rate 50 times the specified maximum dark signal generation rate at 293 K (measured between 233 and 273 K). The typical temperature dependence of white spot blemishes is different from that of the average dark signal and is given by:

$$Q_d / Q_{d0} = 122T^3 e^{-6400/T}$$

White column A column which contains at least 9 white defects.

Black column A column which contains at least 9 black defects.

GRADE	0	1	2
Column defects:			
black or slipped	0	2	6
white	0	0	0
Traps >200 e^-	2	5	12
White spots	42	42	65
Black spots	20	40	200

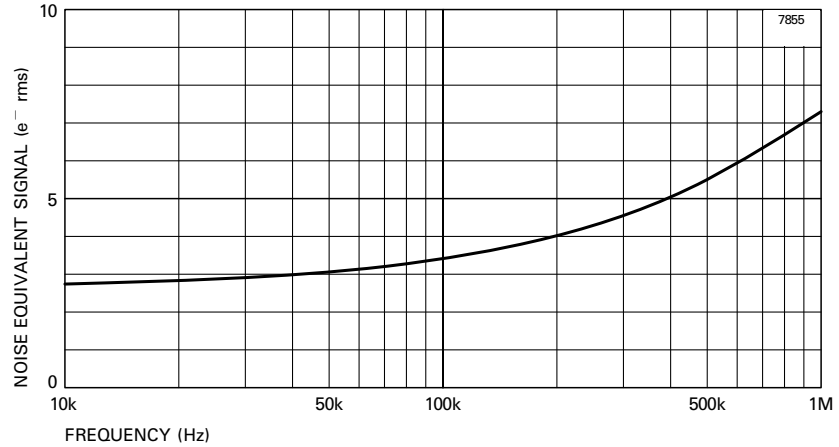
Grade 5 Devices which are fully functioning but with image quality below that of grade 2 and which may not meet all other performance parameters.

Minimum separation between
adjacent black columns . . . . . 50 pixels

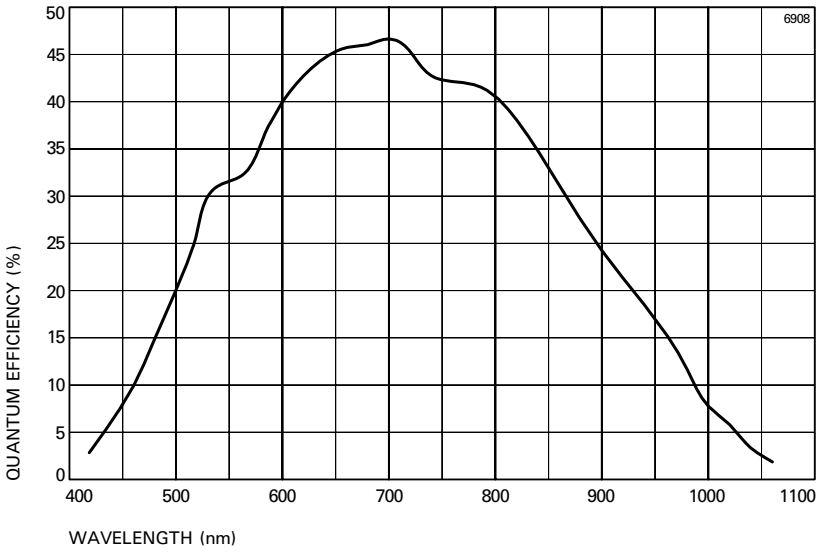
Note The effect of temperature on defects is that traps will be less noticeable at higher temperatures but more may appear below 253 K. The amplitude of white spots and columns will decrease rapidly with temperature.

TYPICAL OUTPUT CIRCUIT NOISE

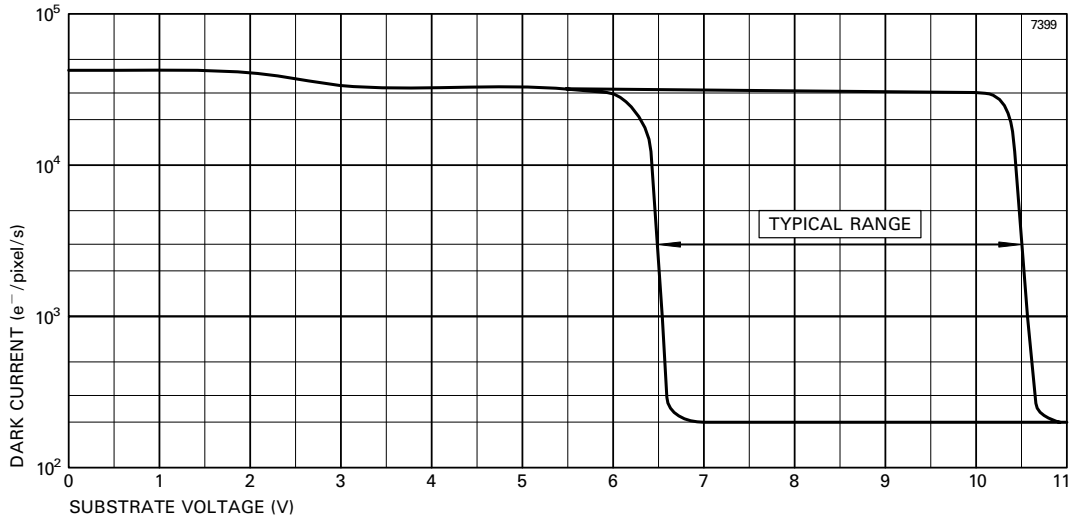
(Low noise amplifier, measured using clamp and sample)



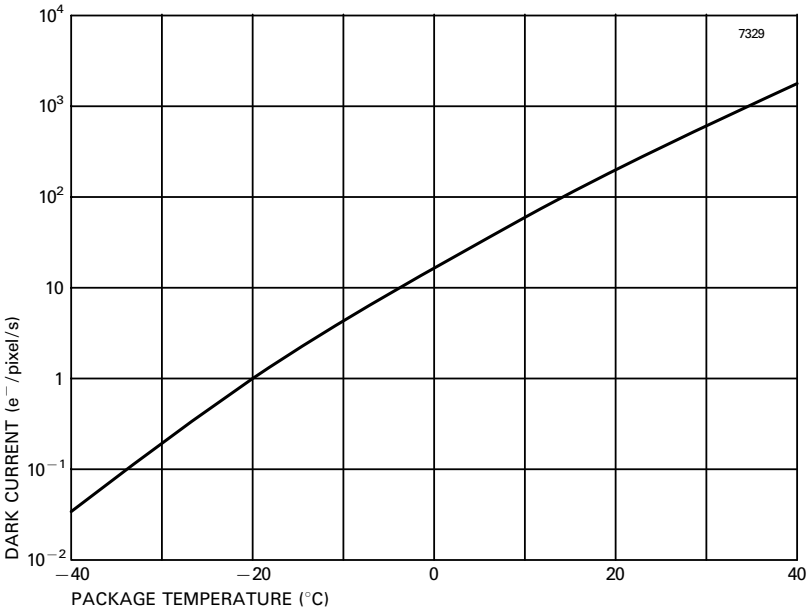
TYPICAL SPECTRAL RESPONSE (No window)



TYPICAL VARIATION OF DARK SIGNAL WITH SUBSTRATE VOLTAGE

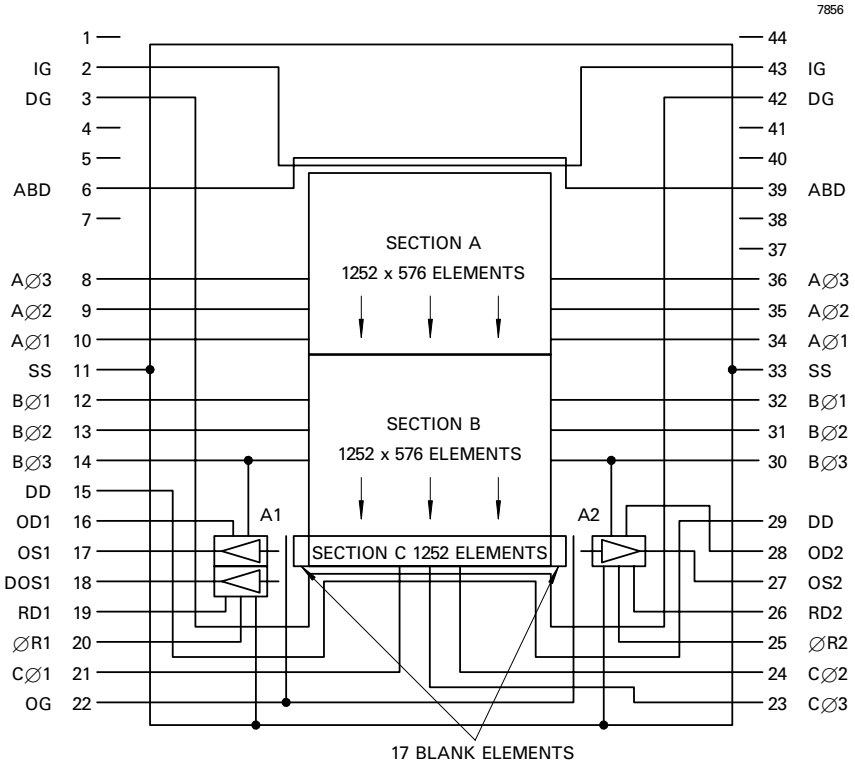


TYPICAL VARIATION OF DARK CURRENT WITH TEMPERATURE



DEVICE SCHEMATIC

The charge detection amplifier A1 is optimised for large signal, high speed operation, whereas amplifier A2 is optimised for very low noise under cooled slow-scan operation.



CONNECTIONS, TYPICAL VOLTAGES AND ABSOLUTE MAXIMUM RATINGS

PIN	REF	DESCRIPTION	PULSE AMPLITUDE OR DC LEVEL (V) (see note 9) Min	Typical	Max	MAXIMUM RATINGS with respect to V_{SS}
1	-	No connection	-	-	-	-
2	IG	Isolation gate (see note 10)	−5	0	1	±20 V
3	DG	Dump gate (see note 11)	−5	0	1	±20 V
4	-	No connection	-	-	-	-
5	-	No connection	-	-	-	-
6	ABD	Anti-blooming drain (see note 12)	20	22	25	−0.3 to +25 V
7	-	No connection	-	-	-	-
8	A∅3	Section A drive pulse	10	12	15	±20 V
9	A∅2	Section A drive pulse	10	12	15	±20 V
10	A∅1	Section A drive pulse	10	12	15	±20 V
11	SS	Substrate (see note 13)	8	9.5	10.5	-
12	B∅1	Section B drive pulse	10	12	15	±20 V
13	B∅2	Section B drive pulse	10	12	15	±20 V
14	B∅3	Section B drive pulse	10	12	15	±20 V
15	DD	Dump drain	20	22	25	−0.3 to +25 V
16	OD1	Output drains (A1)	27	29	30	−0.3 to +30 V
17	OS1	Output transistor source (A1)	see note 14			−0.3 to +30 V
18	DOS1	Dummy output source (A1)	see note 14			−0.3 to +30 V
19	RD1	Reset transistor drain (A1)	15	17	19	−0.3 to +25 V
20	∅R1	Output reset pulse (A1)	8	12	15	±20 V
21	C∅1	C register readout (see note 15)	10	12	15	±20 V
22	OGC	C register output gate (A1 and A2)	2	3	5	±20 V
23	C∅3	C register readout (see note 15)	10	12	15	±20 V
24	C∅2	C register readout (see note 15)	10	12	15	±20 V
25	∅R2	Output reset pulse (A2)	8	12	15	±20 V
26	RD2	Reset transistor drain (A2)	15	17	22	−0.3 to +25 V
27	OS2	Output transistor source (A2)	see note 16			−0.3 to +30 V
28	OD2	Output transistor drain (A2)	27	29	30	−0.3 to +30 V
29	DD	Dump drain	20	22	25	−0.3 to +25 V
30	B∅3	Section B drive pulse	10	12	15	±20 V
31	B∅2	Section B drive pulse	10	12	15	±20 V
32	B∅1	Section B drive pulse	10	12	15	±20 V
33	SS	Substrate (see note 13)	8	9.5	10.5	-
34	A∅1	Section A drive pulse	10	12	15	±20 V
35	A∅2	Section A drive pulse	10	12	15	±20 V
36	A∅3	Section A drive pulse	10	12	15	±20 V
37	-	No connection	-	-	-	-
38	-	No connection	-	-	-	-
39	ABD	Anti-blooming drain (see note 12)	20	22	25	−0.3 to +25 V
40	-	No connection	-	-	-	-
41	-	No connection	-	-	-	-
42	DG	Dump gate (see note 11)	−5	0	1	±20 V
43	IG	Isolation gate (see note 10)	−5	0	1	±20 V
44	-	No connection	-	-	-	-

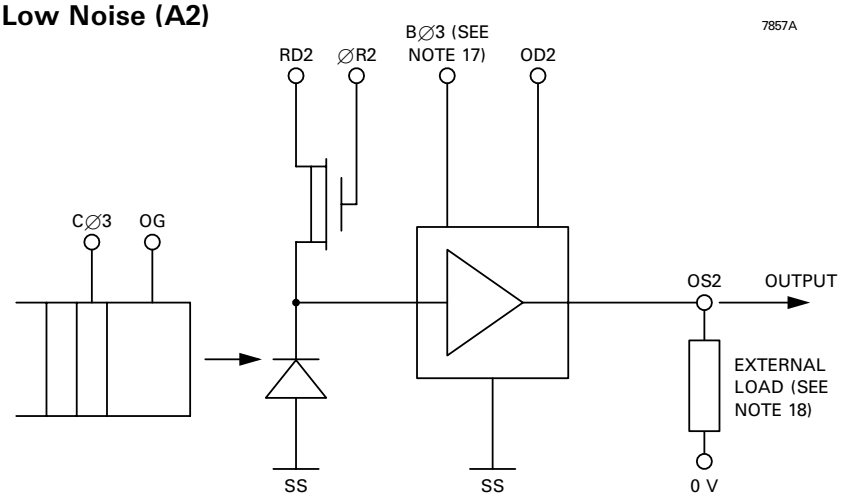
Voltages between pairs of pins:

pin 16 (OD1) to pin 17 (OS1)	±15	V
pin 16 (OD1) to pin 18 (DOS1)	±15	V
pin 27 (OS2) to pin 28 (OD2)	±15	V
Current through OD1	20	mA
Current through any other source or drain pin . .	10	mA

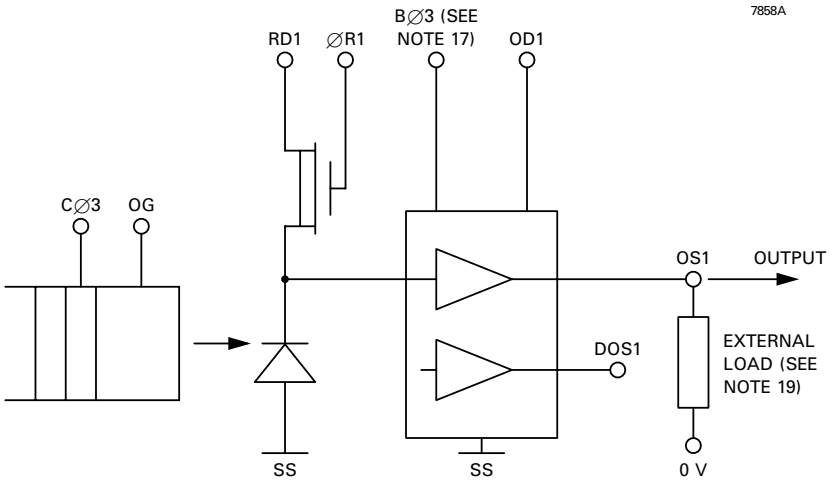
Operation at the typical voltages should give performance at, or close to, the specification limits. Some adjustment within the specified range may be required to optimise performance.

OUTPUT AMPLIFIER SCHEMATICS

Low Noise (A2)



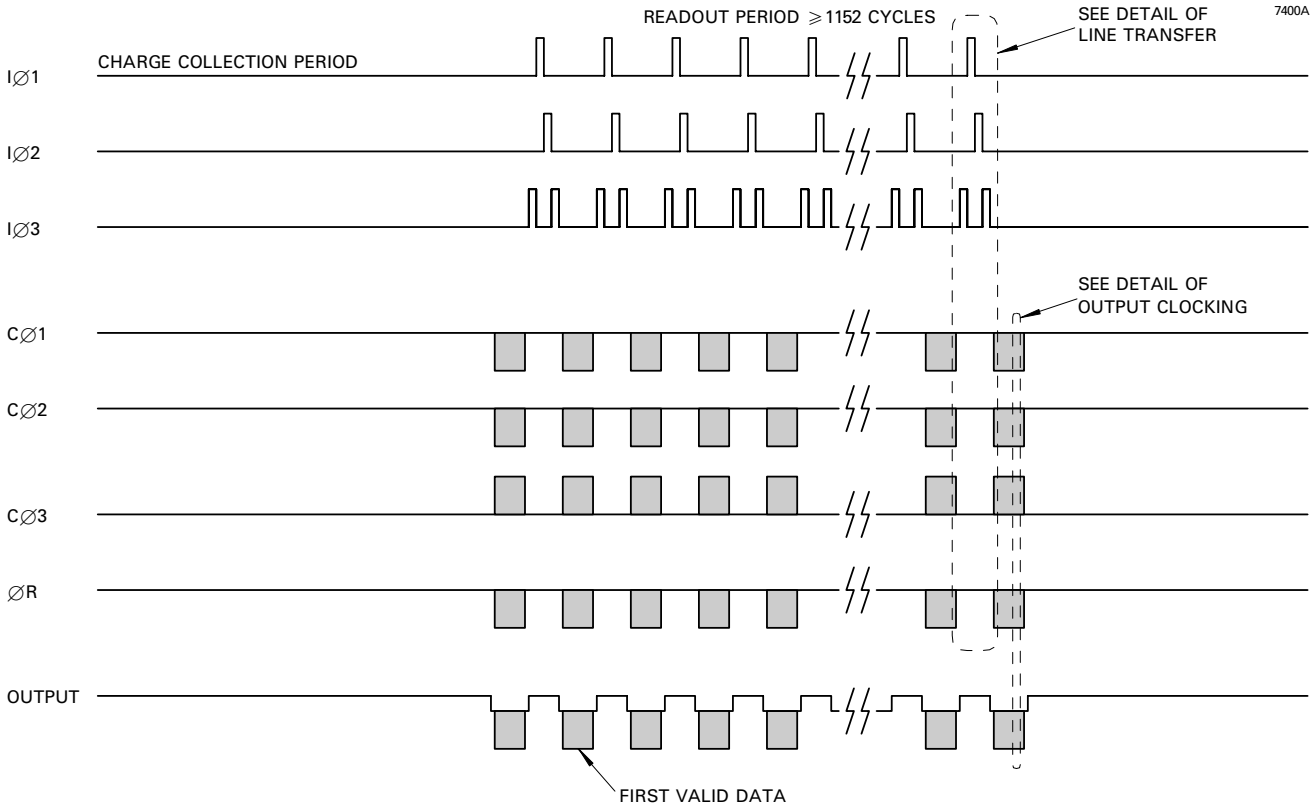
Large Signal (A1)



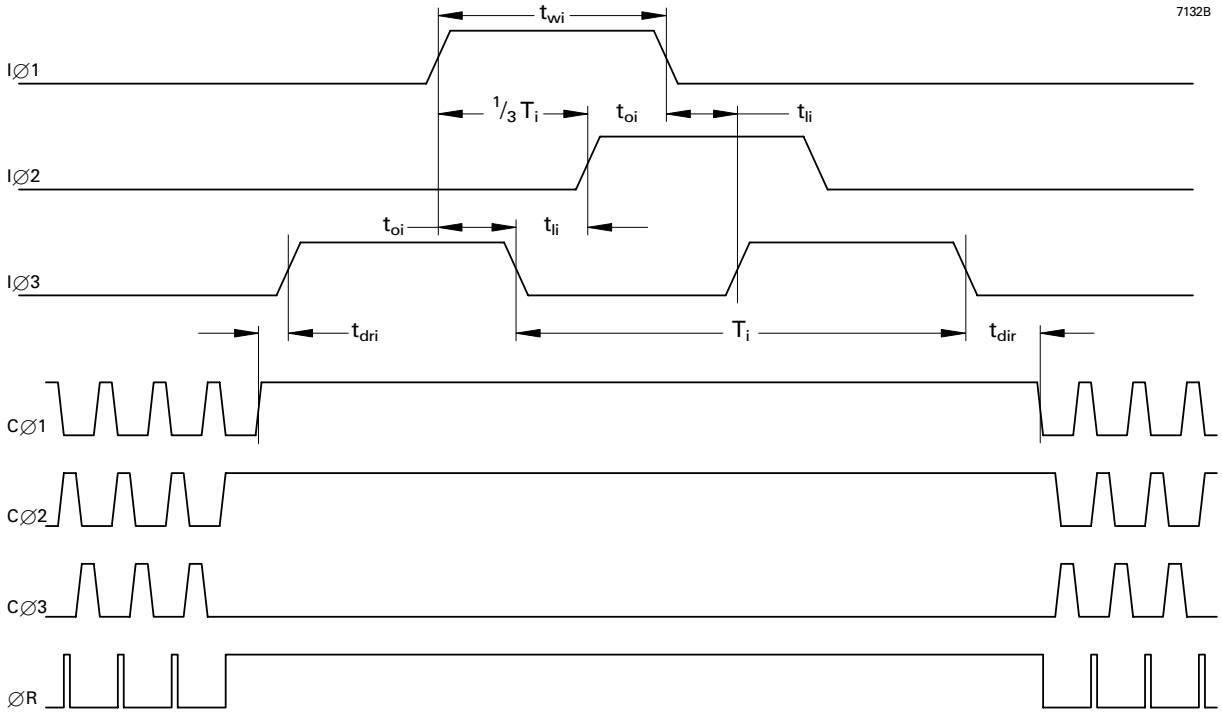
NOTES

9. All image clock low levels 0 ± 0.5 V. Other clock low levels + 1 V.
10. Charge can be reverse clocked into the drain at the top of the device. During this period of clocking, V_{IG} should be 12 ± 2 V.
11. Non-charge dumping level shown. For charge dumping, DG should be pulsed to 12 ± 2 V.
12. The device has no antiblooming but a drain bus is present above section A and must be biased to prevent charge injection. The isolation gate is between this bus and the first A∅1 electrode.
13. The substrate voltage may need to be adjusted within the range indicated to achieve correct inverted mode operation.
14. With a 7.5 mA constant current load, $V_{OS} = V_{RD} + 6$ V.
15. Readout through amplifier 2 shown; for readout through amplifier 1, C∅1 and C∅2 should be interchanged.
16. With a 5 mA constant current load, $V_{OS} = V_{RD} + 6$ V.
17. The amplifier has a DC restoration circuit which is internally activated whenever B∅3 is high.
18. Load not critical, can be 5 mA constant current supply or a 5 kΩ resistor.
19. Load not critical, can be 7.5 mA constant current supply or a 3.3 kΩ resistor.

FRAME READOUT TIMING DIAGRAM

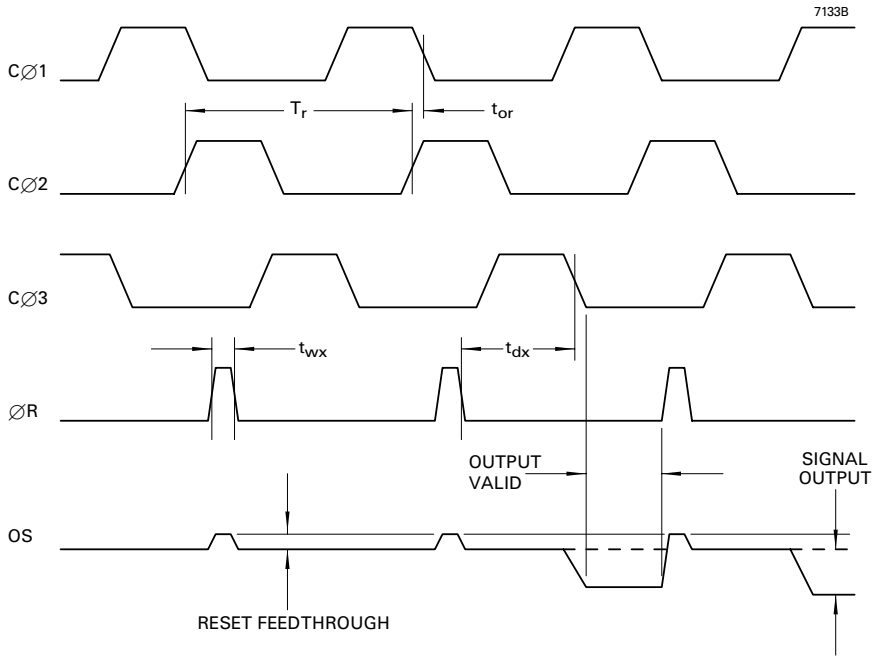


DETAIL OF LINE TRANSFER

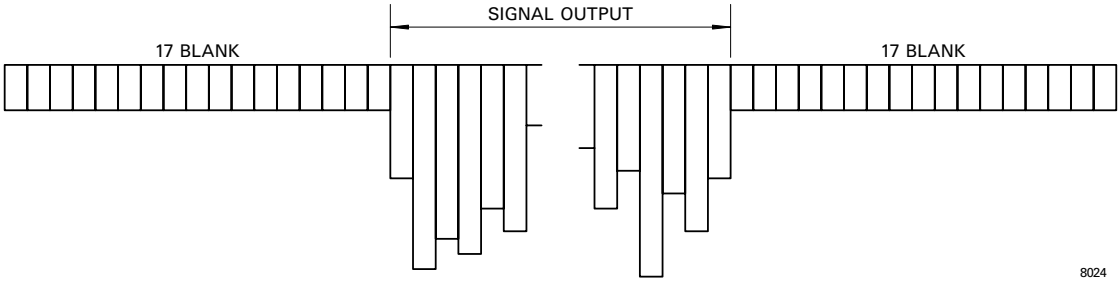


Note IØ1 = AØ1 + BØ1, IØ2 = AØ2 + BØ2, IØ3 = AØ3 + BØ3.

DETAIL OF OUTPUT CLOCKING



LINE OUTPUT FORMAT



CLOCK TIMING REQUIREMENTS

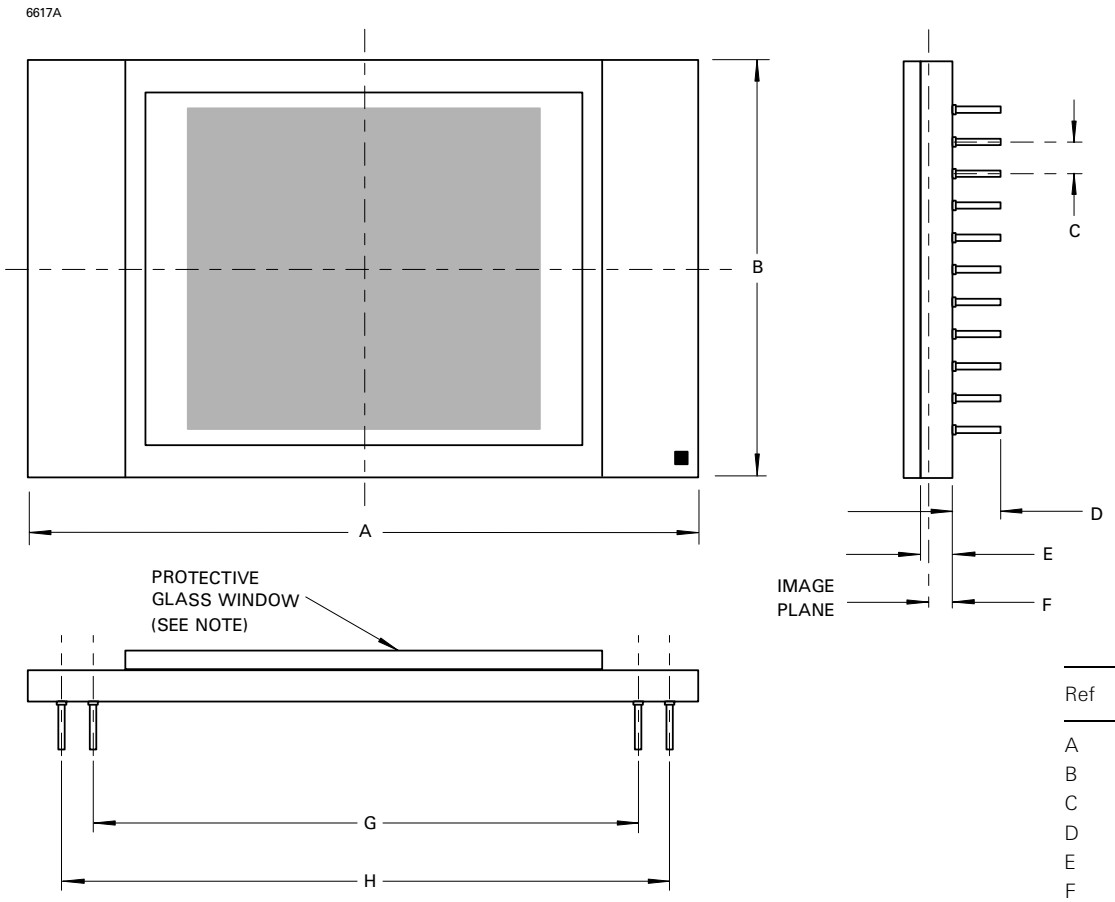
Symbol	Description	Min	Typical	Max	
T_i	Image clock period	15	30	see note 20	µs
t_{wi}	Image clock pulse width	7	15	see note 20	µs
t_{ri}	Image clock pulse rise time (10 to 90%)	0.5	2	$0.5t_{oi}$	µs
t_{fi}	Image clock pulse fall time (10 to 90%)	t_{ri}	2	$0.5t_{oi}$	µs
t_{oi}	Image clock pulse overlap	3	5	$0.2T_i$	µs
t_{li}	Image clock pulse, two phase low	2	5	$0.2T_i$	µs
t_{dir}	Delay time, IØ stop to RØ start	3	5	see note 20	µs
t_{dri}	Delay time, RØ stop to IØ start	1	2	see note 20	µs
T_r	Output register clock cycle period	150	see note 21	see note 20	ns
t_{rr}	Clock pulse rise time (10 to 90%)	10	$0.1T_r$	$0.3T_r$	ns
t_{fr}	Clock pulse fall time (10 to 90%)	t_{rr}	$0.1T_r$	$0.3T_r$	ns
t_{or}	Clock pulse overlap	10	$0.5t_{rr}$	$0.1T_r$	ns
t_{wx}	Reset pulse width	20	$0.1T_r$	$0.2T_r$	ns
t_{rx}, t_{fx}	Reset pulse rise and fall times	10	$0.5t_{rr}$	$0.2T_r$	ns
t_{dx}	Delay time, ØR low to RØ3 low	25	$0.5T_r$	$0.8T_r$	ns

NOTES

20. No maximum other than that necessary to achieve an acceptable dark signal at the longer readout times.
21. As set by the readout period.

OUTLINE (All dimensions nominal)

Not for inspection purposes

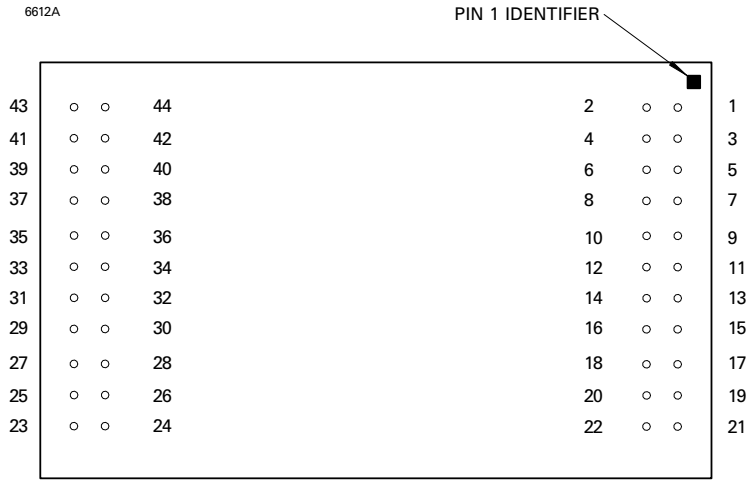


Ref	Millimetres
A	53.34
B	33.02
C	2.54
D	3.81
E	2.29
F	1.68
G	43.18
H	48.26

Outline Note

The device is normally supplied with a temporary glass window for protection purposes. It can also be supplied with a quartz or fibre-optic window where required.

PIN CONNECTIONS (View on Pins)



ORDERING INFORMATION

Options include:

- Temporary Quartz Window
- Temporary Glass Window
- Fibre-optic Coupling
- UV Coating
- X-ray Phosphor Coating
- Backthinned

For further information on the performance of these and other options, please contact e2v technologies.

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full antistatic handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving socket pins to be positively grounded
- Unattended CCDs should not be left out of their conducting foam or socket.

Evidence of incorrect handling will invalidate the warranty.

HIGH ENERGY RADIATION

Device characteristics will change when subject to ionising radiation.

Users planning to operate CCDs in high radiation environments are advised to contact e2v technologies.

TEMPERATURE LIMITS

	Min	Typical	Max	
Storage	153	–	373	K
Operating	153	253	323	K

Operation or storage in humid conditions may give rise to ice on the sensor surface on cooling, causing irreversible damage.

Maximum device heating/cooling . . . . 5 K/min