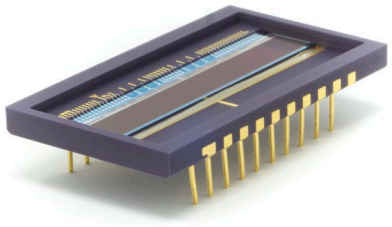
FEATURES

- Full Frame Spectroscopic Sensor
- 2048 by 264 Pixel Format
- 15µm Square Pixels
- Active image area 30.72 x 3.96 mm
- Advanced Inverted Mode Operation (AIMO)



INTRODUCTION

The CCD261-04 is a full frame spectroscopic format sensor product from Teledyne e2v.

The CCD261-04 has 2048(H) x 264(V) elements. Each element is 15 µm square. Standard three phase clocking and buried channel charge transfer are employed and Advanced Inverted Mode Operation (AIMO) is included as standard. Teledyne e2v's AIMO structure gives a 100 times reduction in dark current with minimum reduction in full well capacity.

Designers are advised to consult Teledyne e2v should they be considering using CCD sensors in abnormal environments or if they require customised packaging or performance features.

TYPICAL PERFORMANCE

Pixel readout frequency	1 MHz
Output amplifier sensitivity	6.3 µV/e^-
Peak signal	75 ke^-/pixel
Spectral range	450–1050 nm

GENERAL DATA

Format

Active Image area	30.72 x 3.96 mm
Active pixels	2048 (H) x 264 (V)
Pixel size	15µm square
Number of output amplifiers	1

Package

Overall dimensions	35.5 x 20.0 mm
Number of pins	20
Inter-pin spacing	2.54 mm
Package type	Ceramic DIL

Teledyne UK Limited, Waterhouse Lane, Chelmsford, Essex CM1 2QU United Kingdom Teledyne UK Ltd. is a Teledyne Technologies company.
Telephone: +44 (0)1245 493493 Facsimile: +44 (0)1245 492492
Contact Teledyne e2v by e-mail: Enquiries@Teledyne-e2v.com or visit www.teledyne-e2v.com for global sales and operations centres.

ELECTRO-OPTICAL PERFORMANCE (At 293K unless stated)

Parameters		Min	Typical	Max	Units	Notes
Output amplifier responsivity		5.5		7.8	μV/e-	
Image full well capacity			75		ke-/pixel	Note 2
Register full well capacity			650		ke-/pixel	Note 2
Output amplifier full well capacity			370		ke-	Note 2
Readout noise at 50kHz				4	e- rms	
Pixel readout frequency			0.5	3	MHz	Note 2, 3 & 4
Photo Response Non Uniformity	650nm			3	%	Note 5
	900nm			3	%	
Dark signal				650	e-/pix/s	Note 6
Dark Signal non-uniformity (DSNU)				160	e-/pix/s	Note 7

NOTES

1) All tests are at a pixel rate of 500kHz, except the noise test.
2) These values are inferred by design and not measured.
3) The quoted maximum frequencies assume a 20pF load and that correlated double sampling is being used.
4) This max pixel rate limit refers to that set by the output amplifier.
5) Photo Response Non-Uniformity (PRNU) is defined as the local 1σ variation in photo response to flat field illumination. Any pixels classed as dark defects at high light level are omitted from the analysis.
6) The quoted dark signal has approximately the usual temperature dependence for inverted mode operation. Clock induced charge is only weakly temperature dependent, is independent of integration time, and depends on the operating biases and timings employed. It is typically 0.26 e- / pixel/frame at T = +20 °C. For more information, refer to the technical note "Dark Signal and Clock-Induced Charge in L3Vision™ CCD Sensors"
7) DSNU is defined as the 1σ variation of the dark signal.

COSMETIC SPECIFICATION

Maximum allowed defect levels are indicated below.

GRADE	1
White Column defects	0
Black Column defects	0
White spots	5
Black spots	10

Grade 5 devices are also available as electrical samples. These are confirmed to have working outputs and will nominally provide an image. Not all parameters are guaranteed to be tested or provided and the image quality may be worse than that of a grade 1.

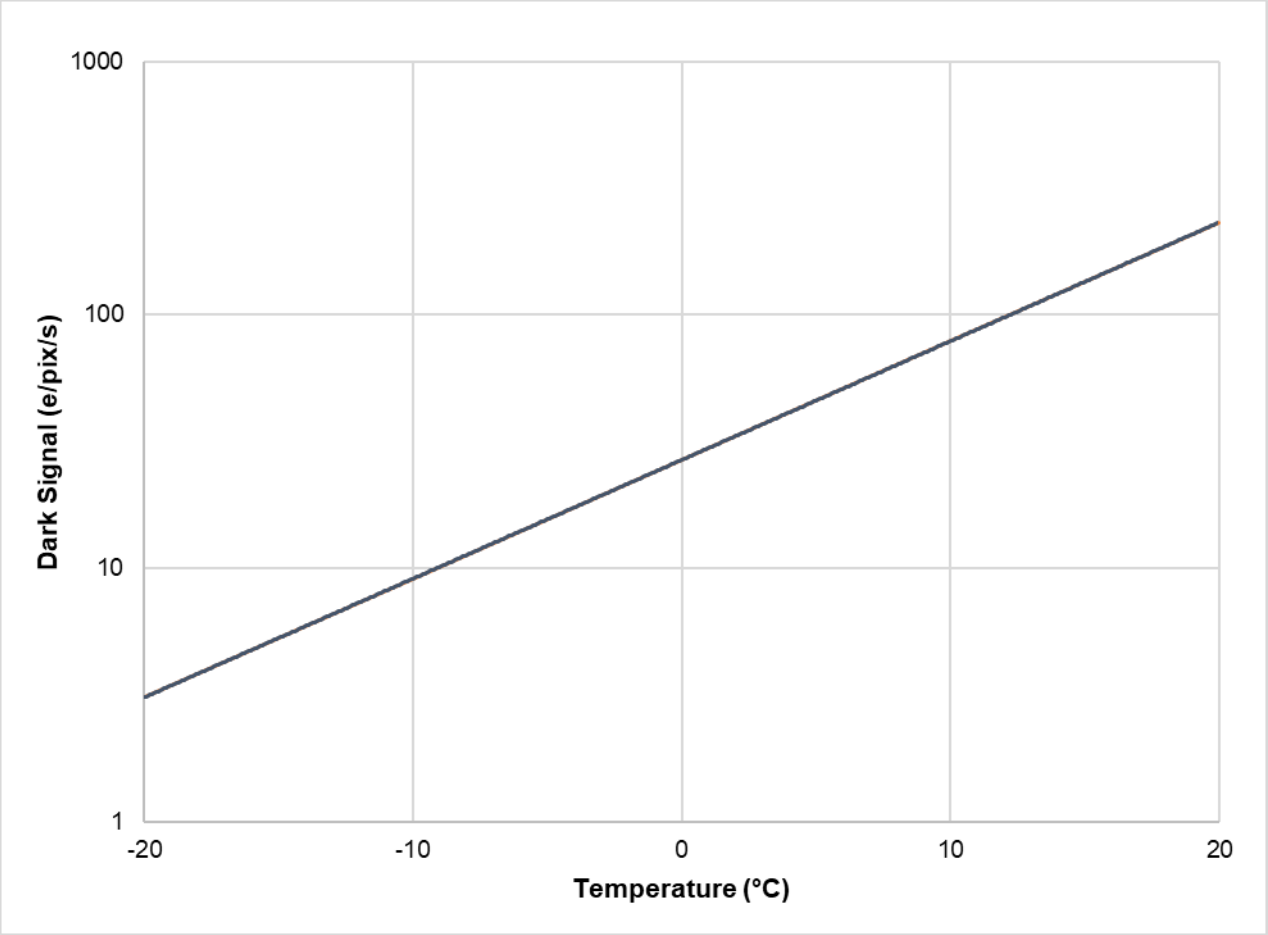
Note 8: Faint white spots and columns are ignored in the defect count

Note 9: A partial column defect longer than 100 pixels is counted as a column defect

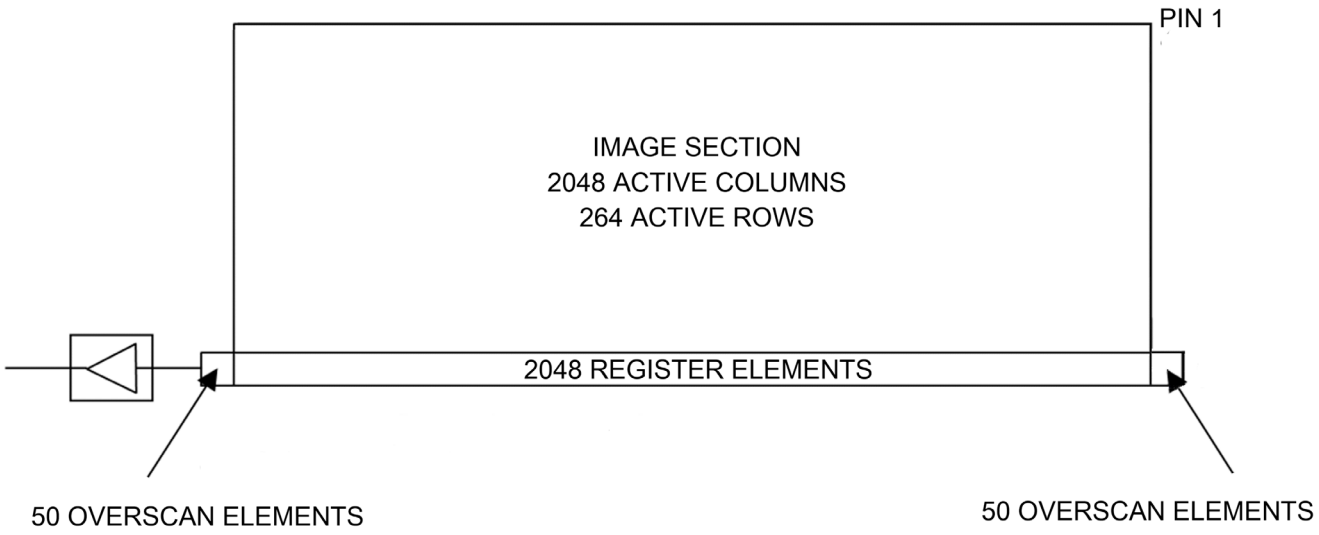
Note 10: A ‘black/white” pair column is a double column defect

Note 11: A partial black/partial white single column is classed as a black defect column

TYPICAL VARIATION OF DARK SIGNAL WITH TEMPERATURE



DEVICE SCHEMATIC



Not all connections are shown.

ELECTRICAL INTERFACE

PIN	REF	DESCRIPTION	CLOCK AMPLITUDE OR DC LEVEL (V) (see note 12)			MAX RATINGS with respect to SS	Notes
			Min	Typical	Max		
1	SS	Substrate	+8	+8.5	+11	N/A	15
2	IØ3	Image Clock High	+10	+14	+15	±20	15
		Image Clock Low	-0.5	0	+0.5	±20	
3	IØ2	Image Clock High	+10	+14	+15	±20	15
		Image Clock Low	-0.5	0	+0.5	±20	
4	IØ1	Image Clock High	+10	+14	+15	±20	15
		Image Clock Low	-0.5	0	+1.5	±20	
5	SS	Substrate	+8	+8.5	+11	N/A	15
6	ØR	Reset Clock High	+8	+12	+15	±20	13
		Reset Clock Low	-0.5	0	+1.5	±20	
7	RØ3	Register Clock High	+8	+12	+15	±20	
		Register Clock Low	-0.5	0	+1.5	±20	
8	RØ1	Register Clock High	+8	+12	+15	±20	
		Register Clock Low	-0.5	0	+1.5	±20	
9	RØ2	Register Clock High	+8	+12	+15	±20	
		Register Clock Low	-0.5	0	+1.5	±20	
10	N/C	Not Connected	-			N/A	
11	N/C	Not Connected	-			N/A	
12	OG	Output Gate	+1	+3	+5	±20	
13	OS	Output Source	N/A			-0.3 to +35	14
14	OD	Output Drain	+27	+31	+32	-0.3 to +35	
15	RD	Reset Drain	+15	+18	+19	-0.3 to +35	
16	SS	Substrate	+8	+8.5	+11	N/A	15
17	SW	Summing Well Clock High	+8	+12	+15	±20	
		Summing Well Clock Low	-0.5	0	+1.5	±20	
18	GD	Guard Drain	+27	+30	+32	-0.3 to +35	
19	SG	Spare Gate	0	0	+5	±20	
20	SS	Substrate	+8	+8.5	+11	N/A	15

NOTES

12) All operating voltages are with respect to readout clock low level (nominally 0V). To ensure correct device operation, the drive circuitry must be designed so that any value in the range Min to Min to Max can be set.

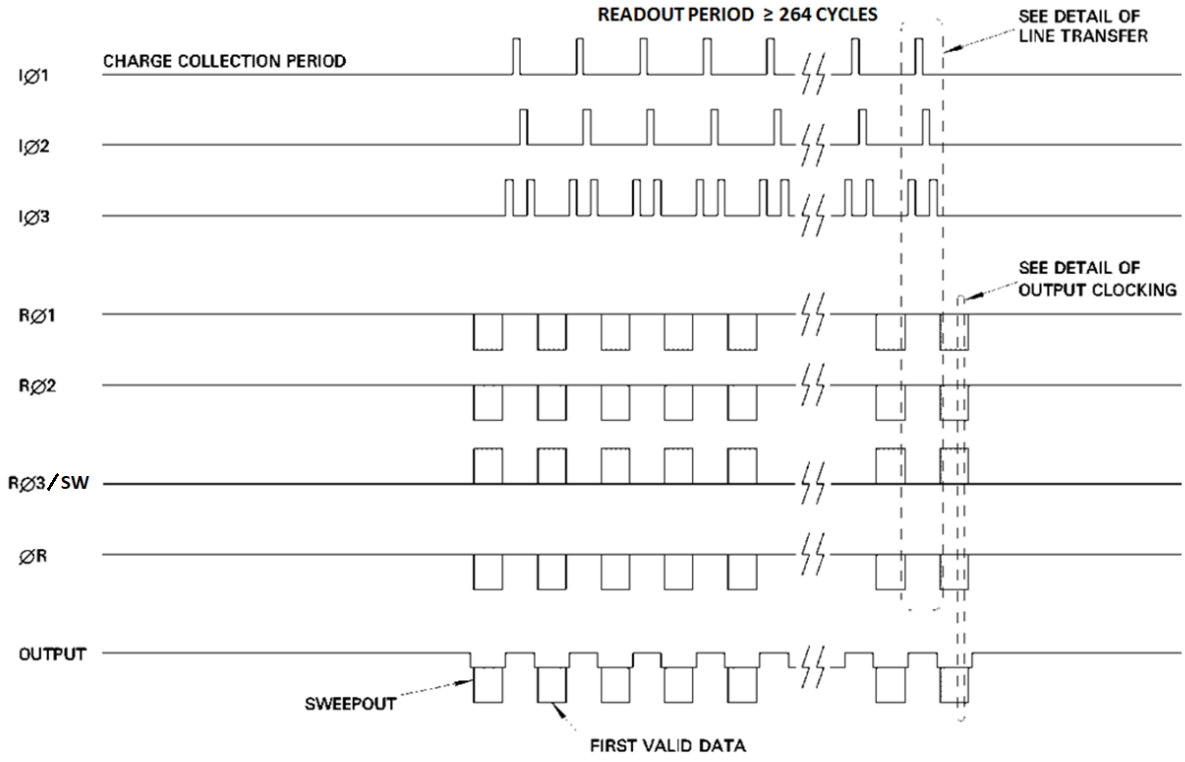
13) ØR high level is typically 1V above the high level of RØ1, RØ2 & RØ3.

14) See details of output circuit. Do not connect to voltage supply but use a ~5mA current source or a ~5kΩ external load. The quiescent voltage on OS is typically 5V more positive than that on RD. The current through these pins must not exceed 20mA. Permanent damage may result if, in operation, OS experiences short circuit conditions.

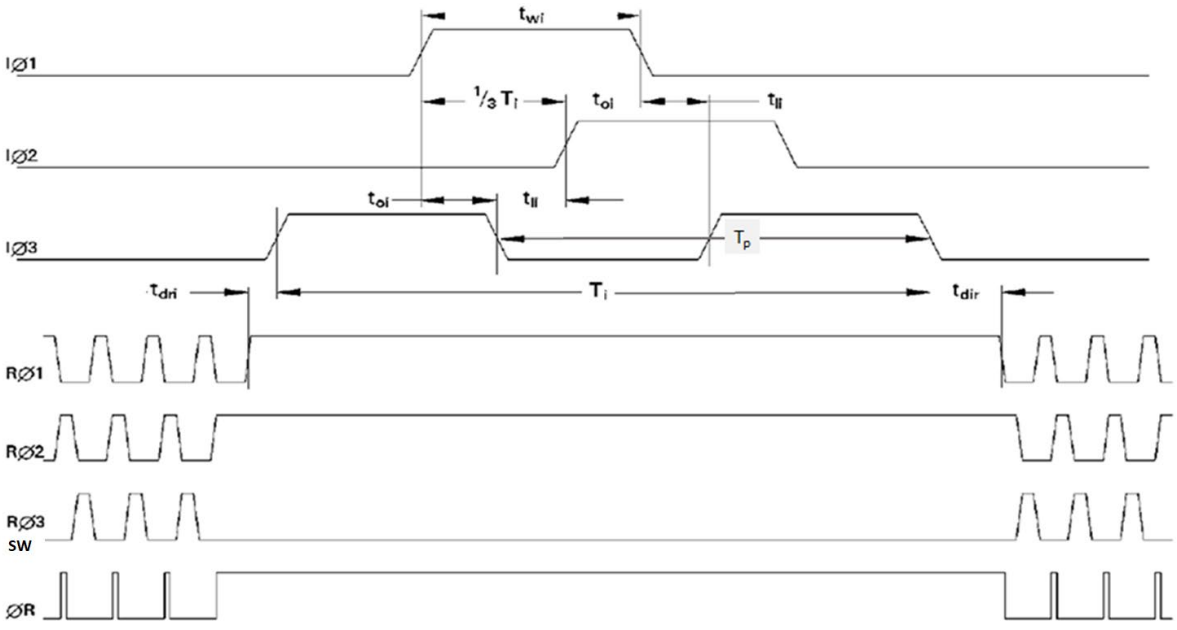
15) There is an interdependence between the SS, image section voltages and line transfer time. If one of these parameters is changed then it is often required to change one of the others.

16) If all the voltages are set to the “typical” values, operation at or close to specification should be obtained. Some adjustments within the minimum – maximum range specified may be required to optimise performance.

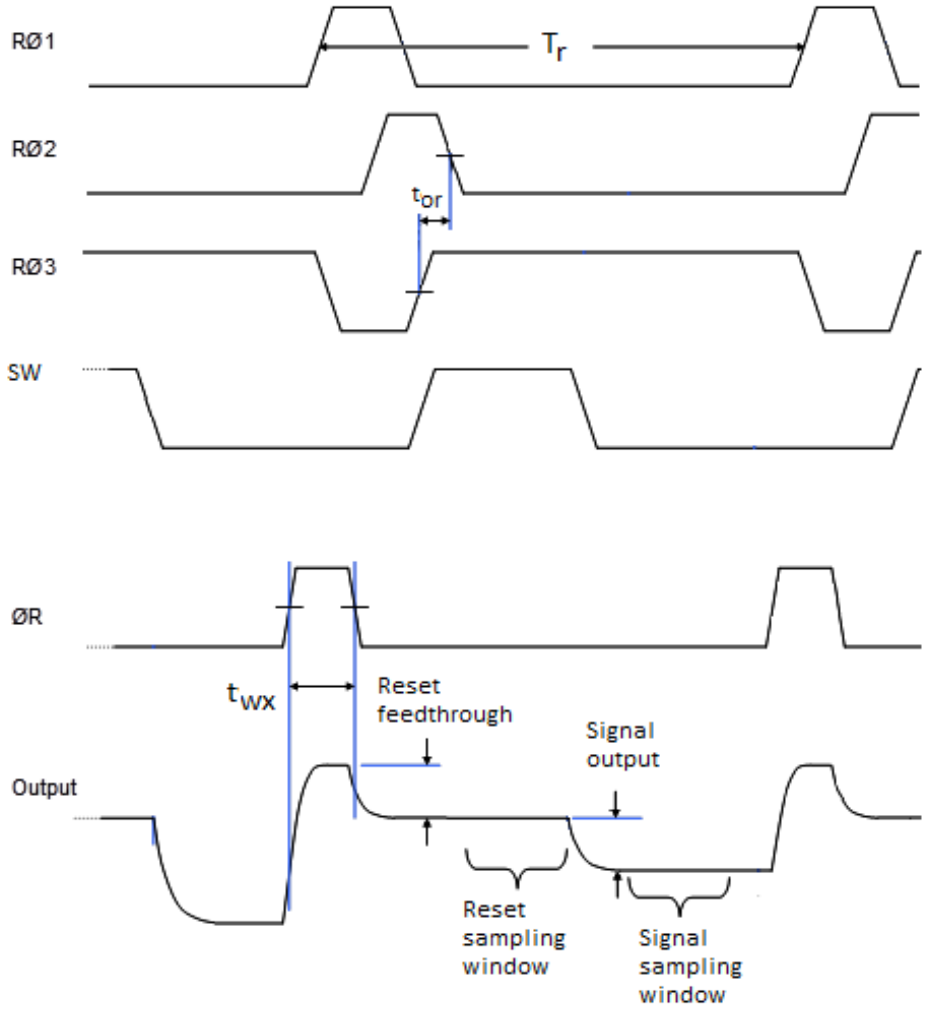
FRAME READOUT TIMING DIAGRAM



DETAIL OF LINE TRANSFER (Not to scale)



DETAIL OF OUTPUT CLOCKING

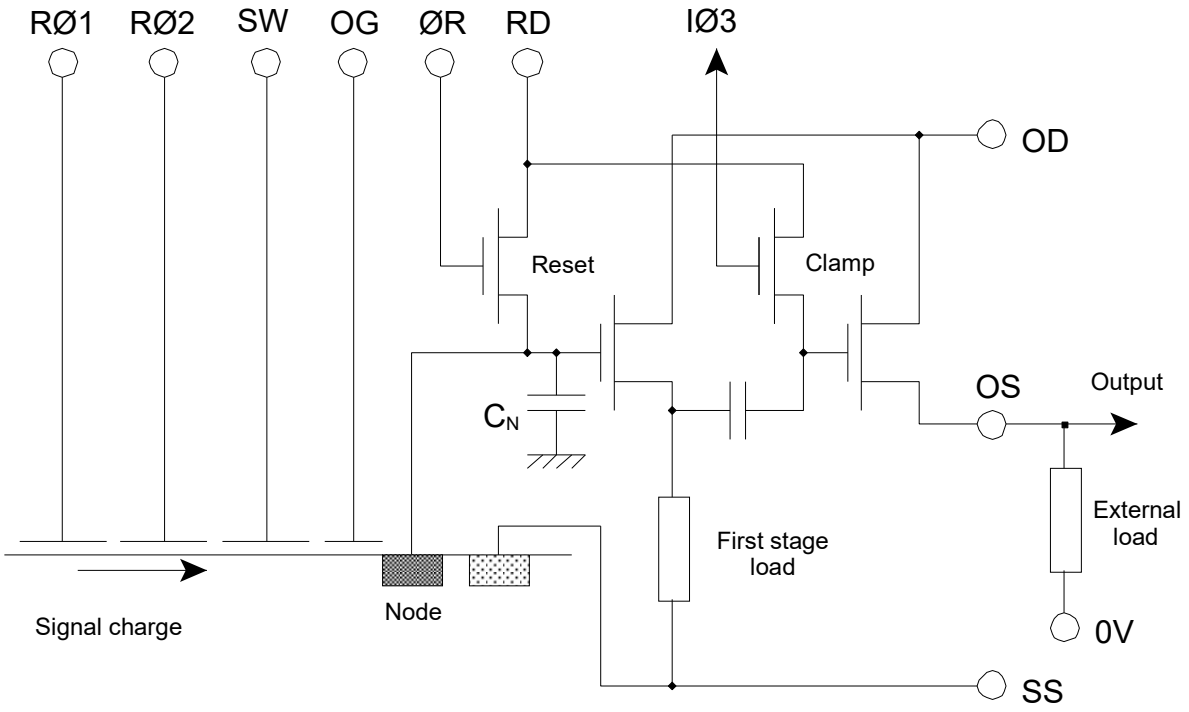


CLOCK TIMING REQUIREMENTS

Symbol	Description	Min	Typ	Max	Unit
T_p	Image clock period	3000	3250	Note 17	µs
T_i	Line transfer Time	-	4510	Note 17	µs
t_{wi}	Image clock pulse width	1500	1800	Note 17	µs
t_{oi}	Image clock pulse overlap	400	500	-	µs
t_{li}	Image clock pulse, two phase low	400	500	Note 17	µs
t_{dir}	Delay time, IØ stop to RØ start	5	20	Note 17	µs
t_{dri}	Delay time, RØ stop to IØ start	5	20	Note 17	µs
T_r	Output register clock cycle period	1	2	Note 18	µs
t_{rr}	Register pulse rise time (10 to 90%)	50	90	Note 19	ns
t_{fr}	Register pulse fall time (10 to 90%)	50	90	Note 19	ns
t_{or}	Register pulse overlap (50%)	20	120	Note 19	ns
t_{wx}	Reset pulse width	30	170	Note 19	ns
t_{rx}	Reset pulse rise and fall times	20	80	Note 19	ns
t_{dx}	Delay time, ØR low to RØ3 low	-	80	Note 19	ns

17) No maximum other than that necessary to achieve an acceptable dark signal at longer readout times and general compliance to the line transfer timing diagram. Scale to T_p.
18) Determined by readout time requirement.
19) Scale to T_r.

OUTPUT CIRCUIT

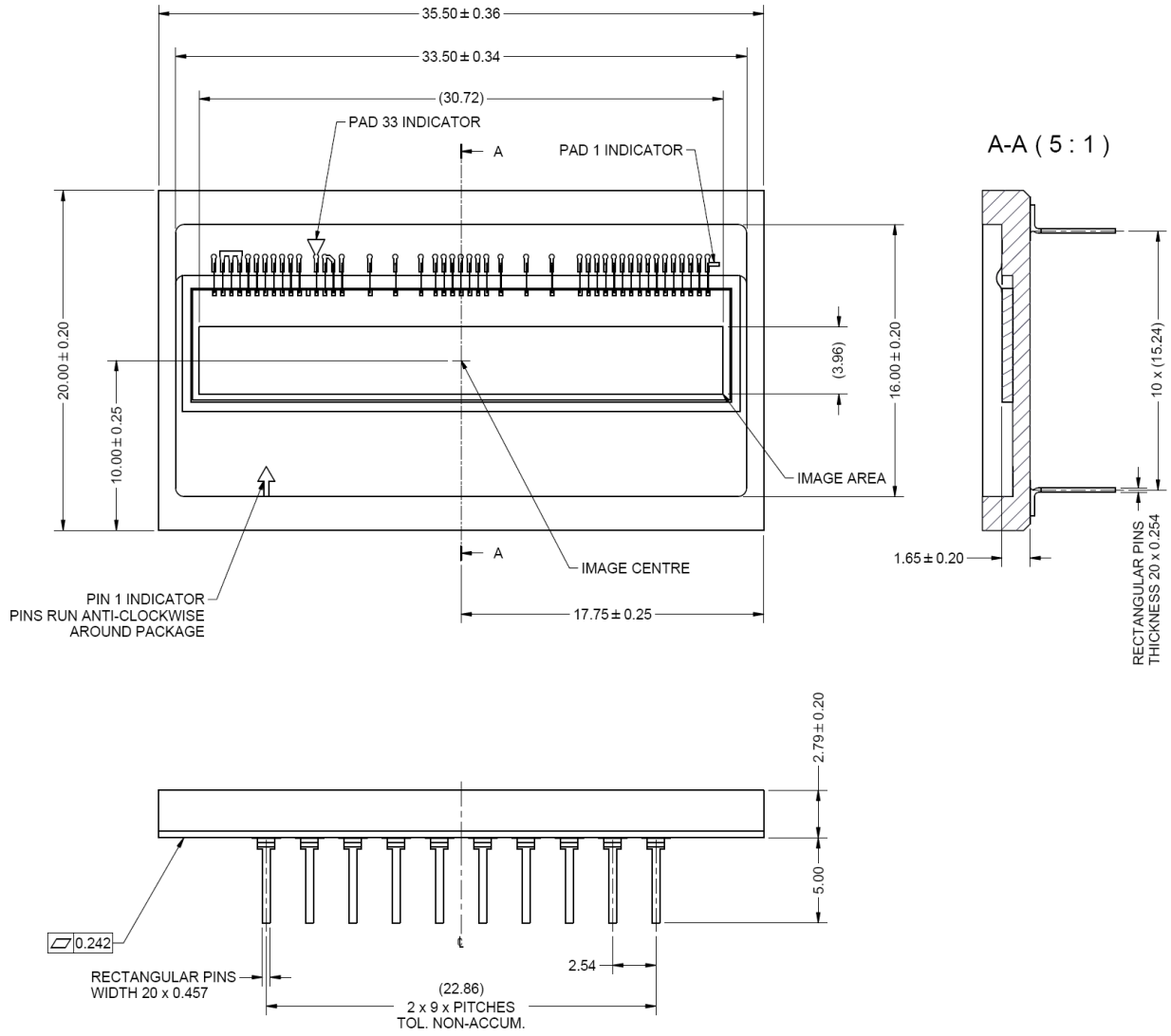


NOTES

20) The amplifier has a DC restoration circuit, which is activated internally whenever IØ3 is pulsed high.

PACKAGE

(All dimensions are nominal and are in mm)



ORDERING INFORMATION

CCD261-04-g-xxx
g = cosmetic grade
xxx= specific variant type (e.g. thickness and coating)

CCD261-04-g-S32: Standard Silicon, no coating

For further information on the performance of this and other options, please contact Teledyne e2v.

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full antistatic handling precautions should be taken whenever using a CCD sensor or module. These include:-

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving socket pins to be positively grounded
- Unattended CCDs should not be left out of their conducting foam or socket.

Evidence of incorrect handling will invalidate the warranty.

HIGH ENERGY RADIATION

Device characteristics will change when subject to ionising radiation.
Users planning to operate CCDs in high radiation environments are advised to contact Teledyne e2v.

TEMPERATURE LIMITS

	Min	Typical	Max	
Storage	148	-	323	K
Operating	223	263	293	K

Operation or storage in humid conditions may give rise to ice on the sensor surface on cooling, causing irreversible damage.

Maximum device heating/cooling ..... 5 K/min