FEATURES

- 1504 × 2000 Pixels

    Pixel size is 7 × 7 µm

- Four parallel analogue output ports

    Each port has both reset and signal levels

- Back-illuminated spectral response and low readout noise

    Excellent image quality

- An easy to drive image sensor for use in space applications

    Parallel buses for row and column addresses

- Ceramic pin grid array package

OVERVIEW

The sensor has an image area with 1504 × 2000 pixels, read out through 4 parallel analogue output ports in rolling shutter mode. Each port has both reset and signal levels to allow external CDS subtraction and to improve common mode rejection. The pixel size is 7 µm square.

Row and Column addresses are input as parallel buses, so by only reading a selection of row addresses it is possible to read a range of regions of interest (ROI) and achieve a higher frame rate. In the same way a selection of columns can be chosen, but this is more restricted due to the common address for all four blocks of columns.

The output amplifier is designed to give very low noise at readout rates of 6.2 MP/s.

The package is a robust and proven design for use in space. A temporary window is attached for some testing and for shipping, while for the final application it is expected that this window will be removed.

PERFORMANCE (ELECTRO-OPTICAL SPECIFICATION)

Device performance will be within the limits specified by "max" and "min" when operated at the recommended supply voltages, with the recommended read timing and at 293 K, unless otherwise stated. The noise as specified is measured in accordance with note 8.

Parameter	Min	Typical	Max	Units	Note
Pixel size		7		µm	Square
Number of active rows		2000			1
Number of active columns		1504			1
Output settling time		160		ns	2
Frame rate using whole array			7.5	fps	3
Q_{SAT}, saturation charge per pixel	–	33,000	–	e⁻/pixel	4
Q_{LIN}, peak linear charge per pixel	–	27,000	–	e⁻/pixel	5
Non-linearity		±3		%	6
CVF, overall conversion gain	–	50	–	µV/e⁻	7
Mean readout noise in electrons	–	5	–	e⁻ rms	8
Mean readout noise in µV	–	250	–	µV rms	8
Dynamic range	–	74.6		dB	
Pixel readout rate	–	6.2	10	MP/s	9
Time to read and readout one row at 6.2 MP/s	66.65			µs	
Dark current at 293 K	–	20	–	e⁻/pixel/s	10
DSNU at 293 K		12		e⁻/pixel/s	11
Lag		1		%	12
Quantum efficiency at 650 nm	–	90	–	%	13
PRNU at 293 K		2		%	14
BSI fill factor		~100		%	15

Table 1: Electro-optical characteristics.

NOTES

1. 8 rows or columns of dummy pixels added along each edge of active array. These pixels cannot be read and so have no address.

2. Settling to 99% of final change in signal voltage. Measured with I_{READ}=60 µA.

3. Reading only a region of interest will allow a higher frame rate, such as 1000 rows at 15 fps.

4. Maximum signal level. Set by the sense node and not by the pinned photodiode.

5. Signal level at which linearity begins to rapidly degrade. Set by the sense node and not by the pinned photodiode. Q_{LIN} is defined in the measurement system to be where the non-linearity first reaches 5 %.

6. Non-linearity is measured over the range from 10% to 90% of Q_{LIN}.

7. Including in-pixel source follower and whole path to output pin.

8. Measured with correlated double sampling and at 6.2 MP/s nominal pixel rate on each of the four channels.

9. For outputs to adequately settle at 10 MP/s, IREAD must be increased to 100 µA.

10. Dark current is measured at a device temperature of 293 K. It is a strong function of temperature and the temperature change to halve or double the dark current is typically around 5.5 °C.

11. DSNU is the standard deviation of the pixel by pixel dark current and excludes defective pixels.

12. Residual charge in pinned photodiode after transfer to the sense node. Measured at half Q_{LIN}.

13. QE at 650nm shown for M33 variant. See Figure 1 and Figure 2 for typical spectral response curves.

14. PRNU is defined as the standard deviation of all pixel responses (after subtraction of dark offset) in % of the mean response. PRNU is measured at half Q_{LIN} and excludes defective pixels.

15. At UV and visible wavelengths the light is totally absorbed near the input surface to give charge which is collected by the photodiodes and close to 100 % fill factor. At longer wavelengths some of the light will penetrate right through the silicon and so be not detected. This gives both a reduced fill factor and a lower QE. See fall-off in SDE above 700 nm in Figure 1.

SPECTRAL RESPONSE

Figure 1 and Figure 2 give a modelled and measured spectral response curve for the M33 and M48 variants:
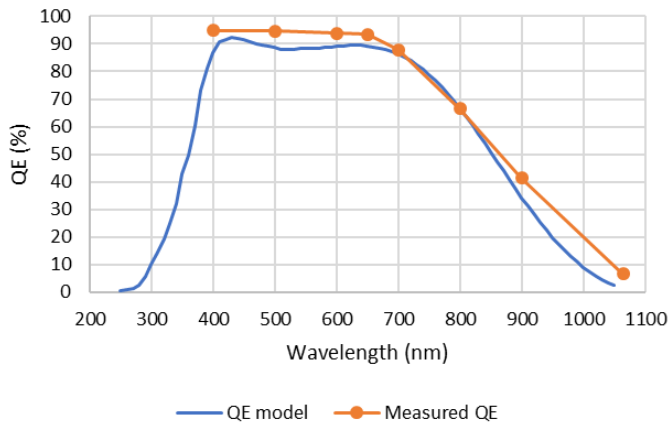

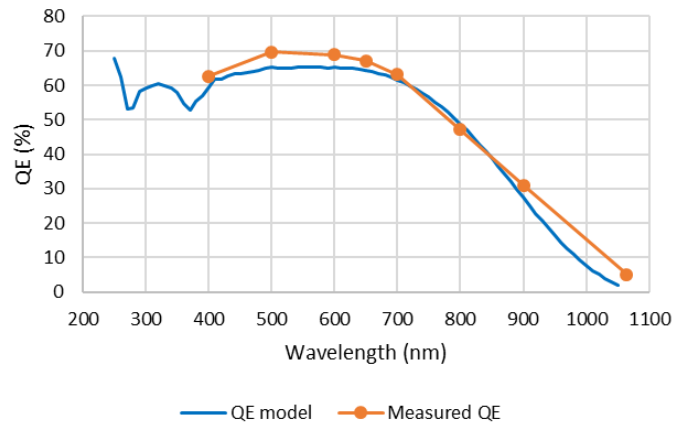*Figure 1: Typical spectral response of M33 variant at 293°K.*

Figure 2: Typical spectral response of M48 variant at 293°K.

Figure 1 gives the response with the "enhanced" back thinning process and a "Multi-2" AR coating (M33 variant). Figure 2 gives the responses with the "enhanced" back thinning process and UV optimised single layer AR coating (M48 variant).

Other coatings (single and multi-layer) could be available as custom variants.

COSMETIC SPECIFICATIONS

Maximum allowed defects for each grade are indicated in Table 2:

	Grade 0	Grade 1
Number of Row defects	0	1
Number of Column defects	0	1
Percentage of pixels with dark signal defects (not including pixels that give row or column defects)	0.1 %	1.0 %
Percentage of pixels with photo-response defects (not including pixels that give row or column defects)	0.05 %	0.1 %
Percentage of pixels that are high noise pixels (not including pixels that give row or column defects)	0.5 %	1.0 %

Table 2: Cosmetic specifications.

Grade 1 is the default for science use.

Other grades may be available.

Grade 5 devices are fully functional but with an image quality below that of grade 1 and may not meet all other specifications – not all parameters are necessarily tested at this grade.

Definitions for cosmetic specifications

Dark signal defects	A pixel is counted as a dark signal defect if its dark current is ≥ 250 e⁻/pixel/s at 293 K.
Photo-response defects	A pixel is counted as a photo-response defect if its photo-response is < 80 % or > 120 % of the local mean.
High noise pixels	A pixel is counted as a noise defect if its Read Out Noise (RON) is ≥ 2 × the typical RON in Table 1.
Column defects	A column is counted as a defect if it contains ≥ 100 single pixel defects.
Row defects	A row is counted as a defect if it contains ≥ 100 single pixel defects.

Table 3: Definitions of types of defect.

DEFINITIONS

Back-Thinning

A back-thinned image sensor (CMOS or CCD) is fabricated on the front surface of the silicon and then subsequently processed for illumination from the reverse side. This avoids loss of transmission due to front surface features (metal tracks in CMOS or the electrodes in CCD) and also removes most of the etalon effect caused by multiple reflecting surfaces. Back-thinning reduces the silicon to a thin layer by a combination of chemical and mechanical means.

AR Coating

Anti-reflection (AR) coatings are normally applied to the back illuminated image sensor to further improve the quantum efficiency. Silicon has a very high refractive index so the air to silicon interface is highly reflective if it is not suitably coated. Standard coatings optimise the response in the visible, ultra-violet or infrared regions. For EUV, VUV and X-ray detection an uncoated device may be preferable.

Spectral Detection Efficiency (SDE)

The ratio of the number of electrons generated and sensed to the number of incident photons over the whole pixel. This includes the effects of Fill Factor, as well as the physics of light detection.

Readout Noise (RON)

CMOS readout noise is the total of the noise from the pixels, read circuits and output stages. The mean value is reported in Table 1.

Correlated Double Sampling (CDS)

Each video output has two pins, an IMAGESIG[n] and an IMAGEREF[n]. The on-chip sampling will put the light-dependent level on IMAGESIG[n] following a transfer from the photodiode to the sense node. This will include the kTC noise from the reset of the sense node, so the IMAGEREF[n] output will give the reset (black) level plus the same kTC noise. By means of a differential pre-amplifier it is possible to subtract the kTC noise and black level from the signal level to give low total noise. The penalty is that the readout noise is increased by a factor of √2, but this is normally much less than the kTC noise. If not required the IMAGEREF[n] outputs can be ignored.

Dark Signal

This is the output signal of the device with zero illumination. This typically consists of thermally generated electrons within the semiconductor material, which are accumulated during signal integration. Dark signal is a strong function of temperature as described in note 9 under Table 1.

Lag

The fraction of collected charge remaining in the photodiode after the transfer pulse intended to transfer all collected charge to the sense node. The value of lag varies with signal size and transfer pulse width.

ARCHITECTURE

Overall Floorplan

The chip structure in Figure 4 shows how the 1504 columns are split into four blocks of 376, each with separate read circuits and column select blocks, but sharing the timing from SHS and SHR and the column address from C_ADDR[8:0]:
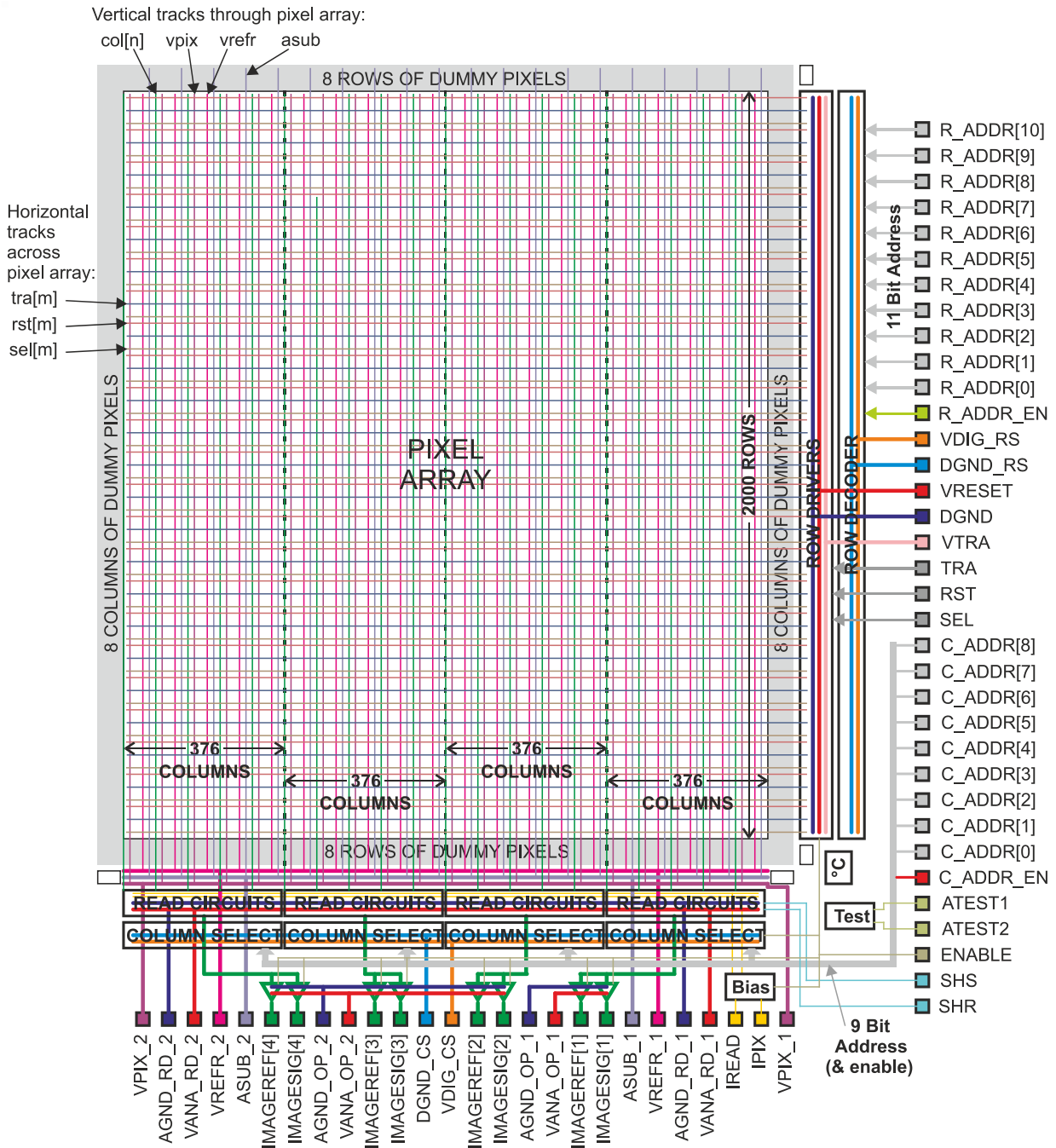

Figure 3: General structure of CIS115.

The pixel array is contiguous, with each block of 376 columns feeding a separate output port.

Only a few sample tracks for the control signals (tra[m], rst[m] and sel[m]), the column outputs (col[n]) and the power and ground connections (vpix, vrefr and asub) are shown to keep the diagram clear while showing in which direction each track is run.

Pixel Design

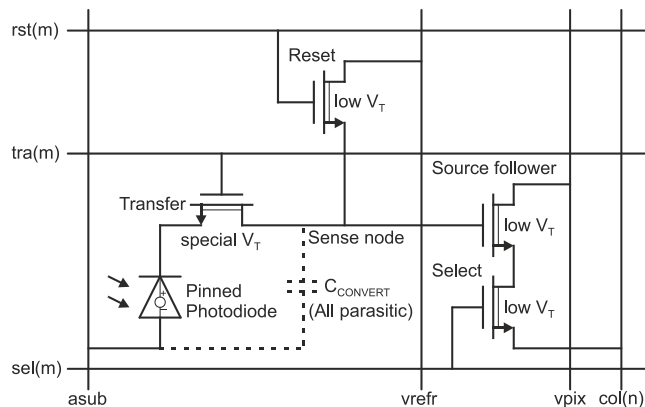All pixels in CIS115 are of the same design. A 4T structure is used, as in Figure 5:

Figure 4: Circuit diagram of each pixel.

Pixel operation

Pixel control signals tra[m], rst[m] and sel[m] are the local versions of the pin signals TRA, RST and SEL formed by gating with the decoded row address and then buffering to drive all pixels in the addressed row. This gating is such that all unaddressed rows have all three signals at low. For the addressed row the internal signals follow the levels on the associated pin. Each read sequence must start with a reset to the sense node (RST at high) so many systems keep RST at high from one read to the next – only the addressed row will see the reset.

Pixel column outputs col[n] drive the read circuits at the bottom of the pixel array. These include a pull-down current source biased by IPIX, set to give a balance of low noise bandwidth and a reasonably fast read speed.

Pixel power and ground connections vpix, vrefr and asub are directly connected to the pins of similar names, VPIX, VREFR and ASUB. The need for two supply connections to the pixel is to allow the sense node reset level and the source follower supply to be independently adjusted, to find the best operating point. In some applications VREFR and VPIX will be connected together.

To improve the performance of the pixels, this device is manufactured on an image sensor CMOS process.

This includes an epitaxial layer of silicon (epi) grown on the starting wafer to allow all active circuit components to be in an optimised substrate. Then, in order to improve the SDE at IR wavelengths, the epi for the CIS115 has been chosen to be thicker than standard. To maintain good MTF at all wavelengths the epi has also been chosen to have higher resistivity than standard. This combination of thickness and resistivity is becoming regular in CMOS image sensor products.

In operation each integrate and read cycle starts with the pinned photodiodes charged to their reset levels by using the reset and transfer transistors in the previous cycle. Light is absorbed in the silicon in and below the photodiodes and releases electrons which are collected in the photodiodes, reducing their potential from the reset level. During most of this integration time all reset control lines rst(m) are held low, as no more than one row can be addressed at any time, so a pulse on the addressed rst(m) is needed just before row m is read to drive the sense nodes of the whole row to the reset level. This is normally provided by loading the address while pin RST is high, see Figure 7. Once the rst(m) and sel(m) feedthrough are finished and the sense nodes have settled at the reset level, a pulse on pin SHR drives the vr sample and hold circuits at the bottom of every column (see Figure 6) to store the reset level on nodes vr. The next action is a pulse on pin TRA to drive a pulse on the addressed tra(m) to move the charge from the photodiodes to the sense nodes. When the sense nodes have settled to their new levels, a pulse on pin SHS drives the vs sample and hold circuits at the bottom of every column (see Figure 6) to store the signal levels on nodes vs. After this pulse on SHS the row has been read, with all reset and signal levels stored in the sample and hold circuits, ready to be output by the column selector. External subtraction can then be used to have the lowest noise by CDS.

Each group of 376 columns has a separate column decoder, but all are driven by the common column address bus C_ADDR[8:0]. The sample and hold circuits are buffered to drive a multiplexor which selects which column will drive the output stages IMAGEREF[n] and IMAGESIG[n] for that set of 376 columns (see Figure 6).
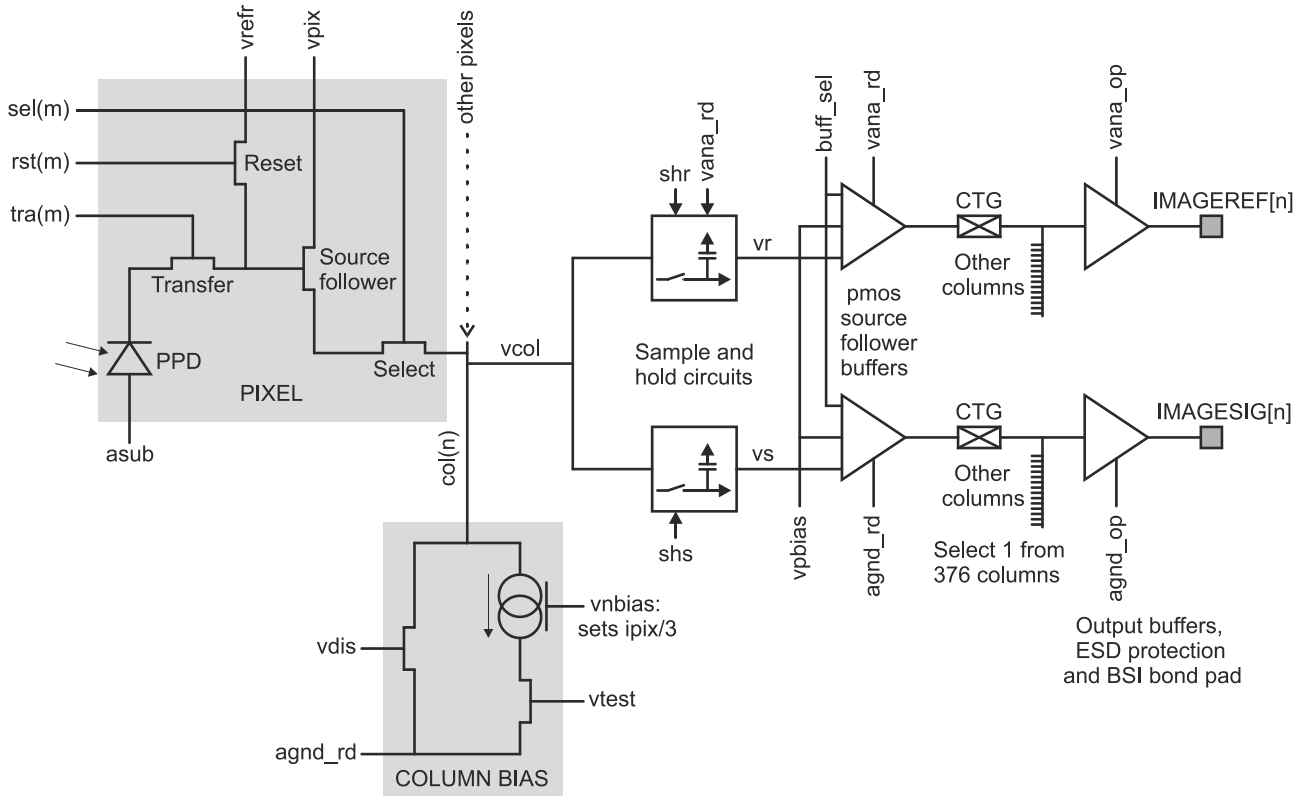
Figure 5: Read path from pixel to output pins.

TIMING INFORMATION

It is possible to operate this image sensor with many different pulse widths and spaces, but the sequence must be as in Figure 7. Durations and separations as in Table 4 were used for the measured performance.
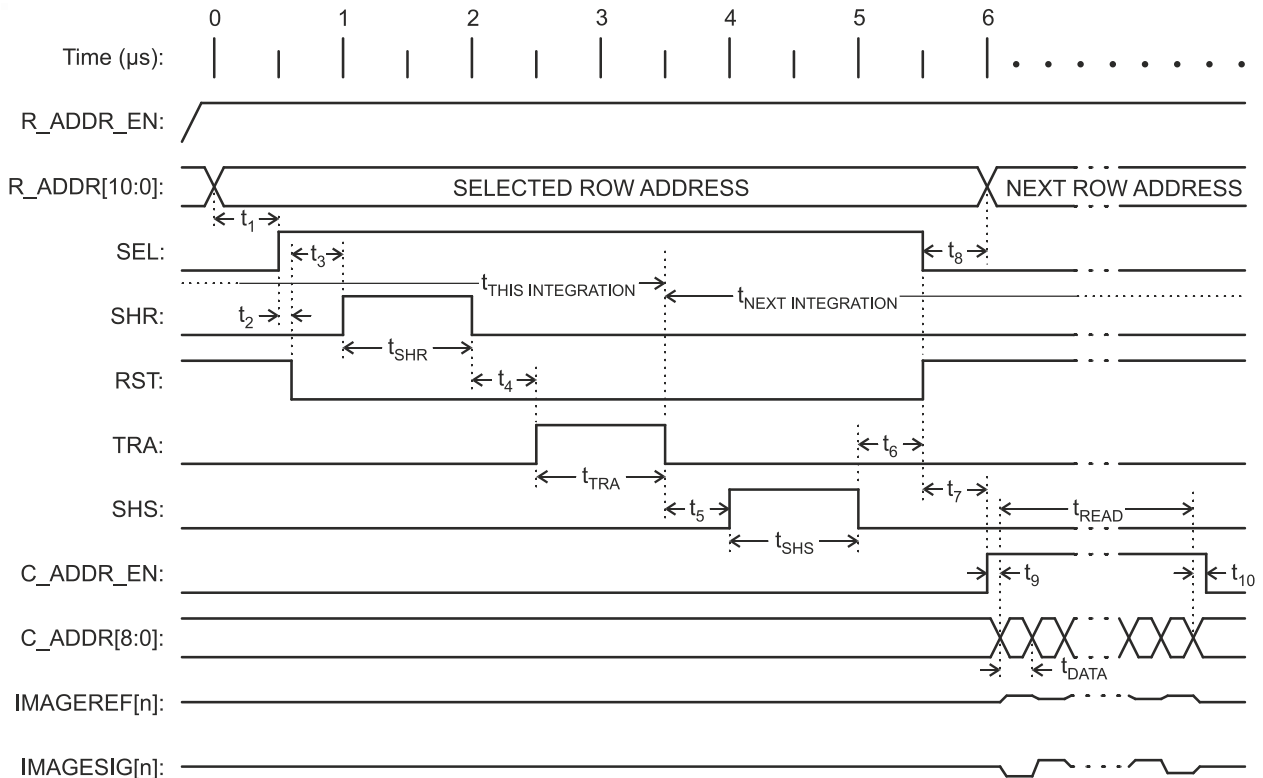

Figure 6: Typical timing diagram.

The two address enables, R_ADDR_EN and C_ADDR_EN are included in the row or column decode gates and so control the drive of internal signals to each address and must be high throughout the time the address is needed. When stepping through a range of addresses to read an area of the image it is usual to hold the enable high during and between each address. The only reason to drive either address enable to low is to block the propagation of erroneous addresses.

Any non-valid address will not be decoded and so will not affect the integration of the required image, but will interrupt the readout of that image.

Note: IMAGEREF[n] will give the reset level of each pixel and so will show little change pixel to pixel. IMAGESIG[n] will give the result of the integration of light and so can show very large changes from pixel to pixel. The difference between these two signals gives the true value of the illumination, pixel by pixel.

Timing	Definition	Typical value	Unit
t_{SHR}	Pulse width to sample the reset level.	1.0	µs
t_{TRA}	Photodiode to sense node transfer pulse width	1.0	µs
t_{SHS}	Pulse width to sample the signal after integration	1.0	µs
t_{DATA}	Time to read out each pixel level at 6.2 MP/s	161	ns
t_{READ}	Time to read out 376 columns per output at 6.2 MP/s	60.65	µs
t_{ROW}	Time to read and read out one complete row at 6.2 MP/s	66.65	µs
$t_{THIS\ INTEGRATION}$ and $t_{NEXT\ INTEGRATION}$	Effective integration time	~ 133	ms
t_1	Minimum setup time from stable row address to SEL rising edge. RST must be high during this time and for the following t_2.	0.5	µs
t_2	Hold time on RST to avoid a soft reset from SEL feed through.	~ 100	ns
t_3	Suggested time between RST falling edge and t_{SHR}	0.4	µs
t_4	Suggested time between t_{SHR} and t_{TRA}	0.5	µs
t_5	Suggested time between t_{TRA} and t_{SHS}	0.5	µs
t_6	Suggested time between t_{SHS} and SEL falling edge	0.5	µs
t_7	Suggested time between SEL falling and C_ADDR_EN rising edges	0.5	µs
t_8	Minimum time between SEL falling edge and row address change	0.5	µs
t_9	Setup time of C_ADDR_EN to new column address input	~ 100	ns
t_{10}	Hold time from last column address to C_ADDR_EN falling edge	~ 100	ns

Table 4: Typical timing values.

These timings are used as the default for the measured results, unless otherwise described.

Transfer pulse width t_{TRA} as given in Table 4 (1 µs) will give a lag level as in Table 1 (1 % at 50 % Q_{LIN}). Other pulse widths may be used; shorter will give more lag especially at larger signal levels and longer will give less lag at all levels.

DEVICE OPERATION

As shown in Figure 7, the typical timing diagram, each row of pixels has its own integrate and read timing, giving the output of all rows in a sequence. If the row address is steadily incremented or decremented this gives a rolling effect and the mode is called a rolling shutter. By processing the rows one at a time, it is simple to use external subtraction to have the lowest read noise by CDS.

A rolling shutter exposes and reads the pixel rows in turn, with their integration times between the reads in successive frames, giving a steady flow of signal, but the timing of each frame overlapping the preceding and following frames, as in Figure 8.
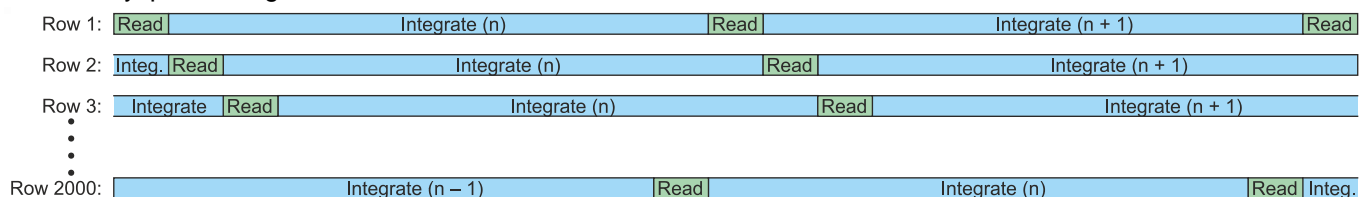

Figure 7: Maximum frame rate rolling shutter.

It can be seen that the rows for each frame are all captured at slightly different times. This can give distortion in the image if there is significant movement.

If a longer integration time is required to capture more signal, the rows will become more synchronous, as in Figure 9.
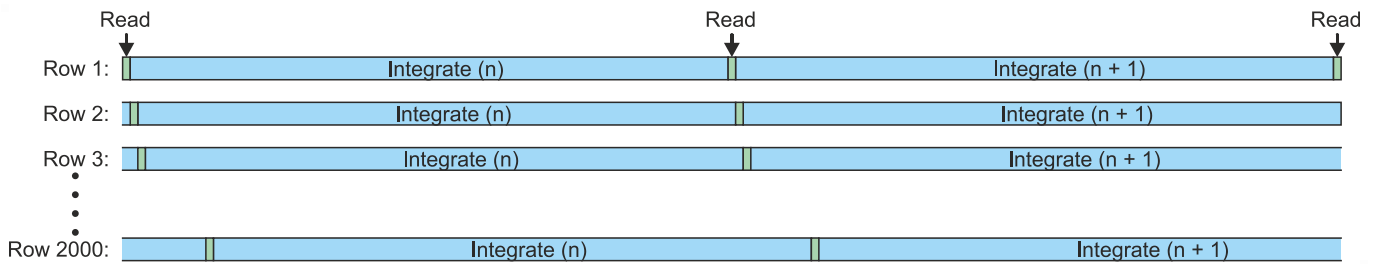

Figure 8: Low frame rate rolling shutter.

OPERATING CONDITIONS

The power supplies used to characterise the CIS115 are summarised in Table 5:

Symbol	Description	Value			Unit
		Min.	**Typ.**	**Max.**	
T	Operating temperature – see note below	−55	20	60	°C
VDIG_CS	Digital power supply to column select	3.0	3.3	3.6	V
VDIG_RS	Digital power supply to row select	3.0	3.3	3.6	V
VANA_RD_1	Analogue power supply to read circuits	3.15	3.3	3.45	V
VANA_RD_2					
VANA_OP1	Analogue power supply to output buffer 1	3.15	3.3	3.45	V
VANA_OP2	Analogue power supply to output buffers 2, 3 and 4	3.15	3.3	3.45	V
VRESET	Select and reset driver supply to row drivers	3.4	3.6	3.8	V
VTRA	Supply used to drive the TG control gate	3.15	3.3	3.45	V
VREFR_1	Reset level power supply for pixels	2.8	2.9	3.0	V
VREFR_2					
VPIX_1	Source follower power supply for pixels	3.15	3.3	3.45	V
VPIX_2					

Table 5: CIS115 operating temperature and supplies.

Note: This image sensor will survive and operate at 60 °C, but the dark current will be very high, leading to very poor image quality. Recommended operating temperature is at or below 20 °C. Even at 90 °C the image sensor will survive and operate, but every pixel will saturate by dark current at the shortest full frame integration time.

The two digital supplies VDIG_CS and VDIG_RS are separate in the CIS115, but may be driven by the same external supply, VDIG. Similarly the four analogue supplies VANA_RD_1, VANA_RD_2, VANA_OP_1 and VANA_OP_2 may be driven by the same external supply VANA. Note that as VANA_RD_1 is internally connected to VANA_RD_2 on the image sensor this is the preferred plan. If both VDIG and VANA are to come from the same power source there must be significant filtering to prevent the digital noise from degrading the analogue signals.

VRESET sets the upper level of the drivers to the select and reset transistors in the pixels, so to ensure a hard reset the level is often higher than the main supplies.

VTRA sets the upper level of the drivers to the transfer transistors in the pixels, so to avoid lag the level should be controlled to a tighter tolerance than needed for other supplies.

VREFR_1 and VREFR_2 (connected together on-chip) drive the level on the drains of the reset transistors in the pixels and so need to be at a lower potential than VRESET to ensure a hard reset.

VPIX_1 and VPIX_2 (connected together on-chip) drive the level on the drains of the source follower transistors in the pixels and so need to be low noise. Provided the level is in the range in Table 5, the exact potential is often not critical.

End users are expected to adjust the supply levels to optimise performance in their application. This is particularly important for VRESET, VTRA, VREFR_1, VREFR_2, VPIX_1 and VPIX_2. Levels lower than given in the Min. column in Table 5 can be preferred in some applications.

In addition to the power supplies there are also two current biases, IPIX and IREAD. These are input as currents to allow each application to use an appropriate accuracy. Both drive nmos current mirrors and so take current from a positive supply, such as VANA and pass it to ground through the current mirror.

IPIX is used to set the pull-down current on each pixel column output track to IPIX × ⅓ by sizing the transistors in this path. The gate bias for these pull-down transistors is vnbias and may be monitored through the test circuit. To more directly measure the column current a pull-up test current Itest_pix at IPIX

× ⅓ is generated in the IPIX bias block and this may also be monitored through the test circuit.

IREAD is used to set several pull-up and pull-down currents in the read path, including the output buffers. The gate bias for the pull-ups is vpbias and may be monitored through the test circuit. As with IPIX, a pull-up test current Itest_read at IREAD × 1 is generated in the IREAD bias block and this may also be monitored through the test circuit.

Both IPIX and IREAD can be set at a lower current to reduce power consumption or to a higher current for faster output settling time.

Symbol	Description	Value (µA)		
		Min.	Typ.	Max.
IPIX	Bias current for column pull-down	4.0	8.0	30.0
IREAD	Bias current for read circuits (pull-up and pull-down) and for output buffers	16	60	100

Table 6: CIS115 bias currents.

Row and column address decoders use a low accuracy current source based on an on-chip resistor. This generates a bias voltage "vdec" to drive the pmos current sources in these decoders. The vdec bias may be monitored through the test circuit.

Row and column select

Gray coded rather than binary coded addresses are used for both row and column addresses so each increment is a one bit change to minimise any disturbance to the image signal levels and also so any timing skew cannot generate decode glitches.

Parallel buses are used so there is no serial to parallel conversion and hence no latches that may be prone to Single Event Upset in the presence of heavy ion radiation. This also allows the addresses to jump in value and so reduce the image readout to one or more ROI and with a higher frame rate.

To convert binary addresses to Gray code is very straightforward:

If B[n:0] is the binary bit array, with n as MSB and 0 as LSB, and G[n:0] is the Gray code bit array,

For Binary to Gray conversion:

G[n] = B[n]

for i = n − 1 downto 0:

G[i] = B[i + 1] xor B[i]

where downto means process the bits in the order from MSB to LSB and xor is the exclusive-OR function.

Row numbers are from 1 to 2000 so the full algorithm to go from required row number to input address is: subtract one, convert to binary and then convert to Gray code. Table 7 gives some examples of Gray codes in the normal address range. Table 8 gives all Gray codes for the special addresses for test access.

As shown in Figure 10, the column numbering is from right to left, as is common for back thinned image sensors – in the design database the order is drawn left to right, then the back thinning results in a left – right flip.

Row addresses for pixels

R_ADDR[10]	R_ADDR[9]	R_ADDR[8]	R_ADDR[7]	R_ADDR[6]	R_ADDR[5]	R_ADDR[4]	R_ADDR[3]	R_ADDR[2]	R_ADDR[1]	R_ADDR[0]	Select
0	0	0	0	0	0	0	0	0	0	0	Row 1 (bottom)
0	0	0	0	0	0	0	0	0	0	1	Row 2
0	0	0	0	0	0	0	0	0	1	1	Row 3
0	0	0	0	0	0	0	0	0	1	0	Row 4
0	0	0	0	0	0	0	0	1	1	0	Row 5
0	0	0	0	0	0	0	0	1	1	1	Row 6
0	0	0	0	0	0	0	0	1	0	1	Row 7
0	0	0	0	0	0	0	0	1	0	0	Row 8
0	0	0	0	0	0	0	1	1	0	0	Row 9
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	0	0	0	0	1	0	1	0	0	1	Row 1999
1	0	0	0	0	1	0	1	0	0	0	Row 2000 (top)

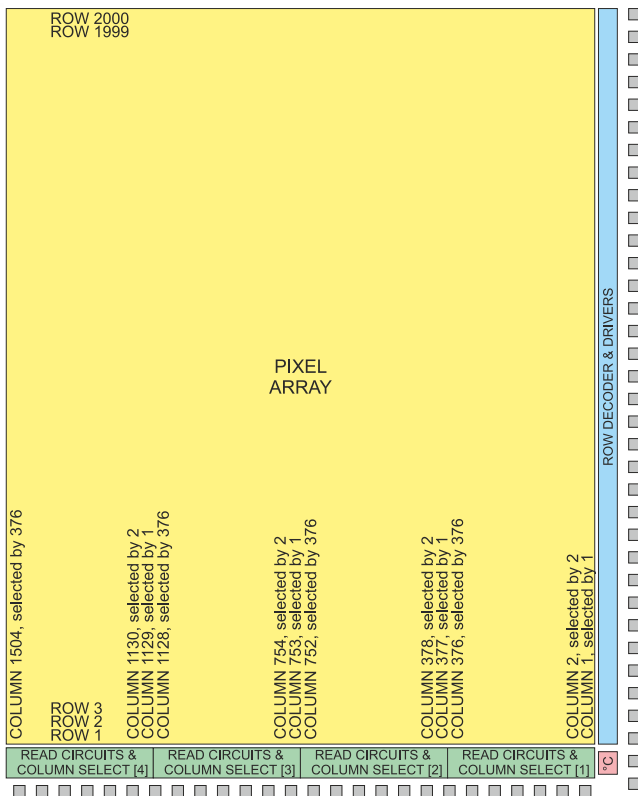*Table 7: Gray codes for pixel row addresses.*

Figure 9: Numbering of CIS115 rows and columns.

Electrical transfer function test mode

As a means to check the operation of the support electronics, it is possible to plot the transfer function of the whole of the readout path from photodiodes to IMAGEREF[4:1] and IMAGESIG[4:1] pins, by using a test mode. Set any one row address from the normal row addresses in Table 7 and drive TRA to low and SEL to high (see below for an alternative), then drive VREFR alternately to each of two levels, with pulses on RST then SHR at one VREFR level and pulses on RST then SHS at the other level to put the effect of both VREFR levels on vr and vs (see Figure 6). These levels are then output on IMAGEREF[4:1] and IMAGESIG[4:1] when a column address is selected. To more accurately see the transfer function as in real imaging, the SEL pin can be pulsed as in Figure 7 and Table 4 to include the select feedthrough.

Row addresses for test control

Row addresses at 10000111000_G (= 2000_{10} for row 2001) and above do not select a row of pixels, but some are used to select one of several analogue levels to output as a test mode. These are listed in Table 8:

R_ADDR[10]	R_ADDR[9]	R_ADDR[8]	R_ADDR[7]	R_ADDR[6]	R_ADDR[5]	R_ADDR[4]	R_ADDR[3]	R_ADDR[2]	R_ADDR[1]	R_ADDR[0]	Equivalent row number of the test address	Selection	Comments
1	0	0	0	0	0	0	0	0	0	0	2048	vnbias to ATEST1	From IPIX buffer
1	0	0	0	0	0	0	0	0	0	1	2047	vpbias to ATEST1	From IREAD buffer
1	0	0	0	0	0	0	0	0	1	1	2046	vdec to ATEST1	From internal reference
1	0	0	0	0	0	0	0	0	1	0	2045	Itest_pix to ATEST1	Extra copy of IPIX
1	0	0	0	0	0	0	0	1	1	0	2044	Itest_read to ATEST1	Extra copy of IREAD
1	0	0	0	0	0	0	0	1	1	1	2043	vtestbuf to ATEST1	ATEST2 drives vtestbuf
1	0	0	0	0	0	0	0	1	0	1	2042	column buffers to image outputs	Modified dummy pixel row drives column buffer
1	0	0	0	0	0	0	0	1	0	0	2041	output buffers to image outputs	ATEST2 drives buffers through select switch

Table 8: Row address Gray codes for test access.

Row addresses not listed in either Table 7 or Table 8 will not drive access to any part of this image sensor, so the pixel column outputs will be pulled to ground by the read circuits. Using the column select circuit with a non-valid row address to output levels on IMAGEREF[4:1], IMAGESIG[4:1] or ATEST1 will give a level near the appropriate AGND_OP_1 or AGND_OP_2.

Bias voltages vnbias, vpbias, vdec and vtestbuf are described in the section OPERATING CONDITIONS, along with the two test currents Itest_pix and Itest_read. They are all listed in this section as the method to access them is by row addresses.

Bias	Expected value	Comment
vnbias	~1.0 to 1.1 V	Depends on IPIX.
vpbias	~2.3 to 2.5 V	Depends on IREAD.
vdec	~1.9 to 2.2 V	Depends on process parameters.
Itest_pix	IPIX / 3	
Itest_read	IREAD × 1	
vtestbuf	0 to 3.3 V	Depends on input to ATEST2.

Table 9: Typical values for the test mode output.

Row address 10000000101_G is used to read a row of dummy pixels which have been modified to disconnect the source followers and to drive the drains of the select transistors directly from the sources of the reset transistors. This allows the level on VREFR_1 and VREFR_2 to be driven onto the corresponding column buffers and the performance of these buffers and the output buffers to be measured. Pin TRA should be held at low during this test.

Row address 10000000100_G is used to connect the analogue test input ATEST2 to the input of each

Column addresses

Gray coded values are again used, but each set of 376 columns repeats the addresses, as in Table 10.

Column addresses at 111000101_G and above select no signal path, so each IMAGEREF[4:1] and

output buffer to test the performance of just these buffers. For this test C_ADDR_EN must be held low to prevent any column buffers interfering with the test.

Figure 11 shows the main test multiplexor, with four bias voltages selected by transmission gates to then drive a voltage buffer and the test output ATEST1. The two test currents can also be selected and then drive the pin directly. In image sense mode the node "outmux" is tied to ground to minimise noise coupling.
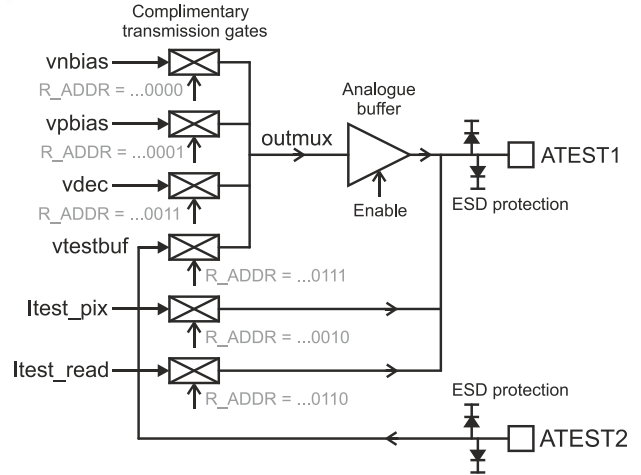

Figure 10: Concept diagram of test multiplexor.

IMAGESIG[4:1] will be driven to the pre-chargestate, an internally set level around mid-way between the appropriate VANA_OP and AGND_OP.

C_ADDR[8]	C_ADDR[7]	C_ADDR[6]	C_ADDR[5]	C_ADDR[4]	C_ADDR[3]	C_ADDR[2]	C_ADDR[1]	C_ADDR[0]	Selection in rightmost set of columns	Parallel selections
0	0	0	0	0	0	0	0	0	Temp. sensor in right block	None
0	0	0	0	0	0	0	0	1	Column 1 (right of block)	Columns 377, 753 and 1129
0	0	0	0	0	0	0	1	1	Column 2	Columns 378, 754 and 1130
0	0	0	0	0	0	0	1	0	Column 3	Columns 379, 755 and 1131
0	0	0	0	0	0	1	1	0	Column 4	Columns 380, 756 and 1132
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	0	0	1	1	0	0	Column 375	Columns 751, 1127 and 1503
1	1	1	0	0	0	1	0	0	Column 376 (left of block)	Columns 752, 1128 and 1504

Table 10: Gray codes for BSI column addresses.

Temperature sensor

An on-chip temperature sensor is included to measure the temperature of the silicon. This reference is used to drive a column buffer when selected by column address 000000000_G and then drives the IMAGESIG[1] output buffer to a level around 1.3 V at 20 °C. At the same time a reference voltage level is output on IMAGEREF[1] at around 0.8 V at 20 °C.

The difference IMAGEREF[1] – IMAGESIG[1] indicates the temperature, around –0.5 V at 20 °C.

The other three pairs of outputs do not have a selected column and so will be driven to an internally set level around mid-way between the appropriate VANA_OP and AGND_OP.

Symbol	Description	Value			Unit
		Min.	Typ.	Max.	
T_{SENSE}	Useful temperature range	–20		+60	°C
T_{SLOPE}	Output voltage change with temperature: IMAGEREF[1] – IMAGESIG[1]		–1.34		mV/°C
$T_{ACCURACY}$	Accuracy over T_{SENSE} range	–1		+1	°C
	Non-linearity over T_{SENSE} range		±0.6		%
PSRR	Power supply rejection ratio at 1 kHz		55		dB
t_{START}	Settling time from selection to meeting specifications			1	ms

Table 11: Simulated performance of temperature sensor.

ELECTRICAL AND MECHANICAL INTERFACE

Package detail

The package is a 140 pin aluminium nitride ceramic pin grid array as in Figure 12 and Figure 13. The central area is free of pins to allow the use of a cold finger for cooling.

Pin numbering on package

Figure 12 shows the pin numbering viewed from image input side, with pins behind. This also shows the nominal position of the chip in the package.

Mechanical details

Image area: 10.528 mm × 14.000 mm.

Nominal sawn silicon size: 13.140 mm × 16.615 mm.

Package size: 48.26 mm square.

Number of used pins: 61.

Nominal focal plane height, above package bottom surface: 2.64 mm.

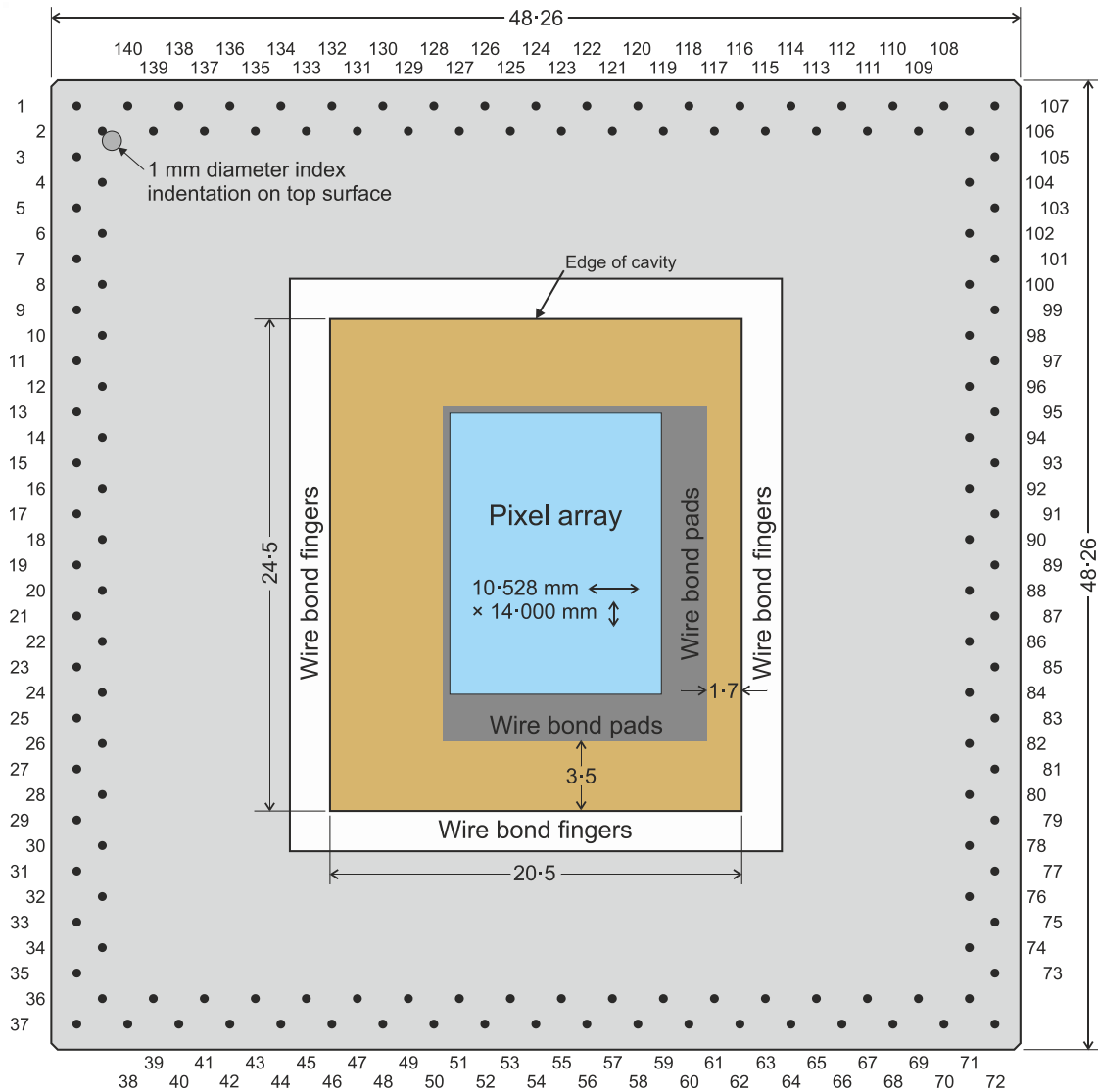Flatness: maximum 10 µm (peak to valley).

Figure 11: Package details and pin numbering (dimensions in mm).

Note: Both the chip and the pixel array are offset from the centre of the package, details are given in Figure 12, Figure 14 and Figure 15.

All bond wires are on the bottom and right edges of the chip – none on the top (no package wire bond fingers) or left (package wire bond fingers are present, but not used) edges.

For delivery, a temporary window is attached over the package cavity to offer some mechanical protection. This window should be removed for use in the final applications.
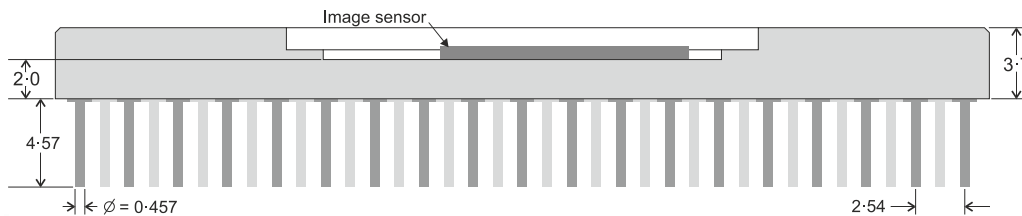

Figure 12: Edge view of package (dimensions in mm).

Dimensions in Figure 13 are nominal. Fired ceramic changes its thickness during the manufacturing process, so there is a ±10 % tolerance on both the 2.0 mm height of the chip mounting plane above the package bottom surface and on the 3.7 mm total thickness.

Position of the pixel array

Using the edges of the cavity as a reference, the nominal position of the centre of the pixel array is as in Figure 14:
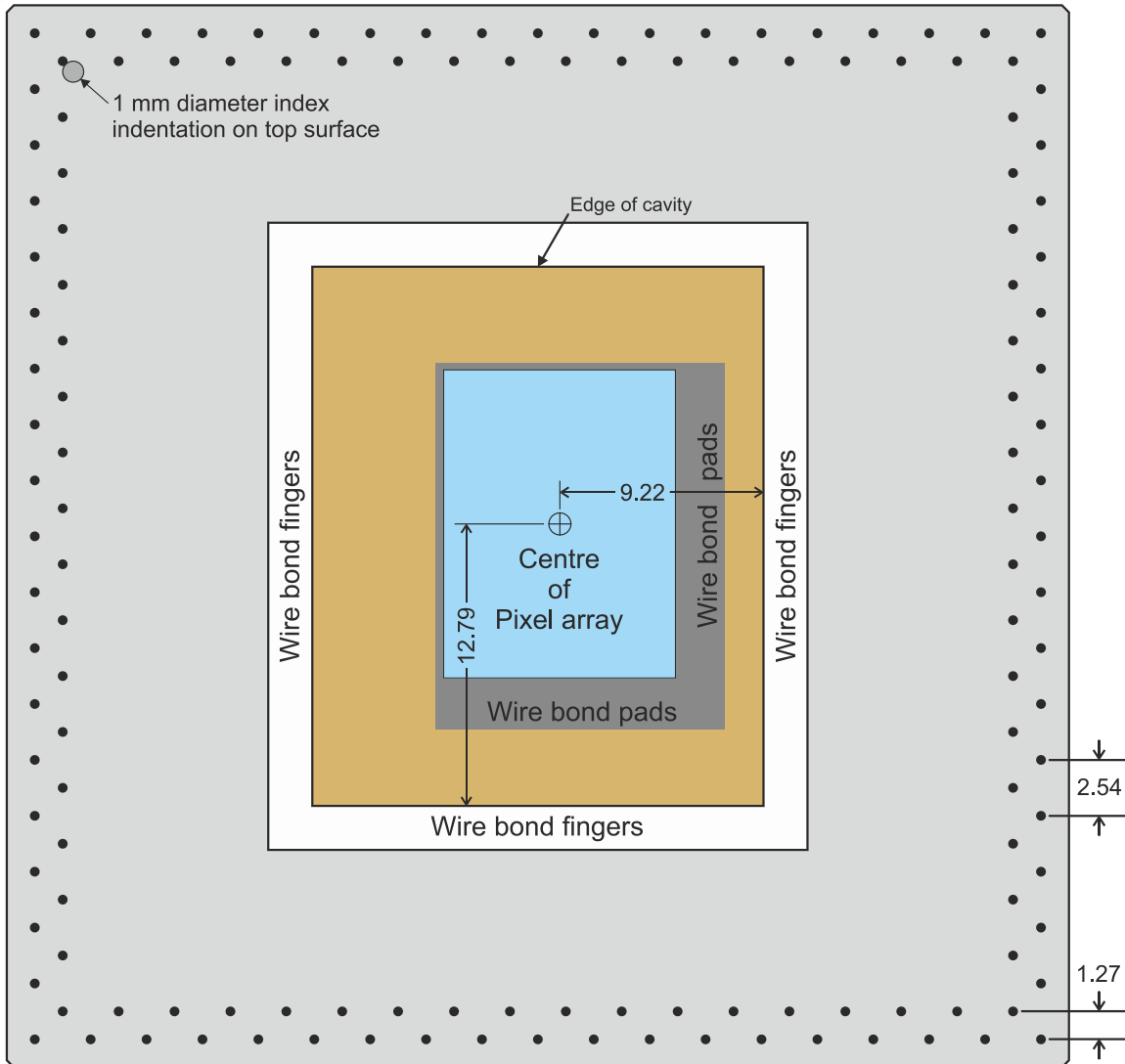

Figure 13: Position of pixels relative to edge of package cavity (dimensions in mm).

Due to both the manufacturing methods used for ceramic packages and those for chip alignment, each dimension has a large tolerance.

To measure the precise location of the pixels, relative to package features such as edges or pins, the alignment cross should be used as in Figure 15. This cross is on the silicon front face and so will give better than ±1 µm accuracy and is made visible by a hole etched in the back face.
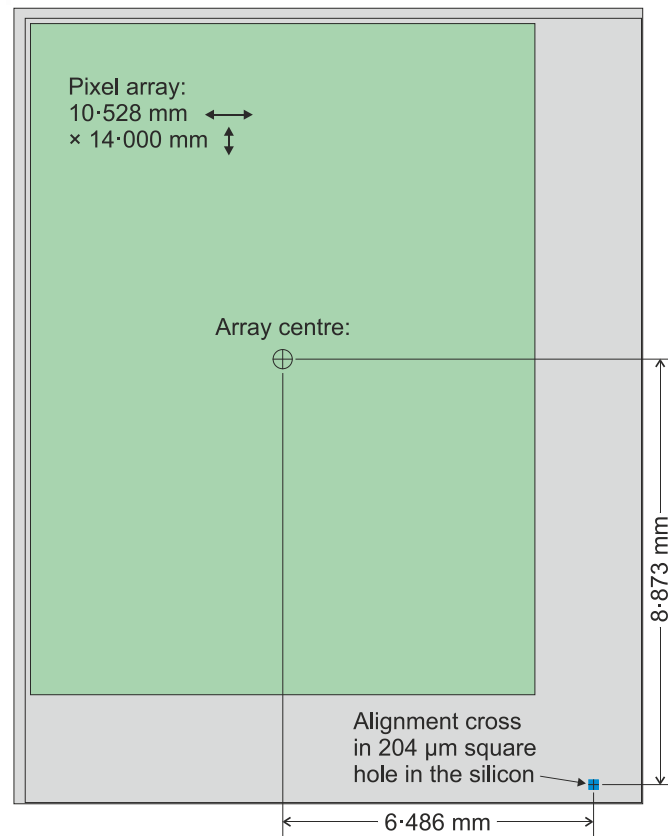
Figure 14: Position of pixels relative to alignment cross.

Pin list

The pin numbering and layout for the PGA package is shown in Figure 12. Each pin has the name and function as described in Table 12.

Note that some package pins do not connect to any tracks in the package and that some pins do connect to tracks, but are not used for this device.

Pin No.	Name	Description
1 to 35	Not used	–
36 & 37	No connection	–
38 to 43	Not used	–
44	VPIX_2	Power to pixel source followers
45	AGND_RD_2	Ground to read circuits
46	VANA_RD_2	Power to read circuits
47	VREFR_2	Power to pixel reset drive
48	ASUB_2	Substrate, especially to pixels
49	IMAGEREF[4]	Reference output 4
50	IMAGESIG[4]	Signal output 4
51	AGND_OP_2	Ground to output buffers 2, 3 and 4
52	VANA_OP_2	Power to output buffers 2, 3 and 4
53	IMAGEREF[3]	Reference output 3
54	No connection	–
55	IMAGESIG[3]	Signal output 3
56	DGND_CS	Ground to column select circuits
57	VDIG_CS	Power to column select circuits

Pin No.	Name	Description
58	IMAGEREF[2]	Reference output 2
59	IMAGESIG[2]	Signal output 2
60	AGND_OP_1	Ground to output buffer 1
61	VANA_OP_1	Power to output buffer 1
62	IMAGEREF[1]	Reference output 1
63	IMAGESIG[1]	Signal output 1
64	ASUB_1	Substrate, especially to pixels
65	VREFR-1	Power to pixel reset drive
66	AGND_RD_1	Ground to read circuits
67	VANA_RD_1	Power to read circuits
68	IREAD	Reference current for read circuits
69	IPIX	Reference current for column pull-downs
70	VPIX_1	Power to pixel source followers
71 & 72	No connection	–
73	SHR	Sampling signal for reference level
74	SHS	Sampling signal for signal level
75	ENABLE	Enable all analogue

Pin No.	Name	Description
		blocks
76	ATEST2	Test
77	ATEST1	Test
78	C_ADDR_EN	Column address enable
79	C_ADDR[0]	Column address bit 0
80	C_ADDR[1]	Column address bit 1
81	C_ADDR[2]	Column address bit 2
82	C_ADDR[3]	Column address bit 3
83	C_ADDR[4]	Column address bit 4
84	C_ADDR[5]	Column address bit 5
85	C_ADDR[6]	Column address bit 6
86	C_ADDR[7]	Column address bit 7
87	C_ADDR[8]	Column address bit 8
88	SEL	Row select, gated with row address
89	RST	Row reset, gated with row address
90	TRA	Transfer, gated with row address
91	VTRA	Power to tra(m) drivers
92	DGND	Ground to sel(m), rst(m) and tra(m) drivers
93	VRESET	Power to rst(m) drivers

Pin No.	Name	Description
94	DGND_RS	Ground to row select circuits
95	VDIG_RS	Power to row select circuits
96	R_ADDR_EN	Row address enable
97	R_ADDR[0]	Row address bit 0
98	R_ADDR[1]	Row address bit 1
99	R_ADDR[2]	Row address bit 2
100	R_ADDR[3]	Row address bit 3
101	R_ADDR[4]	Row address bit 4
102	R_ADDR[5]	Row address bit 5
103	R_ADDR[6]	Row address bit 6
104	R_ADDR[7]	Row address bit 7
105	R_ADDR[8]	Row address bit 8
106	R_ADDR[9]	Row address bit 9
107	R_ADDR[10]	Row address bit 10
108 & 109	Not used	–
110 to 138	No connection	–
139 & 140	Not used	–

Table 12: Pin list and functions.

ELECTRICAL INTERFACE CHARACTERISTICS

In this table VDIG refers to VDIG_CS supply for the digital inputs C_ADDR_EN, C_ADDR[8:0], SEL, RST and TRA or to VDIG_RS supply for digital inputs R_ADDR_EN, R_ADDR[10:0], SHR, SHS and ENABLE. Some of these signals are then buffered to other supplies inside the image sensor to correctly drive the pixels or read circuits.

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
$V_{IN\_DIG\_LO}$	Address and timing input voltage low level	−0.3		$0.3 \times$ VDIG	V
$V_{IN\_DIG\_HI}$	Address and timing input voltage high level	$0.7 \times$ VDIG		VDIG + 0.3	V
C_{IN}	Input pin capacitance			5	pF
I_{LEAK}	Input pin leakage current (all inputs except IPIX and IREAD)			10	µA
IPIX	See Table 6.				
IREAD	See Table 6.				

Table 13: Electrical interface characteristics.

Output buffers

All eight video output buffers are standard five transistor operational amplifiers connected as voltage followers, as in Figure 16:

These have the advantage over simple source follower output stages, as sometimes used for the analogue outputs on image sensors, of having an accurate unity voltage gain without significant extra noise, to give a better overall SNR.
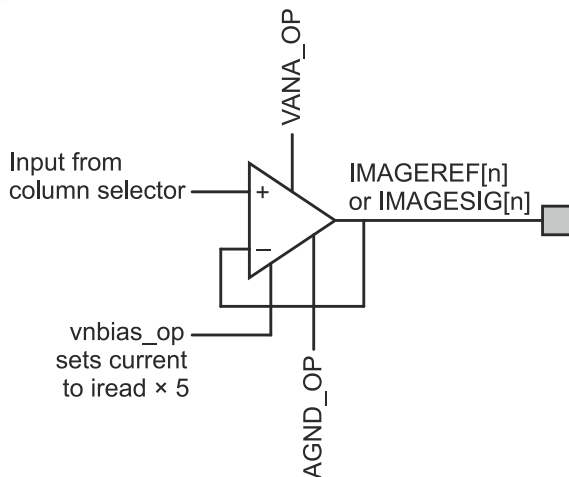

Figure 15: Output buffer structure.

Output buffer settling characteristics

To minimise the noise contribution due to the output buffers a low current design was chosen. This means the load capacitance must be kept very low if the typical or maximum pixel rate is required. Figure 17 shows the effect of adding a capacitor to the minimum load of CIS115 itself plus socket, PCB trace and 'scope probe to give total loads of 22 pF (dark blue), 37 pF (magenta), 69 pF (yellow) or 122 pF (cyan). The settling time given in Table 1 applies with the minimum capacitance on the video outputs. If the external electronics must have a large input capacitance, a buffer between this image sensor and those electronics will help to maintain a high pixel readout rate.

When a low frame rate is adequate the high capacitance of some external electronics may be connected directly to the CIS115 to save adding a buffer.
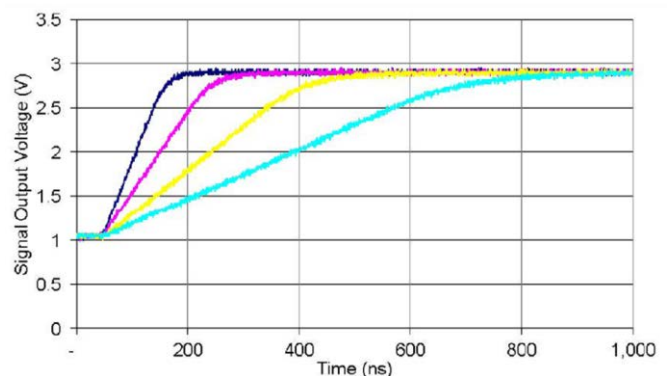

Figure 16: Typical output buffer settling characteristic.

ESTIMATED POWER CONSUMPTION

The power dissipated within the CMOS image sensor is a combination of the static dissipation of the buffers and the dynamic dissipation from the parallel buses and decoders.

With IPIX = 8 µA, IREAD = 60 µA and all VANA and VDIG at 3·3 V, total power is expected to be approximately 40 mW.

TEMPERATURE RANGES

Operating temperature range: see Table 5.

Storage temperature range: see Table 14.

Performance parameters are measured with the device at a temperature of 293 K and, as a result, full performance is only guaranteed at this nominal operating temperature.

Operation or storage in humid conditions may give rise to ice on the surface when the sensor is taken to low ambient temperatures, thereby causing irreversible damage.

Maximum safe rate of heating or cooling: 5 K/min.

ABSOLUTE MAXIMUM RATINGS

These are the limits which if exceeded are likely to cause permanent damage to the device. Operation at these limits is not expected. These limits apply with all ground pins (AGND_RD_1, AGND_RD_2, ASUB_1, ASUB_2, AGND_OP_1, AGND_OP_2, DGND_CS, DGND and DGND_RS) at 0 V.

Symbol	Description or pins	Value			Unit
		Min.	Typ.	Max.	
V_{DIG}	VDIG_CS and VDIG_RS	−0.5	3.3	4.2	V
V_{ANA}	VANA_RD_1, VANA_RD_2, VANA_OP1 and VANA_OP2,	−0.5	3.3	4.2	V
V_{PIXEL_READ}	VTRA and VPIX	−0.5	3.3	4.2	V
V_{PIXEL_RESET}	VRESET	−0.5	3.6	4.2	V
V_{PIXEL_REFR}	VREFR	−0.5	2.9	4.2	V
V_{IN}	Digital input signals	−0.5		V_{DIG} + 0.5	V
T_{STORE}	Storage temperature	−55		+150	°C
T_{SOLDER}	Soldering temperature – see note below.			260	°C
	ESD protection, bare imager, all pins (HBM)	−2		+2	kV

Table 14: Absolute maximum ratings.

Note: Soldering temperature applies for a maximum of 10 s at a minimum of 2 mm from the package and with a minimum of 3 minutes before re-soldering the same pin.

POWER UP or POWER DOWN

When powering the device up or down it is critical that the absolute maximum ratings in Table 13 are met at all times, including the input signal to supply and ground limits. To ensure safe and consistent start-up a recommended sequence is:

(1) Hold R_ADDR_EN, TRA, RST, SEL, C_ADDR_EN, ENABLE, SHS and SHR at low (ground) and IPIX and IREAD at nil current (this is also at ground as the polarity is to source current into the imager). The buses R_ADDR[10:0] and C_ADDR[8:0] and the test input ATEST2 should also be at ground to avoid partially powering the device through the ESD protection diodes.

(2) Drive all supplies (VPIX_1, VPIX_2, VANA_RD_1, VANA_RD_2, VREFR_1, VREFR_2, VANA_OP_1, VANA_OP_2, VDIG_CS, VTRA, VRESET, and VDIG_RS) to their correct levels in any convenient order.

(3) Set IPIX and IREAD to the correct current.

(4) Set ENABLE high to pass bias currents to analogue blocks. A propagation delay of up to 200 µs is expected from ENABLE going high to all circuits being active and ready to image.

(5) Use R_ADDR[10:0] and R_ADDR_EN to select a row.

(6) Use both RST and TRA to clear any accumulated charge.

(7) Repeat (5) and (6) to reset whole imager.

To then capture images:

(8) Use R_ADDR[10:0] with R_ADDR_EN at high to select a row.

(9) Use TRA, RST, SEL, SHS and SHR to read a row.

(10) Use C_ADDR[8:0] with C_ADDR_EN at high to select each column in turn.

(11) Use external subtraction of IMAGESIG[1:4] from IMAGEREF[1:4] to remove kTC noise from the image.

(12) Repeat steps (8) to (11) to read a whole image or use reduced ranges of row and/or column addresses for an ROI.

To shut down cleanly after all required images have been captured:

(13) Set ENABLE low to stop bias currents to analogue blocks.

(14) Set IPIX and IREAD to nil current.

(15) Drive all supplies to ground in any convenient order.

To shut down abruptly it is permitted to do (13), (14) and (15) simultaneously or in any order without damage, but the reset in lines (5) to (7) will be essential at next power-up.

HANDLING CMOS SENSORS

CMOS image sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases, a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full antistatic handling precautions should be taken whenever using, testing or otherwise handling a CMOS sensor or module. These include:

Working at a fully grounded workbench

Operator wearing a grounded wrist strap

Evidence of incorrect handling will invalidate the warranty. All devices are provided with internal protection circuits on input, output and power pins.

The devices are assembled in a clean room environment. Teledyne e2v recommend that similar precautions are taken to avoid contaminating the active surface.

HIGH ENERGY RADIATION

Performance parameters will begin to change if the device is subject to high energy radiation. Characterisation data is held at Teledyne e2v with whom it is recommended that contact be made if devices are to be operated in any high radiation environment.

PART REFERENCE

CIS115-00-g-Mxx

g = cosmetic grade

Mxx = specific part number for option described.

VARIANTS

The CIS115 is made on high resistivity epitaxial silicon, thinned using the Teledyne e2v "enhanced" process. This gives a good balance of visible MTF and of QE at both NIR and UV.

The M33 variant has a "Multi-2" AR coating, which gives a flat QE curve over the visible range and into the NIR, see Figure 1.

The M48 variant has a single layer UV optimised AR coating, which extends usable QE into short wave UV, as shown in Figure 2.

Other coating options (un-coated, single and multi-layer) could be available as custom variants.

Consult Teledyne e2v for further information on these options.