QLS1046A, QLS1026A
Qormino Integrated Multicore communication processor with DDR4

Datasheet DS 60S 217489

Features

- QLS1046A has four cores and QLS1026A has two cores
- 4GB or 8GB of DDR4 with ECC with built-in DDR bus to the processor, achieving 2.1GT/s
- Optimized DDR4 controller configuration provided in the document AN 60S 223060 (available on the product webpage),
- Four 32-bit/64-bit Arm® Cortex®-v8 A72 CPUs
  - Arranged as a single cluster of four cores sharing a single 2 MB L2 cache
  - Up to 1.8 GHz operation
  - Single-threaded cores with 32 KB L1 data cache and 48 KB L1 instruction cache
- Hierarchical interconnect fabric
  - Up to 700 MHz operation
- Data Path Acceleration Architecture (DPAA) incorporating acceleration for the following functions:
  - Packet parsing, classification, and distribution (FMan)
  - Queue management for scheduling, packet sequencing, and congestion management (QMan)
  - Hardware buffer management for buffer allocation and de-allocation (BMan)
  - Cryptography acceleration (SEC)
  - IEEE 1588™ support
- Two RGMII interfaces
- Eight SerDes lanes for high-speed peripheral interfaces
  - Three PCI Express 3.0 controllers
  - One Serial ATA (SATA 6 Gbit/s) controller
  - Up to two XFI (10 GbE) interfaces
  - Up to five SGMII interfaces supporting 1000 Mbps
  - Up to three SGMII interfaces supporting 2500 Mbps
  - Up to one QSGMII interface
  - Supports 10GBase-KR
  - Supports 1000Base-KX
- Additional peripheral interfaces
  - One Quad Serial Peripheral Interface (QSPI) controller
  - One Serial Peripheral Interface (SPI) controller
  - Integrated flash controller (IFC) supporting NAND and NOR flash
  - Three high-speed USB 3.0 controllers with integrated PHY
  - One Enhanced Secure Digital Host Controller supporting SD 3.0, eMMC 4.4, and eMMC 4.5
  - Four I2C controllers
  - Two 16550-compliant DUARTs and six low-power UARTs (LPUARTs)
  - General purpose IO (GPIO), eight Flextimers
  - One Queue Direct Memory Access Controller (qDMA)
  - One Enhanced Direct Memory Access Controller (eDMA)
  - Global programmable interrupt controller (GIC)
  - Thermal monitoring unit (TMU)
- 1415 FC-PBGA package, 26 mm x 44 mm

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1 INTRODUCTION

The QLS1046A is a cost-effective, power-efficient, and highly integrated system-on-chip (SoC) design that extends the reach of the Teledyne e2v value-performance line of QorIQ communications processors. Featuring power-efficient 64-bit Arm® Cortex®-A72 cores with ECC-protected L1 and L2 cache memories for high reliability, running up to 1.8 GHz.

The QLS1046A and QLS1026A processors are perfectly suited for a range of embedded applications such as enterprise routers and switches, linecard controllers, network attached storage, security appliances, virtual customer premise equipment (vCPE), service providers gateways, and single board computers.

This figure shows the block diagram of the chip.

Figure 1. QLS1046A block diagram

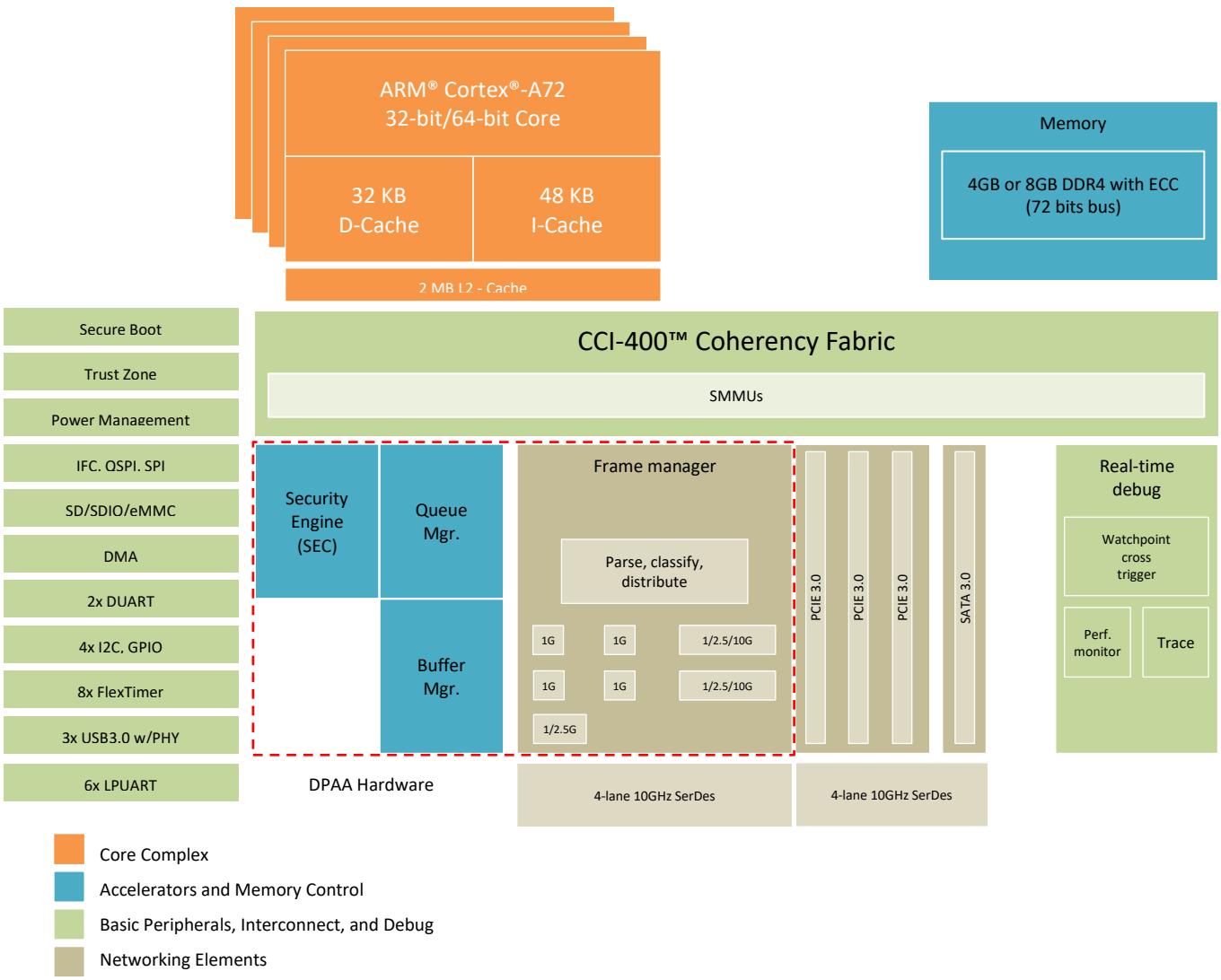

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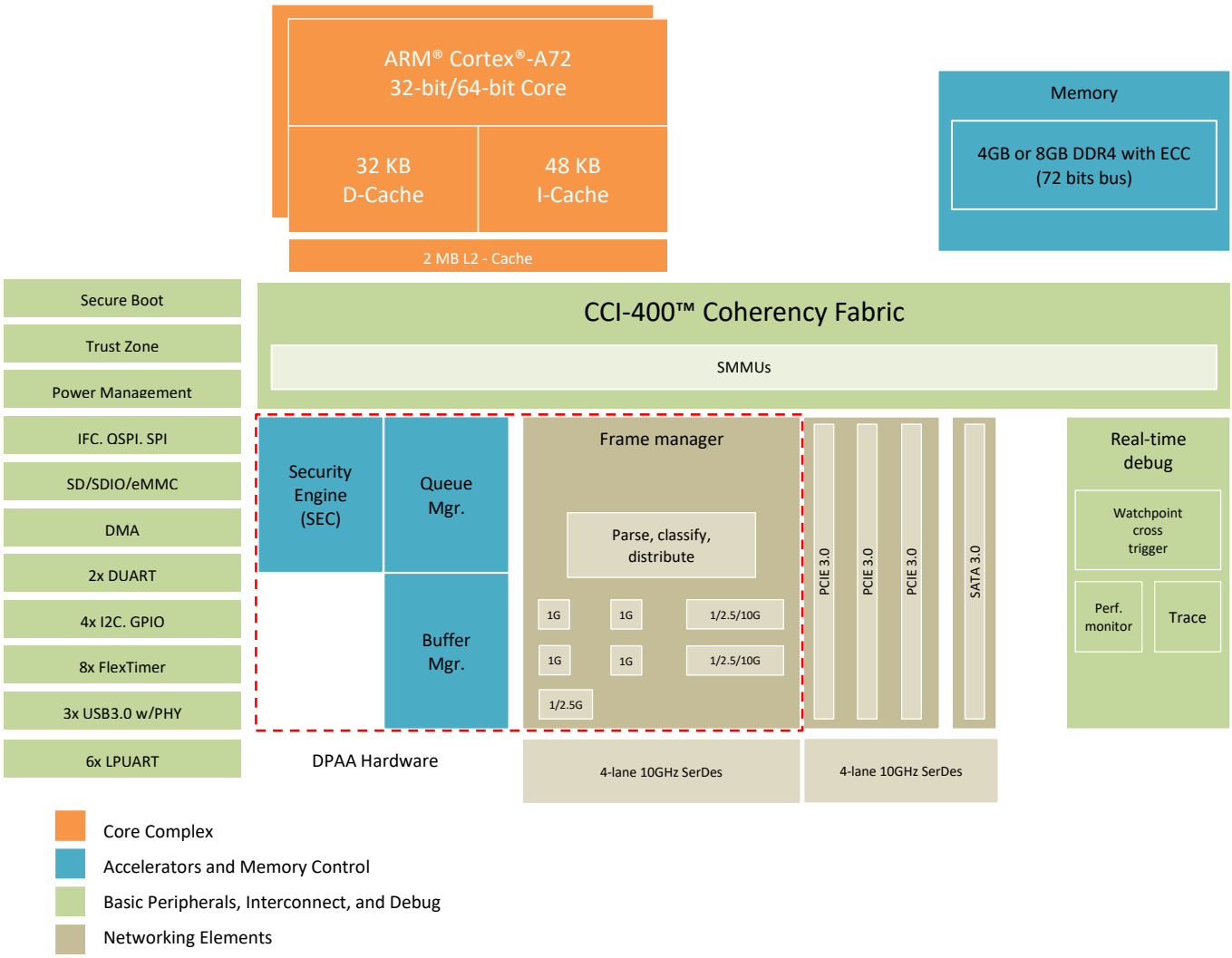
Figure 2. QLS1026A block diagram



2 PIN ASSIGNMENTS

2.1 1415 BGA ball layout diagrams

This figure shows the complete view of the QLS1046A BGA ball map diagram. Figure 4, Figure 5, Figure 6, Figure 7, figure 8 and figure 9 show quadrant views.

Figure 3. Complete BGA Map for the QLS1046A

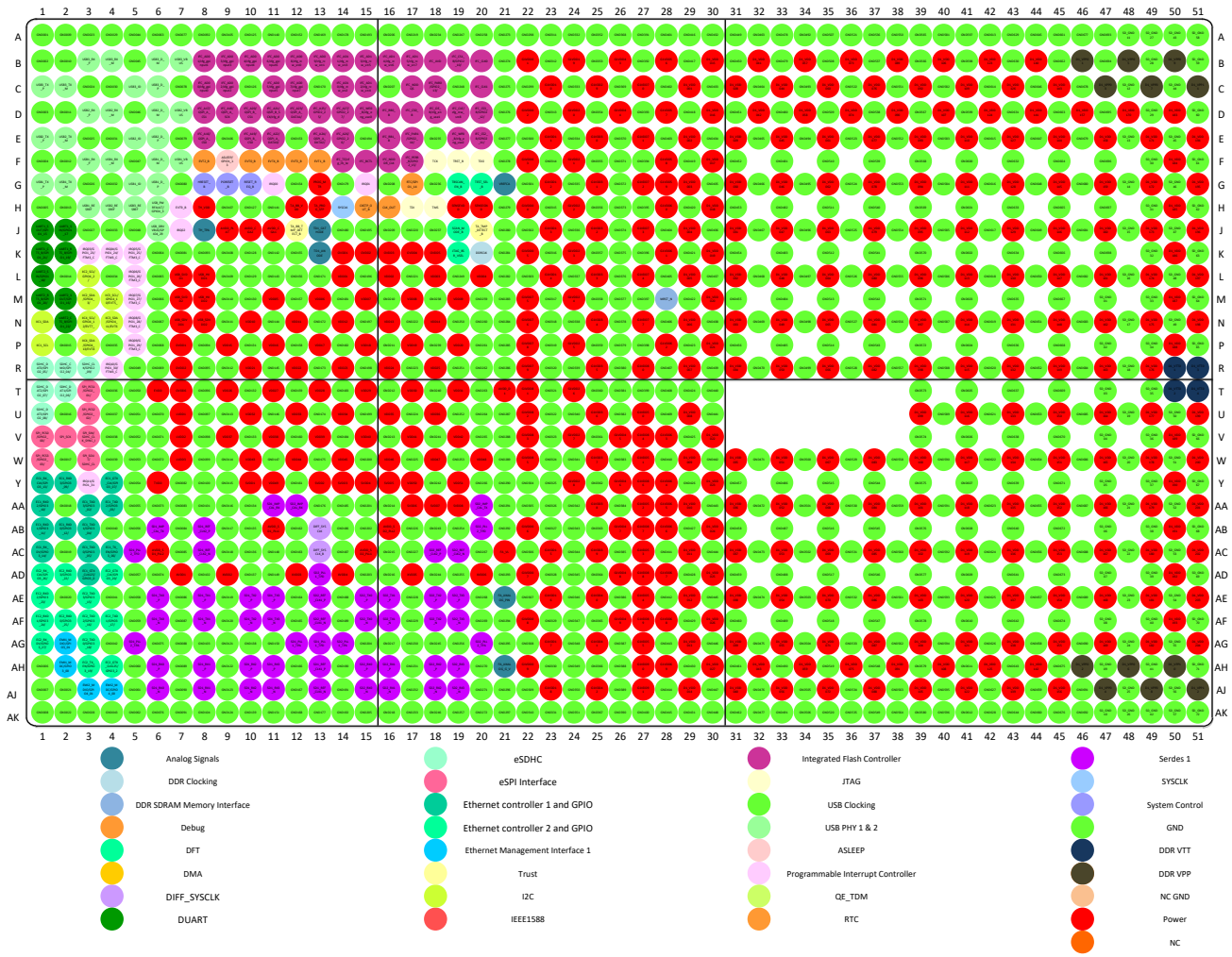


Figure 4. Detail A

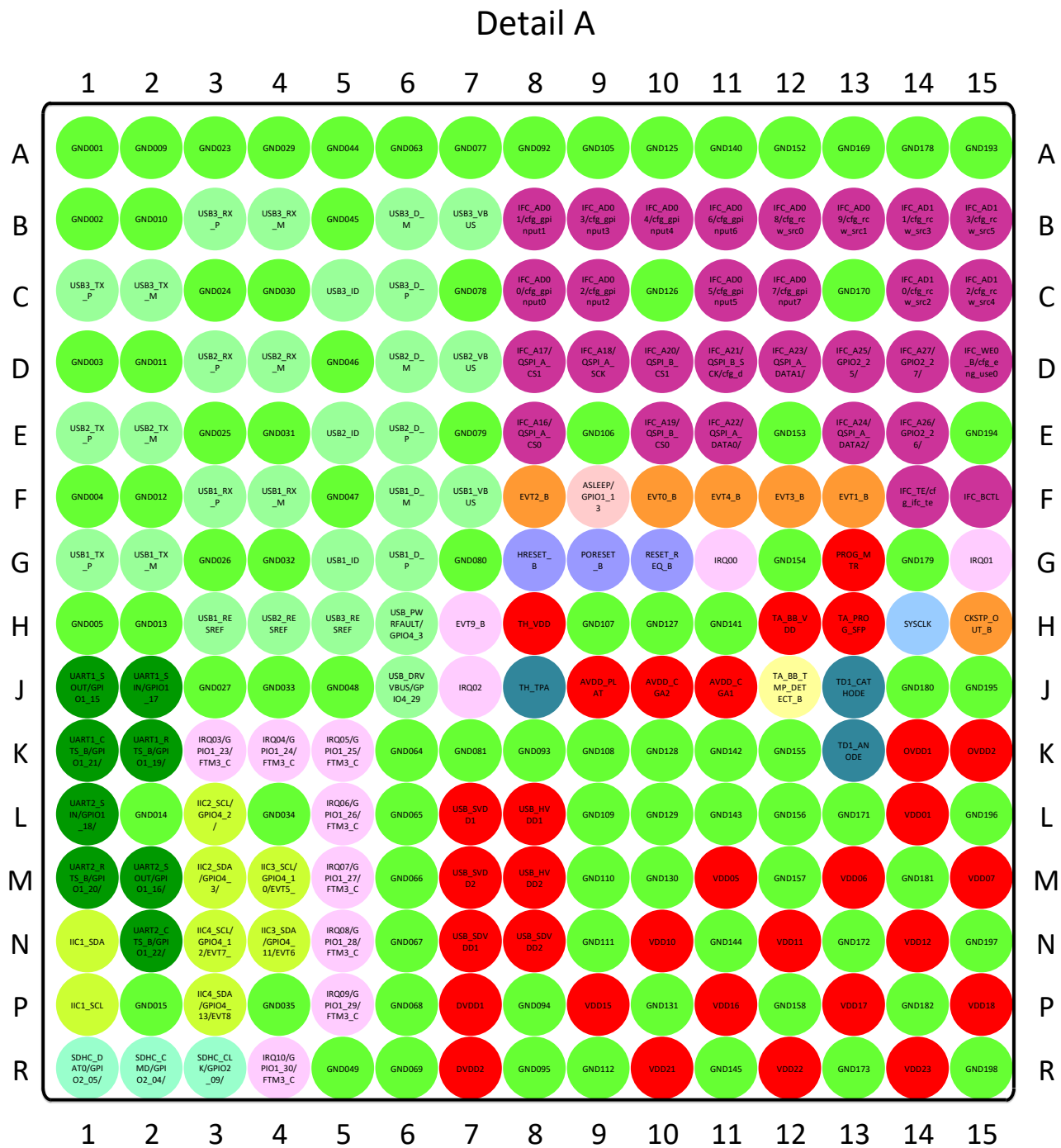


Figure 5. Detail B

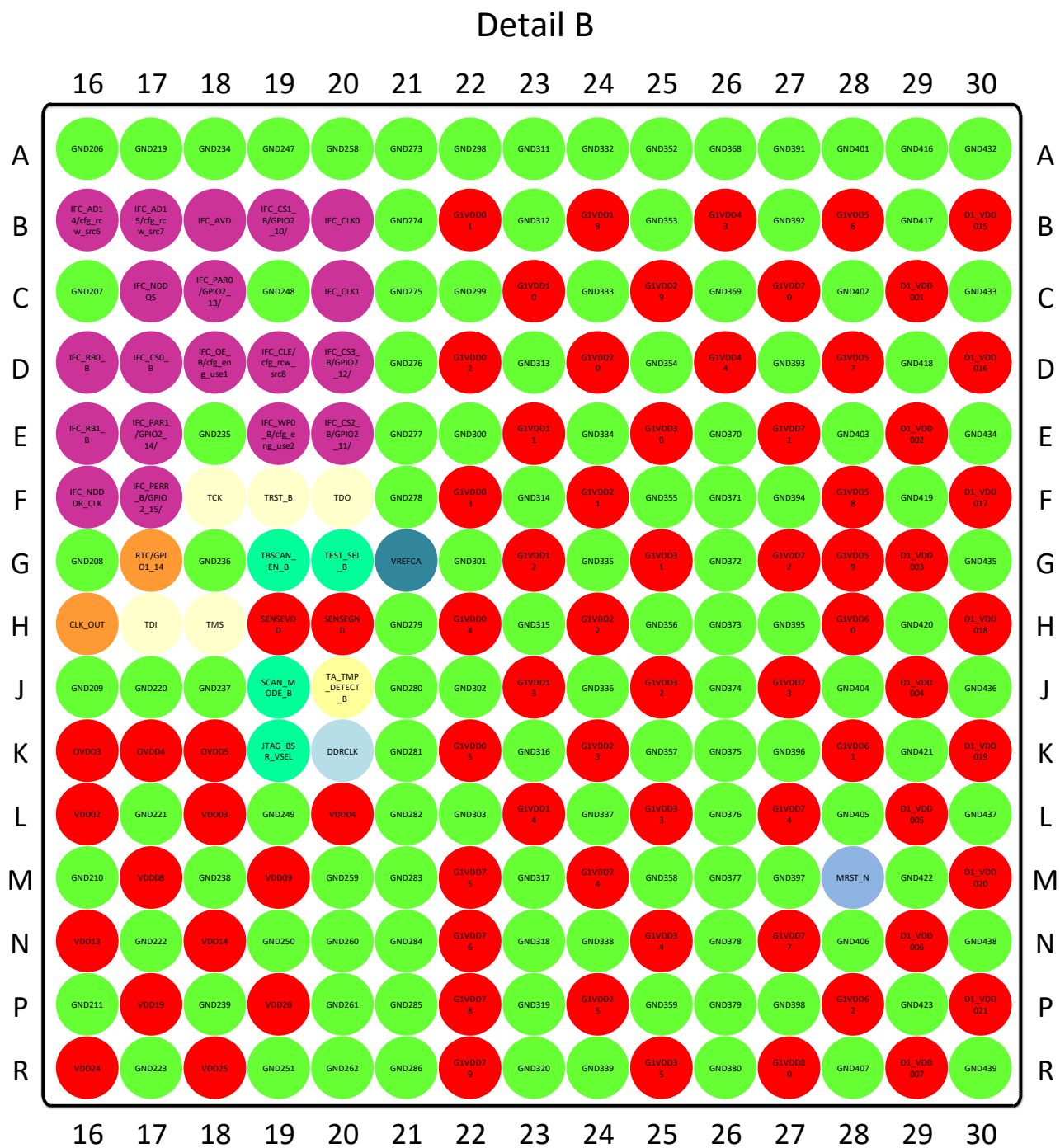


Figure 6. Detail C

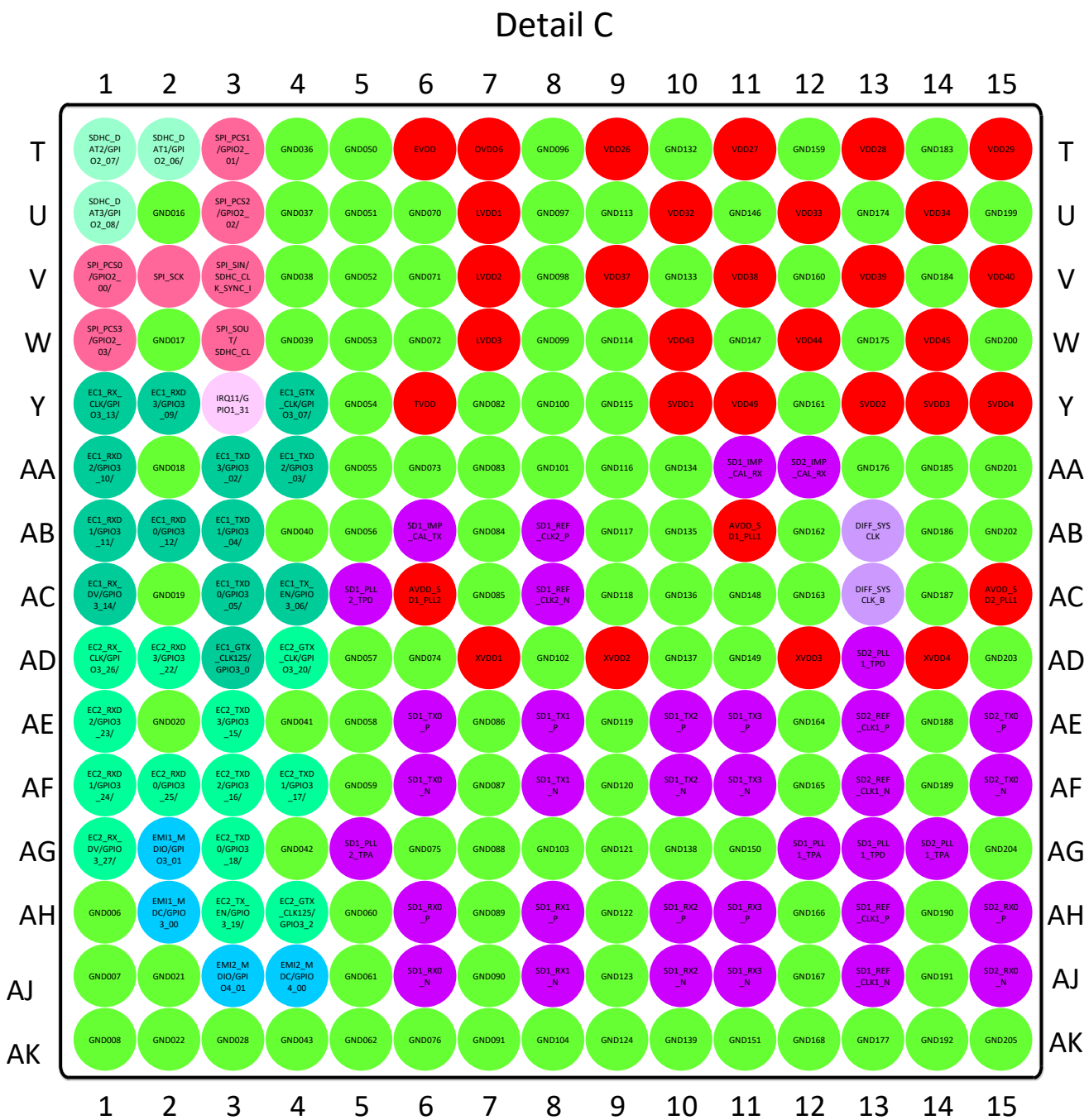


Figure 7. Detail D

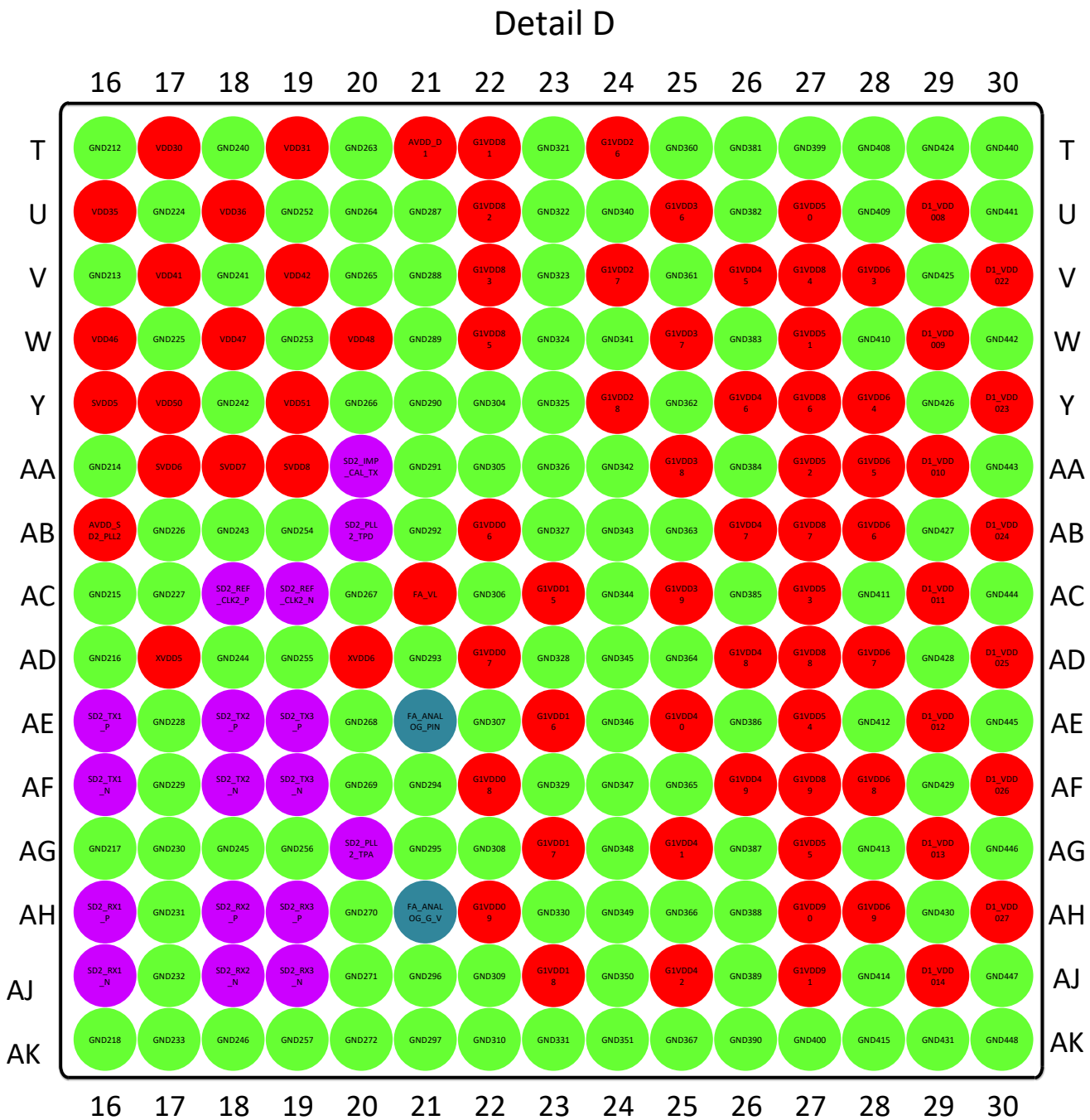


Figure 8. Detail E

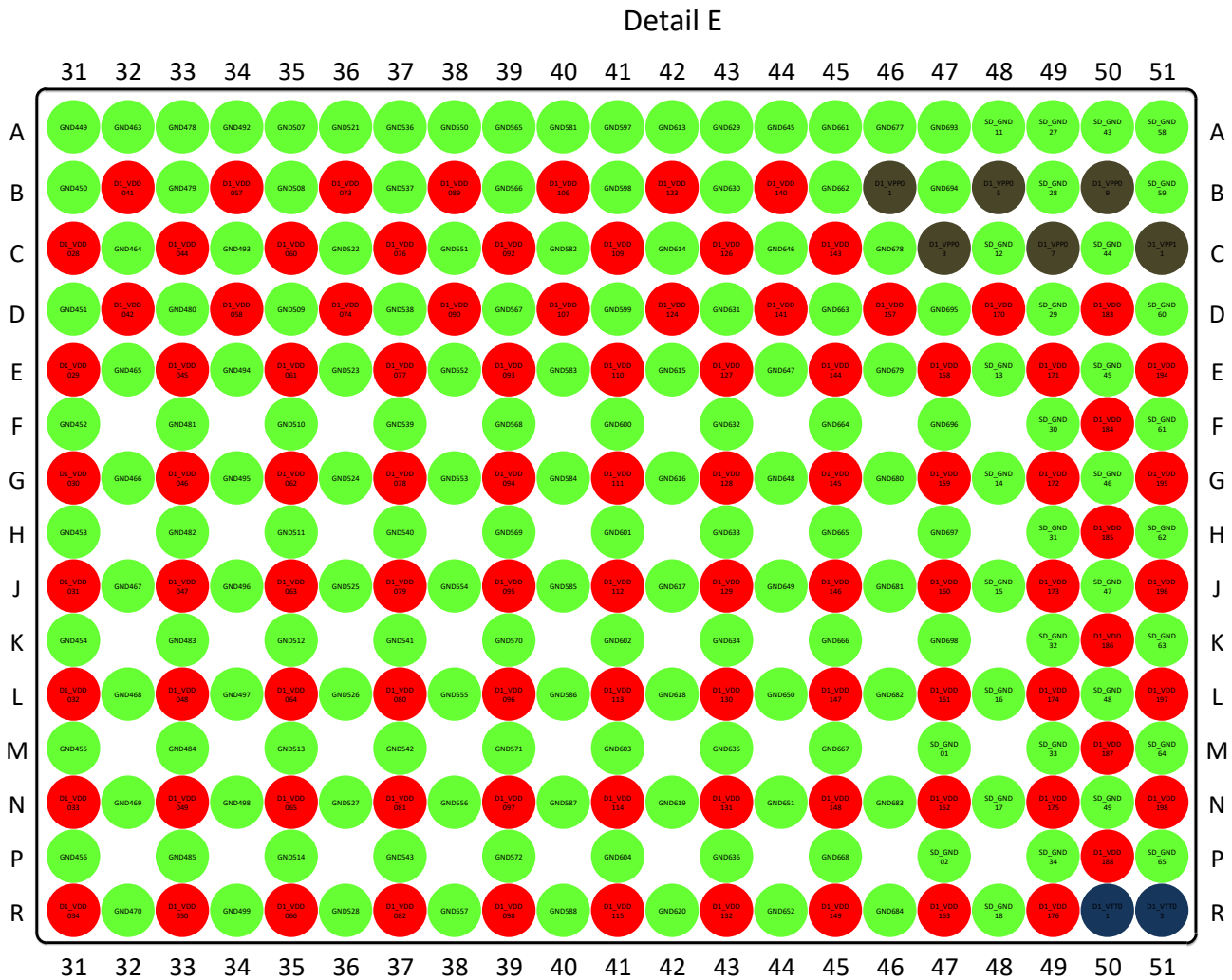
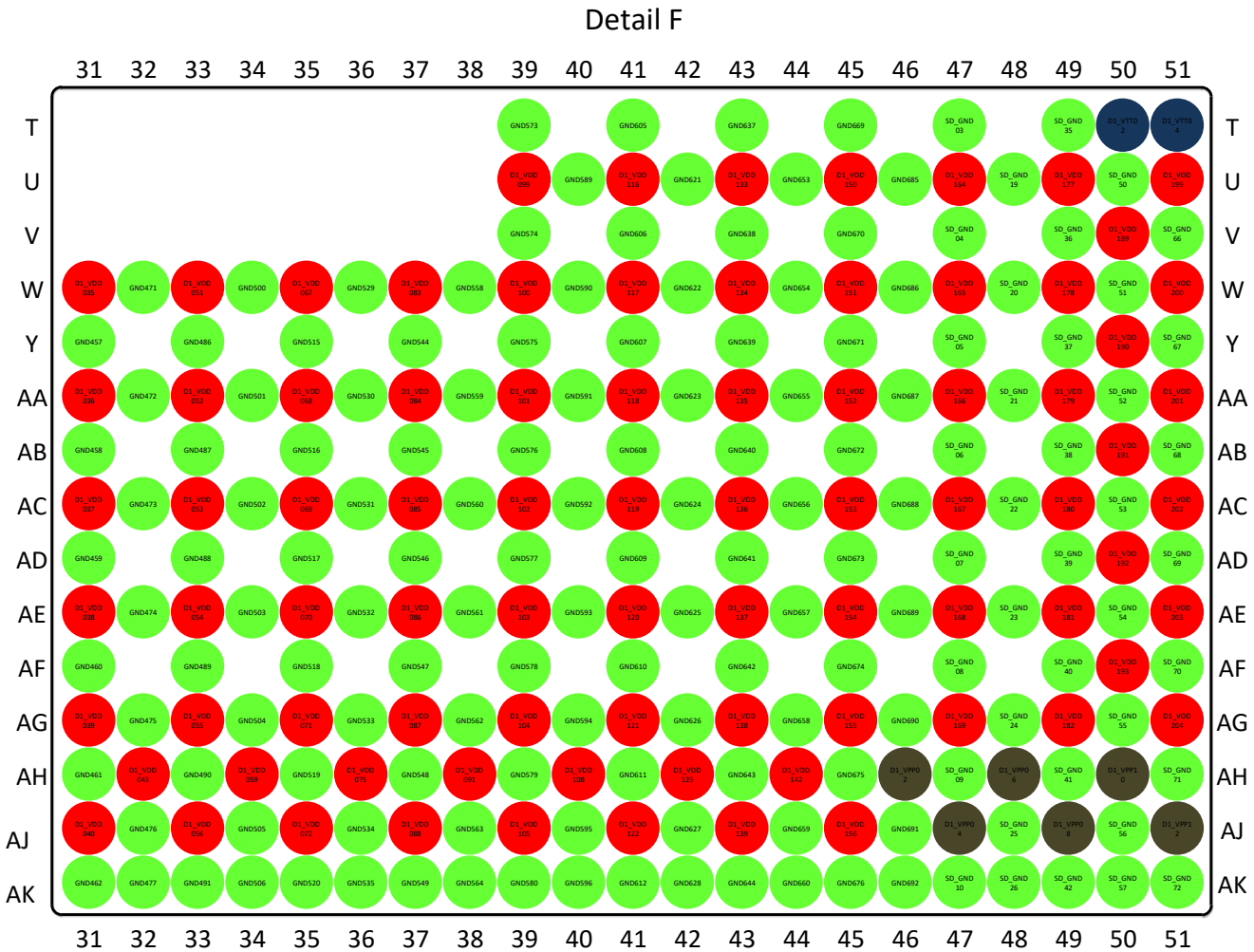


Figure 9. Detail F



2.2 Pinout list

This table provides the pinout listing for the QLS1046A by bus. Primary functions are **bolded** in the table.

Table 1. Pinout list by bus

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
DDR SDRAM Memory Interface 1					
MRST_N	DDR SDRAM Memory Interface 1	M28	I	G1VDD	–
VREFCA	DDR4 reference voltage	G21	–	G1VDD/2	–
Integrated Flash Controller					
IFC_A16/QSPI_A_CS0	IFC Address	E8	O	OVDD	1, 5
IFC_A17/QSPI_A_CS1	IFC Address	D8	O	OVDD	1, 5
IFC_A18/QSPI_A_SCK	IFC Address	D9	O	OVDD	1, 5
IFC_A19/QSPI_B_CS0	IFC Address	E10	O	OVDD	1, 5
IFC_A20/QSPI_B_CS1	IFC Address	D10	O	OVDD	1, 5
IFC_A21/QSPI_B_SCK/ cfg_dram_type	IFC Address	D11	O	OVDD	1, 15
IFC_A22/QSPI_A_DATA0/ IFC_WP1_B	IFC Address	E11	O	OVDD	1
IFC_A23/QSPI_A_DATA1/ IFC_WP2_B	IFC Address	D12	O	OVDD	1
IFC_A24/QSPI_A_DATA2/ IFC_WP3_B	IFC Address	E13	O	OVDD	1
IFC_A25/GPIO2_25/ QSPI_A_DATA3/FTM5_CH0/ IFC_CS4_B/IFC_RB2_B	IFC Address	D13	O	OVDD	1
IFC_A26/GPIO2_26/ FTM5_CH1/IFC_CS5_B/ IFC_RB3_B	IFC Address	E14	O	OVDD	1
IFC_A27/GPIO2_27/ FTM5_EXTCLK/IFC_CS6_B	IFC Address	D14	O	OVDD	1
IFC_AD00/cfg_gpinput0	IFC Address / Data	C8	IO	OVDD	4
IFC_AD01/cfg_gpinput1	IFC Address / Data	B8	IO	OVDD	4
IFC_AD02/cfg_gpinput2	IFC Address / Data	C9	IO	OVDD	4
IFC_AD03/cfg_gpinput3	IFC Address / Data	B9	IO	OVDD	4
IFC_AD04/cfg_gpinput4	IFC Address / Data	B10	IO	OVDD	4
IFC_AD05/cfg_gpinput5	IFC Address / Data	C11	IO	OVDD	4
IFC_AD06/cfg_gpinput6	IFC Address / Data	B11	IO	OVDD	4
IFC_AD07/cfg_gpinput7	IFC Address / Data	C12	IO	OVDD	4
IFC_AD08/cfg_rcw_src0	IFC Address / Data	B12	IO	OVDD	4
IFC_AD09/cfg_rcw_src1	IFC Address / Data	B13	IO	OVDD	4
IFC_AD10/cfg_rcw_src2	IFC Address / Data	C14	IO	OVDD	4
IFC_AD11/cfg_rcw_src3	IFC Address / Data	B14	IO	OVDD	4
IFC_AD12/cfg_rcw_src4	IFC Address / Data	C15	IO	OVDD	4

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Signal	Signal description	Package pin number	Pin type	Power supply	Notes
IFC_AD13/cfg_rcw_src5	IFC Address / Data	B15	IO	OVDD	4
IFC_AD14/cfg_rcw_src6	IFC Address / Data	B16	IO	OVDD	4
IFC_AD15/cfg_rcw_src7	IFC Address / Data	B17	IO	OVDD	4
IFC_AVD	IFC Address Valid	B18	O	OVDD	1, 5
IFC_BCTL	IFC Buffer control	F15	O	OVDD	–
IFC_CLE/cfg_rcw_src8	IFC Command Latch Enable / Write Enable	D19	O	OVDD	1, 4
IFC_CLK0	IFC Clock	B20	O	OVDD	–
IFC_CLK1	IFC Clock	C20	O	OVDD	–
IFC_CS0_B	IFC Chip Select	D17	O	OVDD	1, 6
IFC_CS1_B/GPIO2_10/ FTM7_CH0	IFC Chip Select	B19	O	OVDD	1, 6
IFC_CS2_B/GPIO2_11/ FTM7_CH1	IFC Chip Select	E20	O	OVDD	1, 6
IFC_CS3_B/GPIO2_12/ QSPI_B_DATA3/ FTM7_EXTCLK	IFC Chip Select	D20	O	OVDD	1, 6
IFC_CS4_B/**IFC_A25**/ GPIO2_25/QSPI_A_DATA3/ FTM5_CH0/IFC_RB2_B	IFC Chip Select	D13	O	OVDD	1
IFC_CS5_B/**IFC_A26**/ GPIO2_26/FTM5_CH1/ IFC_RB3_B	IFC Chip Select	E14	O	OVDD	1
IFC_CS6_B/**IFC_A27**/ GPIO2_27/FTM5_EXTCLK	IFC Chip Select	D14	O	OVDD	1
IFC_NDDDR_CLK	IFC NAND DDR Clock	F16	O	OVDD	–
IFC_NDDQS	IFC DQS Strobe	C17	IO	OVDD	–
IFC_OE_B/cfg_eng_use1	IFC Output Enable	D18	O	OVDD	1, 4
IFC_PAR0/GPIO2_13/ **QSPI_B_DATA0**/FTM6_CH0	IFC Address & Data Parity	C18	IO	OVDD	–
IFC_PAR1/GPIO2_14/ QSPI_B_DATA1/FTM6_CH1	IFC Address & Data Parity	E17	IO	OVDD	–
IFC_PERR_B/GPIO2_15/ QSPI_B_DATA2/ FTM6_EXTCLK	IFC Parity Error	F17	I	OVDD	1
IFC_RB0_B	IFC Ready / Busy CS0	D16	I	OVDD	6
IFC_RB1_B	IFC Ready / Busy CS1	E16	I	OVDD	6
IFC_RB2_B/**IFC_A25**/ GPIO2_25/QSPI_A_DATA3/ FTM5_CH0/IFC_CS4_B	IFC Ready/Busy CS 2	D13	I	OVDD	1
IFC_RB3_B/**IFC_A26**/ GPIO2_26/FTM5_CH1/ IFC_CS5_B	IFC Ready/Busy CS 3	E14	I	OVDD	1
IFC_TE/cfg_ifc_te	IFC External Transceiver Enable	F14	O	OVDD	1, 4
IFC_WE0_B/cfg_eng_use0	IFC Write Enable	D15	O	OVDD	1, 4, 26
IFC_WP0_B/cfg_eng_use2	IFC Write Protect	E19	O	OVDD	1, 4
IFC_WP1_B/**IFC_A22**/ QSPI_A_DATA0	IFC Write Protect	E11	O	OVDD	1
IFC_WP2_B/**IFC_A23**/ QSPI_A_DATA1	IFC Write Protect	D12	O	OVDD	1

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Signal	Signal description	Package pin number	Pin type	Power supply	Notes
IFC_WP3_B/**IFC_A24**/ QSPI_A_DATA2	IFC Write Protect	E13	O	OVDD	1
DUART					
UART1_CTS_B/GPIO1_21/ UART3_SIN/FTM4_CH4/ LPUART2_SIN	Clear To Send	K1	I	DVDD	1
UART1_RTS_B/GPIO1_19/ UART3_SOUT/ LPUART2_SOUT/FTM4_CH2	Ready to Send	K2	O	DVDD	1
UART1_SIN/GPIO1_17	Receive Data	J2	I	DVDD	1
UART1_SOUT/GPIO1_15	Transmit Data	J1	O	DVDD	1
UART2_CTS_B/GPIO1_22/ UART4_SIN/FTM4_CH5/ LPUART1_CTS_B/ LPUART4_SIN	Clear To Send	N2	I	DVDD	1
UART2_RTS_B/GPIO1_20/ UART4_SOUT/ LPUART4_SOUT/FTM4_CH3/ LPUART1_RTS_B	Ready to Send	M1	O	DVDD	1
UART2_SIN/GPIO1_18/ FTM4_CH1/LPUART1_SIN	Receive Data	L1	I	DVDD	1
UART2_SOUT/GPIO1_16/ LPUART1_SOUT/FTM4_CH0	Transmit Data	M2	O	DVDD	1
UART3_SIN/**UART1_CTS_B**/ GPIO1_21/FTM4_CH4/ LPUART2_SIN	Receive Data	K1	I	DVDD	1
UART3_SOUT/ **UART1_RTS_B**/GPIO1_19/ LPUART2_SOUT/FTM4_CH2	Transmit Data	K2	O	DVDD	1
UART4_SIN/**UART2_CTS_B**/ GPIO1_22/FTM4_CH5/ LPUART1_CTS_B/ LPUART4_SIN	Receive Data	N2	I	DVDD	1
UART4_SOUT/ **UART2_RTS_B**/GPIO1_20/ LPUART4_SOUT/FTM4_CH3/ LPUART1_RTS_B	Transmit Data	M1	O	DVDD	1
I2C					
IIC1_SCL	Serial Clock (supports PBL)	P1	IO	DVDD	7, 8
IIC1_SDA	Serial Data (supports PBL)	N1	IO	DVDD	7, 8
IIC2_SCL/GPIO4_2/ SDHC_CD_B/FTM3_QD_PHA	Serial Clock	L3	IO	DVDD	7, 8
IIC2_SDA/GPIO4_3/ SDHC_WP/FTM3_QD_PHB	Serial Data	M3	IO	DVDD	7, 8
IIC3_SCL/GPIO4_10/EVT5_B/ USB2_DRVVBUS/FTM8_CH0	Serial Clock	M4	IO	DVDD	7, 8
IIC3_SDA/GPIO4_11/EVT6_B/ USB2_PWRFAULT/ FTM8_CH1	Serial Data	N4	IO	DVDD	7, 8
IIC4_SCL/GPIO4_12/EVT7_B/ USB3_DRVVBUS/ FTM3_FAULT	Serial Clock	N3	IO	DVDD	7, 8
IIC4_SDA/GPIO4_13/EVT8_B/ USB3_PWRFAULT/ FTM3_EXTCLK	Serial Data	P3	IO	DVDD	7, 8
SPI Interface					
SPI_PCS0/GPIO2_00/ SDHC_DAT4/SDHC_VS	SPI Chip Select	V1	O	OVDD	1
SPI_PCS1/GPIO2_01/ SDHC_DAT5/ SDHC_CMD_DIR	SPI Chip Select	T3	O	OVDD	1
SPI_PCS2/GPIO2_02/ SDHC_DAT6/ SDHC_DAT0_DIR	SPI Chip Select	U3	O	OVDD	1
SPI_PCS3/GPIO2_03/ SDHC_DAT7/ SDHC_DAT123_DIR	SPI Chip Select	W1	O	OVDD	1

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Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SPI_SCK	SPI Clock	V2	O	OVDD	1
SPI_SIN/ SDHC_CLK_SYNC_IN	Master In Slave Out	V3	I	OVDD	1
SPI_SOUT/ SDHC_CLK_SYNC_OUT	Master Out Slave In	W3	IO	OVDD	–
eSDHC					
SDHC_CD_B/**IIC2_SCL**/ GPIO4_2/FTM3_QD_PHA	Command	L3	I	DVDD	1
SDHC_CLK/GPIO2_09/ LPUART3_CTS_B/ LPUART6_SIN/ FTM4_QD_PHB	Host to Card Clock	R3	O	EVDD	1
SDHC_CLK_SYNC_IN/**SPI_SIN**	IN	V3	I	OVDD	1
SDHC_CLK_SYNC_OUT/**SPI_SOUT**	OUT	W3	O	OVDD	1
SDHC_CMD/GPIO2_04/ LPUART3_SOUT/FTM4_CH6	Command/Response	R2	IO	EVDD	–
SDHC_CMD_DIR/**SPI_PCS1**/ GPIO2_01/SDHC_DAT5	DIR	T3	O	OVDD	1
SDHC_DAT0/GPIO2_05/ FTM4_CH7/LPUART3_SIN	Data	R1	IO	EVDD	–
SDHC_DAT0_DIR/**SPI_PCS2**/ GPIO2_02/SDHC_DAT6	DIR	U3	O	OVDD	1
SDHC_DAT1/GPIO2_06/ LPUART5_SOUT/	Data	T2	IO	EVDD	–
FTM4_FAULT/ LPUART2_RTS_B					
SDHC_DAT123_DIR/ **SPI_PCS3/GPIO2**_03/ SDHC_DAT7	DIR	W1	O	OVDD	1
SDHC_DAT2/GPIO2_07/ LPUART2_CTS_B/ LPUART5_SIN/ FTM4_EXTCLK	Data	T1	IO	EVDD	–
SDHC_DAT3/GPIO2_08/ LPUART6_SOUT/ FTM4_QD_PHA/ LPUART3_RTS_B	Data	U1	IO	EVDD	–
SDHC_DAT4/**SPI_PCS0**/ GPIO2_00/SDHC_VS	Data	V1	IO	OVDD	–
SDHC_DAT5/**SPI_PCS1**/ GPIO2_01/SDHC_CMD_DIR	Data	T3	IO	OVDD	–
SDHC_DAT6/**SPI_PCS2**/ GPIO2_02/SDHC_DAT0_DIR	Data	U3	IO	OVDD	–
SDHC_DAT7/**SPI_PCS3**/ GPIO2_03/ SDHC_DAT123_DIR	Data	W1	IO	OVDD	–
SDHC_VS/**SPI_PCS0**/ GPIO2_00/SDHC_DAT4	VS	V1	O	OVDD	1
SDHC_WP/**IIC2_SDA**/ GPIO4_3/FTM3_QD_PHB	Write Protect	M3	I	DVDD	1
Programmable Interrupt Controller					
EVT9_B	Event 9	H7	IO	OVDD	1, 6, 7
IRQ00	External Interrupt	G11	I	OVDD	1
IRQ01	External Interrupt	G15	I	OVDD	1
IRQ02	External Interrupt	J7	I	OVDD	1
IRQ03/GPIO1_23/FTM3_CH7	External Interrupt	K3	I	DVDD	1
IRQ04/GPIO1_24/FTM3_CH0	External Interrupt	K4	I	DVDD	1
IRQ05/GPIO1_25/FTM3_CH1	External Interrupt	K5	I	DVDD	1

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Signal	Signal description	Package pin number	Pin type	Power supply	Notes
IRQ06/GPIO1_26/FTM3_CH2	External Interrupt	L5	I	DVDD	1
IRQ07/GPIO1_27/FTM3_CH3	External Interrupt	M5	I	DVDD	1
IRQ08/GPIO1_28/FTM3_CH4	External Interrupt	N5	I	DVDD	1
IRQ09/GPIO1_29/FTM3_CH5	External Interrupt	P5	I	DVDD	1
IRQ10/GPIO1_30/FTM3_CH6	External Interrupt	R4	I	DVDD	1
IRQ11/GPIO1_31	External Interrupt	Y3	I	LVDD	1
Battery Backed Trust					
TA_BB_TMP_DETECT_B	Battery Backed Tamper Detect	J12	I	TA_BB_VDD	–
Trust					
TA_TMP_DETECT_B	Tamper Detect	J20	I	OVDD	1
System Control					
HRESET_B	Hard Reset	G8	IO	OVDD	7, 28
PORESET_B	Power On Reset	G9	I	OVDD	–
RESET_REQ_B	Reset Request	G10	O	OVDD	1, 5
Power Management					
ASLEEP/GPIO1_13	Asleep	F9	O	OVDD	1
SYSCLK					
SYSCLK	System Clock	H14	I	OVDD	22
DDR Clocking					
DDRCLK	DDR Controller Clock	K20	I	OVDD	22
RTC					
RTC/GPIO1_14	Real Time Clock	G17	I	OVDD	1
Debug					
CKSTP_OUT_B	RSVD	H15	-	OVDD	6, 7
CLK_OUT	Clock Out	H16	O	OVDD	–
EVT0_B	Event 0	F10	IO	OVDD	9
EVT1_B	Event 1	F13	IO	OVDD	–
EVT2_B	Event 2	F8	IO	OVDD	–
EVT3_B	Event 3	F12	IO	OVDD	–
EVT4_B	Event 4	F11	IO	OVDD	–
EVT5_B/**IIC3_SCL**/GPIO4_10/ USB2_DRVVBUS/FTM8_CH0	Event 5	M4	IO	DVDD	–
EVT6_B/**IIC3_SDA**/GPIO4_11/ USB2_PWRFAULT/ FTM8_CH1	Event 6	N4	IO	DVDD	–
EVT7_B/**IIC4_SCL**/GPIO4_12/ USB3_DRVVBUS/ FTM3_FAULT	Event 7	N3	IO	DVDD	–
EVT8_B/**IIC4_SDA**/GPIO4_13/ USB3_PWRFAULT/ FTM3_EXTCLK	Event 8	P3	IO	DVDD	–

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Signal	Signal description	Package pin number	Pin type	Power supply	Notes
DFT					
JTAG_BSR_VSEL	An IEEE 1149.1 JTAG Compliance Enable pin. 0: normal operation. 1: To be compliant to the 1149.1 specification for boundary scan functions. The JTAG compliant state is documented in the BSDL.	K19	I	OVDD	24, 25
SCAN_MODE_B	Reserved	J19	I	OVDD	10, 25
TBSCAN_EN_B	An IEEE 1149.1 JTAG Compliance Enable pin. 0: To be compliant to the 1149.1 specification for boundary scan functions. The JTAG compliant state is documented in the BSDL. 1: JTAG connects to DAP controller for the Arm core debug.	G19	I	OVDD	20, 25
TEST_SEL_B	Reserved	G20	I	OVDD	19, 25
JTAG					
TCK	Test Clock	F18	I	OVDD	–
TDI	Test Data In	H17	I	OVDD	9
TDO	Test Data Out	F20	O	OVDD	2
TMS	Test Mode Select	H18	I	OVDD	9
TRST_B	Test Reset	F19	I	OVDD	9
Analog Signals					
FA_ANALOG_G_V	Reserved	AH21	IO		15
FA_ANALOG_PIN	Reserved	AE21	IO		15
TD1_ANODE	Thermal diode anode	K13	IO		17
TD1_CATHODE	Thermal diode cathode	J13	IO		17
TH_TPA	Thermal Test Point Analog	J8	-	-	12
SerDes 1					
SD1_IMP_CAL_RX	SerDes Receive Impedence Calibration	AA11	I	SVDD	11
SD1_IMP_CAL_TX	SerDes Transmit Impedance Calibration	AB6	I	XVDD	16
SD1_PLL1_TPA	SerDes PLL 1 Test Point Analog	AG12	O	AVDD_SD1_PLL1	12
SD1_PLL1_TPD	SerDes Test Point Digital	AG13	O	XVDD	12
SD1_PLL2_TPA	SerDes PLL 2 Test Point Analog	AG5	O	AVDD_SD1_PLL2	12
SD1_PLL2_TPD	SerDes Test Point Digital	AC5	O	XVDD	12
SD1_REF_CLK1_N	SerDes PLL 1 Reference Clock Complement	AJ13	I	SVDD	–
SD1_REF_CLK1_P	SerDes PLL 1 Reference Clock	AH13	I	SVDD	–
SD1_REF_CLK2_N	SerDes PLL 2 Reference Clock Complement	AC8	I	SVDD	–
SD1_REF_CLK2_P	SerDes PLL 2 Reference Clock	AB8	I	SVDD	–

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Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD1_RX0_N	SerDes Receive Data (negative)	AJ6	I	SVDD	–
SD1_RX0_P	SerDes Receive Data (positive)	AH6	I	SVDD	–
SD1_RX1_N	SerDes Receive Data (negative)	AJ8	I	SVDD	–
SD1_RX1_P	SerDes Receive Data (positive)	AH8	I	SVDD	–
SD1_RX2_N	SerDes Receive Data (negative)	AJ10	I	SVDD	–
SD1_RX2_P	SerDes Receive Data (positive)	AH10	I	SVDD	–
SD1_RX3_N	SerDes Receive Data (negative)	AJ11	I	SVDD	–
SD1_RX3_P	SerDes Receive Data (positive)	AH11	I	SVDD	–
SD1_TX0_N	SerDes Transmit Data (negative)	AF6	O	XVDD	–
SD1_TX0_P	SerDes Transmit Data (positive)	AE6	O	XVDD	–
SD1_TX1_N	SerDes Transmit Data (negative)	AF8	O	XVDD	–
SD1_TX1_P	SerDes Transmit Data (positive)	AE8	O	XVDD	–
SD1_TX2_N	SerDes Transmit Data (negative)	AF10	O	XVDD	–
SD1_TX2_P	SerDes Transmit Data (positive)	AE10	O	XVDD	–
SD1_TX3_N	SerDes Transmit Data (negative)	AF11	O	XVDD	–
SD1_TX3_P	SerDes Transmit Data (positive)	AE11	O	XVDD	–
SerDes 2					
SD2_IMP_CAL_RX	SerDes Receive Impedence Calibration	AA12	I	SVDD	11
SD2_IMP_CAL_TX	SerDes Transmit Impedance Calibration	AA20	I	XVDD	16
SD2_PLL1_TPA	SerDes PLL 1 Test Point Analog	AG14	O	AVDD_SD2_PLL1	12
SD2_PLL1_TPD	SerDes Test Point Digital	AD13	O	XVDD	12
SD2_PLL2_TPA	SerDes PLL 2 Test Point Analog	AG20	O	AVDD_SD2_PLL2	12
SD2_PLL2_TPD	SerDes Test Point Digital	AB20	O	XVDD	12
SD2_REF_CLK1_N	SerDes PLL 1 Reference Clock Complement	AF13	I	SVDD	–
SD2_REF_CLK1_P	SerDes PLL 1 Reference Clock	AE13	I	SVDD	–
SD2_REF_CLK2_N	SerDes PLL 2 Reference Clock Complement	AC19	I	SVDD	–
SD2_REF_CLK2_P	SerDes PLL 2 Reference Clock	AC18	I	SVDD	–
SD2_RX0_N	SerDes Receive Data (negative)	AJ15	I	SVDD	–
SD2_RX0_P	SerDes Receive Data (positive)	AH15	I	SVDD	–
SD2_RX1_N	SerDes Receive Data (negative)	AJ16	I	SVDD	–
SD2_RX1_P	SerDes Receive Data (positive)	AH16	I	SVDD	–
SD2_RX2_N	SerDes Receive Data (negative)	AJ18	I	SVDD	–
SD2_RX2_P	SerDes Receive Data (positive)	AH18	I	SVDD	–

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SD2_RX3_N	SerDes Receive Data (negative)	AJ19	I	SVDD	–
SD2_RX3_P	SerDes Receive Data (positive)	AH19	I	SVDD	–
SD2_TX0_N	SerDes Transmit Data (negative)	AF15	O	XVDD	–
SD2_TX0_P	SerDes Transmit Data (positive)	AE15	O	XVDD	–
SD2_TX1_N	SerDes Transmit Data (negative)	AF16	O	XVDD	–
SD2_TX1_P	SerDes Transmit Data (positive)	AE16	O	XVDD	–
SD2_TX2_N	SerDes Transmit Data (negative)	AF18	O	XVDD	–
SD2_TX2_P	SerDes Transmit Data (positive)	AE18	O	XVDD	–
SD2_TX3_N	SerDes Transmit Data (negative)	AF19	O	XVDD	–
SD2_TX3_P	SerDes Transmit Data (positive)	AE19	O	XVDD	–
USB3 PHY #1					
USB1_D_M	USB PHY HS Data (-)	F6	IO	-	–
USB1_D_P	USB PHY HS Data (+)	G6	IO	-	–
USB1_ID	USB PHY ID Detect	G5	I	-	–
USB1_RESREF	USB PHY Impedance Calibration	H3	IO	-	18
USB1_RX_M	USB PHY SS Receive Data (-)	F4	I	-	–
USB1_RX_P	USB PHY SS Receive Data (+)	F3	I	-	–
USB1_TX_M	USB PHY SS Transmit Data (-)	G2	O	-	–
USB1_TX_P	USB PHY SS Transmit Data (+)	G1	O	-	–
USB1_VBUS	USB PHY VBUS	F7	I	-	–
USB3 PHY #2					
USB2_D_M	USB PHY HS Data (-)	D6	IO	-	–
USB2_D_P	USB PHY HS Data (+)	E6	IO	-	–
USB2_ID	USB PHY ID Detect	E5	I	-	–
USB2_RESREF	USB PHY Impedance Calibration	H4	IO	-	18
USB2_RX_M	USB PHY SS Receive Data (-)	D4	I	-	–
USB2_RX_P	USB PHY SS Receive Data (+)	D3	I	-	–
USB2_TX_M	USB PHY SS Transmit Data (-)	E2	O	-	–
USB2_TX_P	USB PHY SS Transmit Data (+)	E1	O	-	–
USB2_VBUS	USB PHY VBUS	D7	I	-	–
USB PHY #3					
USB3_D_M	USB PHY HS Data (-)	B6	IO	-	–
USB3_D_P	USB PHY HS Data (+)	C6	IO	-	–
USB3_ID	USB PHY ID Detect	C5	I	-	–
USB3_RESREF	USB PHY Impedance Calibration	H5	IO	-	18

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USB3_RX_M	USB PHY SS Receive Data (-)	B4	I	-	–
USB3_RX_P	USB PHY SS Receive Data (+)	B3	I	-	–
USB3_TX_M	USB PHY SS Transmit Data (-)	C2	O	-	–
USB3_TX_P	USB PHY SS Transmit Data (+)	C1	O	-	–
USB3_VBUS	USB PHY VBUS	B7	I	-	–
Ethernet Management Interface 1					
EMI1_MDC/GPIO3_00	Management Data Clock	AH2	O	LVDD	1
EMI1_MDIO/GPIO3_01	Management Data In/Out	AG2	IO	LVDD	–
Ethernet Management Interface 2					
EMI2_MDC/GPIO4_00	Management Data Clock	AJ4	O	TVDD	1
EMI2_MDIO/GPIO4_01	Management Data In/Out	AJ3	IO	TVDD	–
Ethernet Controller 1					
EC1_GTX_CLK/GPIO3_07/ FTM1_EXTCLK	Transmit Clock Out	Y4	O	LVDD	1
EC1_GTX_CLK125/GPIO3_08	Reference Clock	AD3	I	LVDD	1
EC1_RXD0/GPIO3_12/ FTM1_CH0	Receive Data	AB2	I	LVDD	1
EC1_RXD1/GPIO3_11/ FTM1_CH1	Receive Data	AB1	I	LVDD	1
EC1_RXD2/GPIO3_10/ FTM1_CH6	Receive Data	AA1	I	LVDD	1
EC1_RXD3/GPIO3_09/ FTM1_CH4	Receive Data	Y2	I	LVDD	1
EC1_RX_CLK/GPIO3_13/ FTM1_QD_PHA	Receive Clock	Y1	I	LVDD	1
EC1_RX_DV/GPIO3_14/ FTM1_QD_PHB	Receive Data Valid	AC1	I	LVDD	1
EC1_TXD0/GPIO3_05/ FTM1_CH2	Transmit Data	AC3	O	LVDD	1
EC1_TXD1/GPIO3_04/ FTM1_CH3	Transmit Data	AB3	O	LVDD	1
EC1_TXD2/GPIO3_03/ FTM1_CH7	Transmit Data	AA4	O	LVDD	1
EC1_TXD3/GPIO3_02/ FTM1_CH5	Transmit Data	AA3	O	LVDD	1
EC1_TX_EN/GPIO3_06/ FTM1_FAULT	Transmit Enable	AC4	O	LVDD	1, 14
Ethernet Controller 2					
EC2_GTX_CLK/GPIO3_20/ FTM2_EXTCLK	Transmit Clock Out	AD4	O	LVDD	1
EC2_GTX_CLK125/GPIO3_21	Reference Clock	AH4	I	LVDD	1
EC2_RXD0/GPIO3_25/ TSEC_1588_TRIG_IN2/ FTM2_CH0	Receive Data	AF2	I	LVDD	1
EC2_RXD1/GPIO3_24/ TSEC_1588_PULSE_OUT1/ FTM2_CH1	Receive Data	AF1	I	LVDD	1
EC2_RXD2/GPIO3_23/ FTM2_CH6	Receive Data	AE1	I	LVDD	1
EC2_RXD3/GPIO3_22/ FTM2_CH4	Receive Data	AD2	I	LVDD	1
EC2_RX_CLK/GPIO3_26/ TSEC_1588_CLK_IN/ FTM2_QD_PHA	Receive Clock	AD1	I	LVDD	1

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EC2_RX_DV/GPIO3_27/ TSEC_1588_TRIG_IN1/ FTM2_QD_PHB	Receive Data Valid	AG1	I	LVDD	1
EC2_TXD0/GPIO3_18/ TSEC_1588_PULSE_OUT2/ FTM2_CH2	Transmit Data	AG3	O	LVDD	1
EC2_TXD1/GPIO3_17/ TSEC_1588_CLK_OUT/ FTM2_CH3	Transmit Data	AF4	O	LVDD	1
EC2_TXD2/GPIO3_16/ TSEC_1588_ALARM_OUT1/ FTM2_CH7	Transmit Data	AF3	O	LVDD	1
EC2_TXD3/GPIO3_15/ TSEC_1588_ALARM_OUT2/ FTM2_CH5	Transmit Data	AE3	O	LVDD	1
EC2_TX_EN/GPIO3_19/ FTM2_FAULT	Transmit Enable	AH3	O	LVDD	1, 14
USB					
USB2_DRVVBUS/**IIC3_SCL**/ GPIO4_10/EVT5_B/ FTM8_CH0	DRV VBus	M4	O	DVDD	1
USB2_PWRFAULT/**IIC3_SDA**/ GPIO4_11/EVT6_B/ FTM8_CH1	PWR Fault	N4	I	DVDD	1
USB3_DRVVBUS/**IIC4_SCL**/ GPIO4_12/EVT7_B/ FTM3_FAULT	DRV Bus	N3	O	DVDD	1
USB3_PWRFAULT/**IIC4_SDA**/ GPIO4_13/EVT8_B/ FTM3_EXTCLK	PWR Fault	P3	I	DVDD	1
USB_DRVVBUS/GPIO4_29	USB_DRVVBUS	J6	O	DVDD	1
USB_PWRFAULT/GPIO4_30	USB_PWRFAULT	H6	I	DVDD	1
DSYSCLK					
DIFF_SYSCLK	Single Source System Clock Differential (positive)	AB13	I	OVDD	21
DIFF_SYSCLK_B	Single Source System Clock Differential (negative)	AC13	I	OVDD	21
Power-On-Reset Configuration					
cfg_dram_type/**IFC_A21**/ QSPI_B_SCK	Power-on-Reset Configuration	D11	I	OVDD	1, 15
cfg_eng_use0/**IFC_WE0_B**	Power-on-Reset Configuration	D15	I	OVDD	1, 4, 26
cfg_eng_use1/**IFC_OE_B**	Power-on-Reset Configuration	D18	I	OVDD	1, 4
cfg_eng_use2/**IFC_WP0_B**	Power-on-Reset Configuration	E19	I	OVDD	1, 4
cfg_gpinput0/**IFC_AD00**	Power-on-Reset Configuration	C8	I	OVDD	1, 4
cfg_gpinput1/**IFC_AD01**	Power-on-Reset Configuration	B8	I	OVDD	1, 4
cfg_gpinput2/**IFC_AD02**	Power-on-Reset Configuration	C9	I	OVDD	1, 4
cfg_gpinput3/**IFC_AD03**	Power-on-Reset Configuration	B9	I	OVDD	1, 4
cfg_gpinput4/**IFC_AD04**	Power-on-Reset Configuration	B10	I	OVDD	1, 4
cfg_gpinput5/**IFC_AD05**	Power-on-Reset Configuration	C11	I	OVDD	1, 4
cfg_gpinput6/**IFC_AD06**	Power-on-Reset Configuration	B11	I	OVDD	1, 4
cfg_gpinput7/**IFC_AD07**	Power-on-Reset Configuration	C12	I	OVDD	1, 4
cfg_ifc_te/**IFC_TE**	Power-on-Reset Configuration	F14	I	OVDD	1, 4
cfg_rcw_src0/**IFC_AD08**	Power-on-Reset Configuration	B12	I	OVDD	1, 4

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cfg_rcw_src1/**IFC_AD09**	Power-on-Reset Configuration	B13	I	OVDD	1, 4
cfg_rcw_src2/**IFC_AD10**	Power-on-Reset Configuration	C14	I	OVDD	1, 4
cfg_rcw_src3/**IFC_AD11**	Power-on-Reset Configuration	B14	I	OVDD	1, 4
cfg_rcw_src4/**IFC_AD12**	Power-on-Reset Configuration	C15	I	OVDD	1, 4
cfg_rcw_src5/**IFC_AD13**	Power-on-Reset Configuration	B15	I	OVDD	1, 4
cfg_rcw_src6/**IFC_AD14**	Power-on-Reset Configuration	B16	I	OVDD	1, 4
cfg_rcw_src7/**IFC_AD15**	Power-on-Reset Configuration	B17	I	OVDD	1, 4
cfg_rcw_src8/**IFC_CLE**	Power-on-Reset Configuration	D19	I	OVDD	1, 4
QSPI					
QSPI_A_CS0/**IFC_A16**	Chip Select	E8	O	OVDD	1, 5
QSPI_A_CS1/**IFC_A17**	CS1	D8	O	OVDD	1, 5
QSPI_A_DATA0/**IFC_A22**/ IFC_WP1_B	DATA0	E11	IO	OVDD	–
QSPI_A_DATA1/**IFC_A23**/ IFC_WP2_B	DATA1	D12	IO	OVDD	–
QSPI_A_DATA2/**IFC_A24**/ IFC_WP3_B	DATA2	E13	IO	OVDD	–
QSPI_A_DATA3/**IFC_A25**/ GPIO2_25/FTM5_CH0/ IFC_CS4_B/IFC_RB2_B	DATA3	D13	IO	OVDD	–
QSPI_A_SCK/**IFC_A18**	SCK	D9	O	OVDD	1, 5
QSPI_B_CS0/**IFC_A19**	Chip Select	E10	O	OVDD	1, 5
QSPI_B_CS1/**IFC_A20**	CS1	D10	O	OVDD	1, 5
QSPI_B_DATA0/**IFC_PAR0**/ GPIO2_13/FTM6_CH0	DATA0	C18	IO	OVDD	–
QSPI_B_DATA1/**IFC_PAR1**/ GPIO2_14/FTM6_CH1	DATA1	E17	IO	OVDD	–
QSPI_B_DATA2/ **IFC_PERR_B**/GPIO2_15/ FTM6_EXTCLK	DATA2	F17	IO	OVDD	–
QSPI_B_DATA3/**IFC_CS3_B**/ GPIO2_12/FTM7_EXTCLK	DATA3	D20	IO	OVDD	–
QSPI_B_SCK/**IFC_A21**/ cfg_dram_type	SCK	D11	O	OVDD	1, 15
General Purpose Input/Output					
GPIO1_13/ASLEEP	General Purpose Input/Output	F9	O	OVDD	1
GPIO1_14/RTC	General Purpose Input/Output	G17	IO	OVDD	–
GPIO1_15/**UART1_SOUT**	General Purpose Input/Output	J1	IO	DVDD	–
GPIO1_16/**UART2_SOUT**/ LPUART1_SOUT/FTM4_CH0	General Purpose Input/Output	M2	IO	DVDD	–
GPIO1_17/**UART1_SIN**	General Purpose Input/Output	J2	IO	DVDD	–
GPIO1_18/**UART2_SIN**/ FTM4_CH1/LPUART1_SIN	General Purpose Input/Output	L1	IO	DVDD	–
GPIO1_19/**UART1_RTS_B**/ UART3_SOUT/ LPUART2_SOUT/FTM4_CH2	General Purpose Input/Output	K2	IO	DVDD	–

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GPIO1_20/**UART2_RTS_B**/ UART4_SOUT/ LPUART4_SOUT/FTM4_CH3/ LPUART1_RTS_B	General Purpose Input/Output	M1	IO	DVDD	–
GPIO1_21/**UART1_CTS_B**/ UART3_SIN/FTM4_CH4/ LPUART2_SIN	General Purpose Input/Output	K1	IO	DVDD	–
GPIO1_22/**UART2_CTS_B**/ UART4_SIN/FTM4_CH5/ LPUART1_CTS_B/ LPUART4_SIN	General Purpose Input/Output	N2	IO	DVDD	–
GPIO1_23/**IRQ03**/FTM3_CH7	General Purpose Input/Output	K3	IO	DVDD	–
GPIO1_24/**IRQ04**/FTM3_CH0	General Purpose Input/Output	K4	IO	DVDD	–
GPIO1_25/**IRQ05**/FTM3_CH1	General Purpose Input/Output	K5	IO	DVDD	–
GPIO1_26/**IRQ06**/FTM3_CH2	General Purpose Input/Output	L5	IO	DVDD	–
GPIO1_27/**IRQ07**/FTM3_CH3	General Purpose Input/Output	M5	IO	DVDD	–
GPIO1_28/**IRQ08**/FTM3_CH4	General Purpose Input/Output	N5	IO	DVDD	–
GPIO1_29/**IRQ09**/FTM3_CH5	General Purpose Input/Output	P5	IO	DVDD	–
GPIO1_30/**IRQ10**/FTM3_CH6	General Purpose Input/Output	R4	IO	DVDD	–
GPIO1_31/**IRQ11**	General Purpose Input/Output	Y3	IO	LVDD	–
GPIO2_00/**SPI_PCS0**/ SDHC_DAT4/SDHC_VS	General Purpose Input/Output	V1	IO	OVDD	–
GPIO2_01/**SPI_PCS1**/ SDHC_DAT5/ SDHC_CMD_DIR	General Purpose Input/Output	T3	IO	OVDD	–
GPIO2_02/**SPI_PCS2**/ SDHC_DAT6/ SDHC_DAT0_DIR	General Purpose Input/Output	U3	IO	OVDD	–
GPIO2_03/**SPI_PCS3**/ SDHC_DAT7/ SDHC_DAT123_DIR	General Purpose Input/Output	W1	IO	OVDD	–
GPIO2_04/**SDHC_CMD**/ LPUART3_SOUT/FTM4_CH6	General Purpose Input/Output	R2	IO	EVDD	–
GPIO2_05/**SDHC_DAT0**/ FTM4_CH7/LPUART3_SIN	General Purpose Input/Output	R1	IO	EVDD	–
GPIO2_06/**SDHC_DAT1**/ LPUART5_SOUT/ FTM4_FAULT/ LPUART2_RTS_B	General Purpose Input/Output	T2	IO	EVDD	–
GPIO2_07/**SDHC_DAT2**/ LPUART2_CTS_B/ LPUART5_SIN/ FTM4_EXTCLK	General Purpose Input/Output	T1	IO	EVDD	–
GPIO2_08/**SDHC_DAT3**/ LPUART6_SOUT/ FTM4_QD_PHA/ LPUART3_RTS_B	General Purpose Input/Output	U1	IO	EVDD	–
GPIO2_09/**SDHC_CLK**/ LPUART3_CTS_B/ LPUART6_SIN/ FTM4_QD_PHB	General Purpose Input/Output	R3	IO	EVDD	–
GPIO2_10/**IFC_CS1_B**/ FTM7_CH0	General Purpose Input/Output	B19	IO	OVDD	–
GPIO2_11/**IFC_CS2**_B/ FTM7_CH1	General Purpose Input/Output	E20	IO	OVDD	–
GPIO2_12/**IFC_CS3_B**/ QSPI_B_DATA3/ FTM7_EXTCLK	General Purpose Input/Output	D20	IO	OVDD	–
GPIO2_13/**IFC_PAR0**/ QSPI_B_DATA0/FTM6_CH0	General Purpose Input/Output	C18	IO	OVDD	–
GPIO2_14/**IFC_PAR1**/ QSPI_B_DATA1/FTM6_CH1	General Purpose Input/Output	E17	IO	OVDD	–
GPIO2_15/**IFC_PERR_B**/ QSPI_B_DATA2/ FTM6_EXTCLK	General Purpose Input/Output	F17	IO	OVDD	–

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GPIO2_25/**IFC_A25**/ QSPI_A_DATA3/FTM5_CH0/ IFC_CS4_B/IFC_RB2_B	General Purpose Input/Output	D13	IO	OVDD	–
GPIO2_26/**IFC_A26**/ FTM5_CH1/IFC_CS5_B/ IFC_RB3_B	General Purpose Input/Output	E14	IO	OVDD	–
GPIO2_27/**IFC_A27**/ FTM5_EXTCLK/IFC_CS6_B	General Purpose Input/Output	D14	IO	OVDD	–
GPIO3_00/**EMI1_MDC**	General Purpose Input/Output	AH2	IO	LVDD	–
GPIO3_01/**EMI1_MDIO**	General Purpose Input/Output	AG2	IO	LVDD	–
GPIO3_02/**EC1_TXD3**/ FTM1_CH5	General Purpose Input/Output	AA3	IO	LVDD	–
GPIO3_03/**EC1_TXD2**/ FTM1_CH7	General Purpose Input/Output	AA4	IO	LVDD	–
GPIO3_04/**EC1_TXD1**/ FTM1_CH3	General Purpose Input/Output	AB3	IO	LVDD	–
GPIO3_05/**EC1_TXD0**/ FTM1_CH2	General Purpose Input/Output	AC3	IO	LVDD	–
GPIO3_06/**EC1_TX_EN**/ FTM1_FAULT	General Purpose Input/Output	AC4	IO	LVDD	–
GPIO3_07/**EC1_GTX_CLK**/ FTM1_EXTCLK	General Purpose Input/Output	Y4	IO	LVDD	–
GPIO3_08/**EC1_GTX_CLK125**	General Purpose Input/Output	AD3	IO	LVDD	–
GPIO3_09/**EC1_RXD3**/ FTM1_CH4	General Purpose Input/Output	Y2	IO	LVDD	–
GPIO3_10/**EC1_RXD2**/ FTM1_CH6	General Purpose Input/Output	AA1	IO	LVDD	–
GPIO3_11/**EC1_RXD1**/ FTM1_CH1	General Purpose Input/Output	AB1	IO	LVDD	–
GPIO3_12/**EC1_RXD0**/ FTM1_CH0	General Purpose Input/Output	AB2	IO	LVDD	–
GPIO3_13/**EC1_RX_CLK**/ FTM1_QD_PHA	General Purpose Input/Output	Y1	IO	LVDD	–
GPIO3_14/**EC1_RX_DV**/ FTM1_QD_PHB	General Purpose Input/Output	AC1	IO	LVDD	–
GPIO3_15/**EC2_TXD3**/ TSEC_1588_ALARM_OUT2/ FTM2_CH5	General Purpose Input/Output	AE3	IO	LVDD	–
GPIO3_16/**EC2_TXD2**/ TSEC_1588_ALARM_OUT1/ FTM2_CH7	General Purpose Input/Output	AF3	IO	LVDD	–
GPIO3_17/**EC2_TXD1**/ TSEC_1588_CLK_OUT/ FTM2_CH3	General Purpose Input/Output	AF4	IO	LVDD	–
GPIO3_18/**EC2_TXD0**/ TSEC_1588_PULSE_OUT2/ FTM2_CH2	General Purpose Input/Output	AG3	IO	LVDD	–
GPIO3_19/**EC2_TX_EN**/ FTM2_FAULT	General Purpose Input/Output	AH3	IO	LVDD	–
GPIO3_20/**EC2_GTX_CLK**/ FTM2_EXTCLK	General Purpose Input/Output	AD4	IO	LVDD	–
GPIO3_21/**EC2_GTX_CLK125**	General Purpose Input/Output	AH4	IO	LVDD	–
GPIO3_22/**EC2_RXD3**/ FTM2_CH4	General Purpose Input/Output	AD2	IO	LVDD	–
GPIO3_23/**EC2_RXD2**/ FTM2_CH6	General Purpose Input/Output	AE1	IO	LVDD	–
GPIO3_24/**EC2_RXD1**/ TSEC_1588_PULSE_OUT1/ FTM2_CH1	General Purpose Input/Output	AF1	IO	LVDD	–
GPIO3_25/**EC2_RXD0**/ TSEC_1588_TRIG_IN2/ FTM2_CH0	General Purpose Input/Output	AF2	IO	LVDD	–
GPIO3_26/**EC2_RX_CLK**/ TSEC_1588_CLK_IN/ FTM2_QD_PHA	General Purpose Input/Output	AD1	IO	LVDD	–
GPIO3_27/**EC2_RX_DV**/ TSEC_1588_TRIG_IN1/ FTM2_QD_PHB	General Purpose Input/Output	AG1	IO	LVDD	–

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GPIO4_00/**EMI2_MDC**	General Purpose Input/Output	AJ4	IO	TVDD	–
GPIO4_01/**EMI2_MDIO**	General Purpose Input/Output	AJ3	IO	TVDD	–
GPIO4_10/**IIC3_SCL**/EVT5_B/ USB2_DRVVBUS/FTM8_CH0	General Purpose Input/Output	M4	IO	DVDD	–
GPIO4_11/**IIC3_SDA**/EVT6_B/ USB2_PWRFAULT/ FTM8_CH1	General Purpose Input/Output	N4	IO	DVDD	–
GPIO4_12/**IIC4_SCL**/EVT7_B/ USB3_DRVVBUS/ FTM3_FAULT	General Purpose Input/Output	N3	IO	DVDD	–
GPIO4_13/**IIC4_SDA**/EVT8_B/ USB3_PWRFAULT/ FTM3_EXTCLK	General Purpose Input/Output	P3	IO	DVDD	–
GPIO4_2/**IIC2_SCL**/ SDHC_CD_B/FTM3_QD_PHA	General Purpose Input/Output	L3	IO	DVDD	–
GPIO4_29/**USB_DRVVBUS**	General Purpose Input/Output	J6	IO	DVDD	–
GPIO4_3/**IIC2_SDA**/ SDHC_WP/FTM3_QD_PHB	General Purpose Input/Output	M3	IO	DVDD	–
GPIO4_30/**USB_PWRFAULT**	General Purpose Input/Output	H6	IO	DVDD	–
Frequency Timer Module					
FTM1_CH0/**EC1_RXD0**/ GPIO3_12	Channel 0	AB2	IO	LVDD	–
FTM1_CH1/**EC1_RXD1**/ GPIO3_11	Channel 1	AB1	IO	LVDD	–
FTM1_CH2/**EC1_TXD0**/ GPIO3_05	Channel 2	AC3	IO	LVDD	–
FTM1_CH3/**EC1_TXD1**/ GPIO3_04	Channel 3	AB3	IO	LVDD	–
FTM1_CH4/**EC1_RXD3**/ GPIO3_09	Channel 4	Y2	IO	LVDD	–
FTM1_CH5/**EC1_TXD3**/ GPIO3_02	Channel 5	AA3	IO	LVDD	–
FTM1_CH6/**EC1_RXD2**/ GPIO3_10	Channel 6	AA1	IO	LVDD	–
FTM1_CH7/**EC1_TXD2**/ GPIO3_03	Channel 7	AA4	IO	LVDD	–
FTM1_EXTCLK/ **EC1_GTX_CLK**/GPIO3_07	External Clock	Y4	I	LVDD	1
FTM1_FAULT/EC1_TX_EN/ GPIO3_06	Fault	AC4	I	LVDD	1
FTM1_QD_PHA/ **EC1_RX_CLK**/GPIO3_13	Phase A	Y1	I	LVDD	1
FTM1_QD_PHB/**EC1_RX_DV**/ GPIO3_14	Phase B	AC1	I	LVDD	1
FTM2_CH0/**EC2_RXD0**/ GPIO3_25/ TSEC_1588_TRIG_IN2	Channel 0	AF2	IO	LVDD	–
FTM2_CH1/**EC2_RXD1**/ GPIO3_24/ TSEC_1588_PULSE_OUT1	Channel 1	AF1	IO	LVDD	–
FTM2_CH2/**EC2_TXD0**/ GPIO3_18/ TSEC_1588_PULSE_OUT2	Channel 2	AG3	IO	LVDD	–
FTM2_CH3/**EC2_TXD1**/ GPIO3_17/ TSEC_1588_CLK_OUT	Channel 3	AF4	IO	LVDD	–
FTM2_CH4/**EC2_RXD3**/ GPIO3_22	Channel 4	AD2	IO	LVDD	–
FTM2_CH5/**EC2_TXD3**/ GPIO3_15/ TSEC_1588_ALARM_OUT2	Channel 5	AE3	IO	LVDD	–
FTM2_CH6/**EC2_RXD2**/ GPIO3_23	Channel 6	AE1	IO	LVDD	–

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Signal	Signal description	Package pin number	Pin type	Power supply	Notes
FTM2_CH7/**EC2_TXD2**/ GPIO3_16/ TSEC_1588_ALARM_OUT1	Channel 7	AF3	IO	LVDD	–
FTM2_EXTCLK/ **EC2_GTX_CLK**/GPIO3_20	External Clock	AD4	I	LVDD	1
FTM2_FAULT/**EC2_TX_EN**/ GPIO3_19	Fault	AH3	I	LVDD	1
FTM2_QD_PHA/ **EC2_RX_CLK**/GPIO3_26/ TSEC_1588_CLK_IN	Phase A	AD1	I	LVDD	1
FTM2_QD_PHB/**EC2_RX_DV**/ GPIO3_27/ TSEC_1588_TRIG_IN1	Phase B	AG1	I	LVDD	1
FTM3_CH0/**IRQ04**/GPIO1_24	Channel 0	K4	IO	DVDD	–
FTM3_CH1/**IRQ05**/GPIO1_25	Channel 1	K5	IO	DVDD	–
FTM3_CH2/**IRQ06**/GPIO1_26	Channel 2	L5	IO	DVDD	–
FTM3_CH3/**IRQ07**/GPIO1_27	Channel 3	M5	IO	DVDD	–
FTM3_CH4/**IRQ08**/GPIO1_28	Channel 4	N5	IO	DVDD	–
FTM3_CH5/**IRQ09**/GPIO1_29	Channel 5	P5	IO	DVDD	–
FTM3_CH6/**IRQ10**/GPIO1_30	Channel 6	R4	IO	DVDD	–
FTM3_CH7/**IRQ03**/GPIO1_23	Channel 7	K3	IO	DVDD	–
FTM3_EXTCLK/**IIC4_SDA**/ GPIO4_13/EVT8_B/ USB3_PWRFAULT	External Clock	P3	I	DVDD	1
FTM3_FAULT/**IIC4_SCL**/ GPIO4_12/EVT7_B/ USB3_DRVVBUS	Fault	N3	I	DVDD	1
FTM3_QD_PHA/**IIC2_SCL**/ GPIO4_2/SDHC_CD_B	Phase A	L3	I	DVDD	1
FTM3_QD_PHB/**IIC2_SDA**/ GPIO4_3/SDHC_WP	Phase B	M3	I	DVDD	1
FTM4_CH0/**UART2_SOUT**/ GPIO1_16/LPUART1_SOUT	Channel 0	M2	IO	DVDD	–
FTM4_CH1/**UART2_SIN**/ GPIO1_18/LPUART1_SIN	Channel 1	L1	IO	DVDD	–
FTM4_CH2/**UART1_RTS_B**/ GPIO1_19/UART3_SOUT/ LPUART2_SOUT	Channel 2	K2	IO	DVDD	–
FTM4_CH3/**UART2_RTS_B**/ GPIO1_20/UART4_SOUT/ LPUART4_SOUT/ LPUART1_RTS_B	Channel 3	M1	IO	DVDD	–
FTM4_CH4/**UART1_CTS_B**/ GPIO1_21/UART3_SIN/ LPUART2_SIN	Channel 4	K1	IO	DVDD	–
FTM4_CH5/**UART2_CTS_B**/ GPIO1_22/UART4_SIN/ LPUART1_CTS_B/ LPUART4_SIN	Channel 5	N2	IO	DVDD	–
FTM4_CH6/**SDHC_CMD**/ GPIO2_04/LPUART3_SOUT	Channel 6	R2	IO	EVDD	–
FTM4_CH7/**SDHC_DAT0**/ GPIO2_05/LPUART3_SIN	Channel 7	R1	IO	EVDD	–
FTM4_EXTCLK/**SDHC_DAT2**/ GPIO2_07/LPUART2_CTS_B/ LPUART5_SIN	External Clock	T1	I	EVDD	1
FTM4_FAULT/**SDHC_DAT1**/ GPIO2_06/LPUART5_SOUT/ LPUART2_RTS_B	Fault	T2	I	EVDD	1
FTM4_QD_PHA/**SDHC_DAT3**/ GPIO2_08/LPUART6_SOUT/ LPUART3_RTS_B	Phase A	U1	I	EVDD	1

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FTM4_QD_PHB/**SDHC_CLK**/ GPIO2_09/LPUART3_CTS_B/ LPUART6_SIN	Phase B	R3	I	EVDD	1
FTM5_CH0/**IFC_A25**/ GPIO2_25/QSPI_A_DATA3/ IFC_CS4_B/IFC_RB2_B	Channel 0	D13	IO	OVDD	–
FTM5_CH1/**IFC_A26**/ GPIO2_26/IFC_CS5_B/ IFC_RB3_B	Channel 1	E14	IO	OVDD	–
FTM5_EXTCLK/**IFC_A27**/ GPIO2_27/IFC_CS6_B	External Clock	D14	I	OVDD	1
FTM6_CH0/**IFC_PAR0**/ GPIO2_13/QSPI_B_DATA0	Channel 0	C18	IO	OVDD	–
FTM6_CH1/**IFC_PAR1**/ GPIO2_14/QSPI_B_DATA1	Channel 1	E17	IO	OVDD	–
FTM6_EXTCLK/**IFC_PERR_B**/ GPIO2_15/QSPI_B_DATA2	External Clock	F17	I	OVDD	1
FTM7_CH0/**IFC_CS1_B**/ GPIO2_10	Channel 0	B19	IO	OVDD	–
FTM7_CH1/**IFC_CS2_B**/ GPIO2_11	Channel 1	E20	IO	OVDD	–
FTM7_EXTCLK/**IFC_CS3_B**/ GPIO2_12/QSPI_B_DATA3	External Clock	D20	I	OVDD	1
FTM8_CH0/**IIC3_SCL**/ GPIO4_10/EVT5_B/ USB2_DRVVBUS	Channel 0	M4	IO	DVDD	–
FTM8_CH1/**IIC3_SDA**/ GPIO4_11/EVT6_B/ USB2_PWRFAULT	Channel 1	N4	IO	DVDD	–
LPUART					
LPUART1_CTS_B/ **UART2_CTS_B**/GPIO1_22/ UART4_SIN/FTM4_CH5/ LPUART4_SIN	Clear to send	N2	I	DVDD	1
LPUART1_RTS_B/ **UART2_RTS_B**/GPIO1_20/ UART4_SOUT/ LPUART4_SOUT/FTM4_CH3	Request to send	M1	O	DVDD	1
LPUART1_SIN/**UART2_SIN**/ GPIO1_18/FTM4_CH1	Receive data	L1	I	DVDD	1
LPUART1_SOUT/ **UART2_SOUT**/GPIO1_16/ FTM4_CH0	Transmit data	M2	IO	DVDD	–
LPUART2_CTS_B/ **SDHC_DAT2**/GPIO2_07/	Clear to send	T1	I	EVDD	1
LPUART5_SIN/ FTM4_EXTCLK					
LPUART2_RTS_B/ **SDHC_DAT1**/GPIO2_06/ LPUART5_SOUT/ FTM4_FAULT	Request to send	T2	O	EVDD	1
LPUART2_SIN/ **UART1_CTS_B**/GPIO1_21/ UART3_SIN/FTM4_CH4	Receive data	K1	I	DVDD	1
LPUART2_SOUT/ **UART1_RTS_B**/GPIO1_19/ UART3_SOUT/FTM4_CH2	Transmit data	K2	IO	DVDD	–
LPUART3_CTS_B/ **SDHC_CLK**/GPIO2_09/ LPUART6_SIN/ FTM4_QD_PHB	Clear to send	R3	I	EVDD	1
LPUART3_RTS_B/ **SDHC_DAT3**/GPIO2_08/ LPUART6_SOUT/ FTM4_QD_PHA	Request to send	U1	O	EVDD	1
LPUART3_SIN/**SDHC_DAT0**/ GPIO2_05/FTM4_CH7	Receive data	R1	I	EVDD	1
LPUART3_SOUT/ **SDHC_CMD**/GPIO2_04/ FTM4_CH6	Transmit data	R2	IO	EVDD	–
LPUART4_SIN/ **UART2_CTS_B**/GPIO1_22/ UART4_SIN/FTM4_CH5/ LPUART1_CTS_B	Receive data	N2	I	DVDD	1

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LPUART4_SOUT/ **UART2_RTS_B**/GPIO1_20/ UART4_SOUT/FTM4_CH3/ LPUART1_RTS_B	Transmit data	M1	IO	DVDD	–
LPUART5_SIN/SDHC_DAT2/ **GPIO2_07**/LPUART2_CTS_B/ FTM4_EXTCLK	Receive data	T1	I	EVDD	1
LPUART5_SOUT/ **SDHC_DAT1**/GPIO2_06/ FTM4_FAULT/ LPUART2_RTS_B	Transmit data	T2	IO	EVDD	–
LPUART6_SIN/**SDHC_CLK**/ GPIO2_09/LPUART3_CTS_B/ FTM4_QD_PHB	Receive data	R3	I	EVDD	1
LPUART6_SOUT/ **SDHC_DAT3**/GPIO2_08/ FTM4_QD_PHA/ LPUART3_RTS_B	Transmit data	U1	IO	EVDD	–
TSEC_1588					
TSEC_1588_ALARM_OUT1/ **EC2_TXD2**/GPIO3_16/ FTM2_CH7	Alarm Out	AF3	O	LVDD	1
TSEC_1588_ALARM_OUT2/ **EC2_TXD3**/GPIO3_15/ FTM2_CH5	Alarm Out	AE3	O	LVDD	1
TSEC_1588_CLK_IN/ **EC2_RX_CLK**/GPIO3_26/ FTM2_QD_PHA	Clock In	AD1	I	LVDD	1
TSEC_1588_CLK_OUT/ **EC2_TXD1**/GPIO3_17/ FTM2_CH3	Clock Out	AF4	O	LVDD	1
TSEC_1588_PULSE_OUT1/ **EC2_RXD1**/GPIO3_24/ FTM2_CH1	Pulse Out	AF1	O	LVDD	1
TSEC_1588_PULSE_OUT2/ **EC2_TXD0**/GPIO3_18/ FTM2_CH2	Pulse Out	AG3	O	LVDD	1
TSEC_1588_TRIG_IN1/ **EC2_RX_DV**/GPIO3_27/ FTM2_QD_PHB	Trigger In	AG1	I	LVDD	1
TSEC_1588_TRIG_IN2/ **EC2_RXD0**/GPIO3_25/ FTM2_CH0	Trigger In	AF2	I	LVDD	1
Power and Ground Signals					
GND001	GND	A1	–	–	–
GND002	GND	B1	–	–	–
GND003	GND	D1	–	–	–
GND004	GND	F1	–	–	–
GND005	GND	H1	–	–	–
GND006	GND	AH1	–	–	–
GND007	GND	AJ1	–	–	–
GND008	GND	AK1	–	–	–
GND009	GND	A2	–	–	–
GND010	GND	B2	–	–	–
GND011	GND	D2	–	–	–
GND012	GND	F2	–	–	–
GND013	GND	H2	–	–	–
GND014	GND	L2	–	–	–
GND015	GND	P2	–	–	–

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GND016	GND	U2	–	–	–
GND017	GND	W2	–	–	–
GND018	GND	AA2	–	–	–
GND019	GND	AC2	–	–	–
GND020	GND	AE2	–	–	–
GND021	GND	AJ2	–	–	–
GND022	GND	AK2	–	–	–
GND023	GND	A3	–	–	–
GND024	GND	C3	–	–	–
GND025	GND	E3	–	–	–
GND026	GND	G3	–	–	–
GND027	GND	J3	–	–	–
GND028	GND	AK3	–	–	–
GND029	GND	A4	–	–	–
GND030	GND	C4	–	–	–
GND031	GND	E4	–	–	–
GND032	GND	G4	–	–	–
GND033	GND	J4	–	–	–
GND034	GND	L4	–	–	–
GND035	GND	P4	–	–	–
GND036	GND	T4	–	–	–
GND037	GND	U4	–	–	–
GND038	GND	V4	–	–	–
GND039	GND	W4	–	–	–
GND040	GND	AB4	–	–	–
GND041	GND	AE4	–	–	–
GND042	GND	AG4	–	–	–
GND043	GND	AK4	–	–	–
GND044	GND	A5	–	–	–
GND045	GND	B5	–	–	–
GND046	GND	D5	–	–	–
GND047	GND	F5	–	–	–
GND048	GND	J5	–	–	–
GND049	GND	R5	–	–	–
GND050	GND	T5	–	–	–

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GND051	GND	U5	–	–	–
GND052	GND	V5	–	–	–
GND053	GND	W5	–	–	–
GND054	GND	Y5	–	–	–
GND055	GND	AA5	–	–	–
GND056	GND	AK5	–	–	–
GND057	GND	A6	–	–	–
GND058	GND	K6	–	–	–
GND059	GND	L6	–	–	–
GND060	GND	M6	–	–	–
GND061	GND	N6	–	–	–
GND062	GND	P6	–	–	–
GND063	GND	R6	–	–	–
GND064	GND	U6	–	–	–
GND065	GND	V6	–	–	–
GND066	GND	W6	–	–	–
GND067	GND	AK6	–	–	–
GND068	GND	A7	–	–	–
GND069	GND	C7	–	–	–
GND070	GND	E7	–	–	–
GND071	GND	G7	–	–	–
GND072	GND	K7	–	–	–
GND073	GND	Y7	–	–	–
GND074	GND	AK7	–	–	–
GND075	GND	A8	–	–	–
GND076	GND	K8	–	–	–
GND077	GND	P8	–	–	–
GND078	GND	R8	–	–	–
GND079	GND	T8	–	–	–
GND080	GND	U8	–	–	–
GND081	GND	V8	–	–	–
GND082	GND	W8	–	–	–
GND083	GND	Y8	–	–	–
GND084	GND	AK8	–	–	–

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GND085	GND	A9	–	–	–
GND086	GND	E9	–	–	–
GND087	GND	H9	–	–	–
GND088	GND	K9	–	–	–
GND089	GND	L9	–	–	–
GND090	GND	M9	–	–	–
GND091	GND	N9	–	–	–
GND092	GND	R9	–	–	–
GND093	GND	U9	–	–	–
GND094	GND	W9	–	–	–
GND095	GND	Y9	–	–	–
GND096	GND	AK9	–	–	–
GND097	GND	A10	–	–	–
GND098	GND	C10	–	–	–
GND099	GND	H10	–	–	–
GND100	GND	K10	–	–	–
GND101	GND	L10	–	–	–
GND102	GND	M10	–	–	–
GND103	GND	P10	–	–	–
GND104	GND	T10	–	–	–
GND105	GND	V10	–	–	–
GND106	GND	AK10	–	–	–
GND107	GND	A11	–	–	–
GND108	GND	H11	–	–	–
GND109	GND	K11	–	–	–
GND110	GND	L11	–	–	–
GND111	GND	N11	–	–	–
GND112	GND	R11	–	–	–
GND113	GND	U11	–	–	–
GND114	GND	W11	–	–	–
GND115	GND	AK11	–	–	–
GND116	GND	A12	–	–	–
GND117	GND	E12	–	–	–
GND118	GND	G12	–	–	–
GND119	GND	K12	–	–	–

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GND120	GND	L12	–	–	–
GND121	GND	M12	–	–	–
GND122	GND	P12	–	–	–
GND123	GND	T12	–	–	–
GND124	GND	V12	–	–	–
GND125	GND	Y12	–	–	–
GND126	GND	AC12	–	–	–
GND127	GND	AK12	–	–	–
GND128	GND	A13	–	–	–
GND129	GND	C13	–	–	–
GND130	GND	L13	–	–	–
GND131	GND	N13	–	–	–
GND132	GND	R13	–	–	–
GND133	GND	U13	–	–	–
GND134	GND	W13	–	–	–
GND135	GND	AA13	–	–	–
GND136	GND	AK13	–	–	–
GND137	GND	A14	–	–	–
GND138	GND	G14	–	–	–
GND139	GND	J14	–	–	–
GND140	GND	M14	–	–	–
GND141	GND	P14	–	–	–
GND142	GND	T14	–	–	–
GND143	GND	V14	–	–	–
GND144	GND	AA14	–	–	–
GND145	GND	AB14	–	–	–
GND146	GND	AK14	–	–	–
GND147	GND	A15	–	–	–
GND148	GND	E15	–	–	–
GND149	GND	J15	–	–	–
GND150	GND	L15	–	–	–
GND151	GND	N15	–	–	–
GND152	GND	R15	–	–	–
GND153	GND	U15	–	–	–

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GND154	GND	W15	–	–	–
GND155	GND	AK15	–	–	–
GND156	GND	A16	–	–	–
GND157	GND	C16	–	–	–
GND158	GND	G16	–	–	–
GND159	GND	J16	–	–	–
GND160	GND	M16	–	–	–
GND161	GND	P16	–	–	–
GND162	GND	T16	–	–	–
GND163	GND	V16	–	–	–
GND164	GND	AK16	–	–	–
GND165	GND	A17	–	–	–
GND166	GND	J17	–	–	–
GND167	GND	L17	–	–	–
GND168	GND	N17	–	–	–
GND169	GND	R17	–	–	–
GND170	GND	U17	–	–	–
GND171	GND	W17	–	–	–
GND172	GND	AK17	–	–	–
GND173	GND	A18	–	–	–
GND174	GND	E18	–	–	–
GND175	GND	G18	–	–	–
GND176	GND	J18	–	–	–
GND177	GND	M18	–	–	–
GND178	GND	P18	–	–	–
GND179	GND	T18	–	–	–
GND180	GND	V18	–	–	–
GND181	GND	Y18	–	–	–
GND182	GND	AK18	–	–	–
GND183	GND	A19	–	–	–
GND184	GND	C19	–	–	–
GND185	GND	L19	–	–	–
GND186	GND	N19	–	–	–
GND187	GND	R19	–	–	–
GND188	GND	U19	–	–	–

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GND189	GND	W19	–	–	–
GND190	GND	AK19	–	–	–
GND191	GND	A20	–	–	–
GND192	GND	M20	–	–	–
GND193	GND	N20	–	–	–
GND194	GND	P20	–	–	–
GND195	GND	R20	–	–	–
GND196	GND	T20	–	–	–
GND197	GND	U20	–	–	–
GND198	GND	V20	–	–	–
GND199	GND	Y20	–	–	–
GND200	GND	AK20	–	–	–
GND201	GND	A21	–	–	–
GND202	GND	B21	–	–	–
GND203	GND	C21	–	–	–
GND204	GND	D21	–	–	–
GND205	GND	E21	–	–	–
GND206	GND	F21	–	–	–
GND207	GND	H21	–	–	–
GND208	GND	J21	–	–	–
GND209	GND	K21	–	–	–
GND210	GND	L21	–	–	–
GND211	GND	M21	–	–	–
GND212	GND	N21	–	–	–
GND213	GND	P21	–	–	–
GND214	GND	R21	–	–	–
GND215	GND	U21	–	–	–
GND216	GND	V21	–	–	–
GND217	GND	W21	–	–	–
GND218	GND	Y21	–	–	–
GND219	GND	AA21	–	–	–
GND220	GND	AB21	–	–	–
GND221	GND	AD21	–	–	–
GND222	GND	AF21	–	–	–

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Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND223	GND	AG21	–	–	–
GND224	GND	AJ21	–	–	–
GND225	GND	AK21	–	–	–
GND226	GND	A22	–	–	–
GND227	GND	C22	–	–	–
GND228	GND	E22	–	–	–
GND229	GND	G22	–	–	–
GND230	GND	J22	–	–	–
GND231	GND	L22	–	–	–
GND232	GND	Y22	–	–	–
GND233	GND	AA22	–	–	–
GND234	GND	AC22	–	–	–
GND235	GND	AE22	–	–	–
GND236	GND	AG22	–	–	–
GND237	GND	AJ22	–	–	–
GND238	GND	AK22	–	–	–
GND239	GND	A23	–	–	–
GND240	GND	B23	–	–	–
GND241	GND	D23	–	–	–
GND242	GND	F23	–	–	–
GND243	GND	H23	–	–	–
GND244	GND	K23	–	–	–
GND245	GND	M23	–	–	–
GND246	GND	N23	–	–	–
GND247	GND	P23	–	–	–
GND248	GND	R23	–	–	–
GND249	GND	T23	–	–	–
GND250	GND	U23	–	–	–
GND251	GND	V23	–	–	–
GND252	GND	W23	–	–	–
GND253	GND	Y23	–	–	–
GND254	GND	AA23	–	–	–
GND255	GND	AB23	–	–	–
GND256	GND	AD23	–	–	–
GND257	GND	AF23	–	–	–

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Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND258	GND	AH23	–	–	–
GND259	GND	AK23	–	–	–
GND260	GND	A24	–	–	–
GND261	GND	C24	–	–	–
GND262	GND	E24	–	–	–
GND263	GND	G24	–	–	–
GND264	GND	J24	–	–	–
GND265	GND	L24	–	–	–
GND266	GND	N24	–	–	–
GND267	GND	R24	–	–	–
GND268	GND	U24	–	–	–
GND269	GND	W24	–	–	–
GND270	GND	AA24	–	–	–
GND271	GND	AB24	–	–	–
GND272	GND	AC24	–	–	–
GND273	GND	AD24	–	–	–
GND274	GND	AE24	–	–	–
GND275	GND	AF24	–	–	–
GND276	GND	AG24	–	–	–
GND277	GND	AH24	–	–	–
GND278	GND	AJ24	–	–	–
GND279	GND	AK24	–	–	–
GND280	GND	A25	–	–	–
GND281	GND	B25	–	–	–
GND282	GND	D25	–	–	–
GND283	GND	F25	–	–	–
GND284	GND	H25	–	–	–
GND285	GND	K25	–	–	–
GND286	GND	M25	–	–	–
GND287	GND	P25	–	–	–
GND288	GND	T25	–	–	–
GND289	GND	V25	–	–	–
GND290	GND	Y25	–	–	–
GND291	GND	AB25	–	–	–

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Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND292	GND	AD25	–	–	–
GND293	GND	AF25	–	–	–
GND294	GND	AH25	–	–	–
GND295	GND	AK25	–	–	–
GND296	GND	A26	–	–	–
GND297	GND	C26	–	–	–
GND298	GND	E26	–	–	–
GND299	GND	F26	–	–	–
GND300	GND	G26	–	–	–
GND301	GND	H26	–	–	–
GND302	GND	J26	–	–	–
GND303	GND	K26	–	–	–
GND304	GND	L26	–	–	–
GND305	GND	M26	–	–	–
GND306	GND	N26	–	–	–
GND307	GND	P26	–	–	–
GND308	GND	R26	–	–	–
GND309	GND	T26	–	–	–
GND310	GND	U26	–	–	–
GND311	GND	W26	–	–	–
GND312	GND	AA26	–	–	–
GND313	GND	AC26	–	–	–
GND314	GND	AE26	–	–	–
GND315	GND	AG26	–	–	–
GND316	GND	AH26	–	–	–
GND317	GND	AJ26	–	–	–
GND318	GND	AK26	–	–	–
GND319	GND	A27	–	–	–
GND320	GND	B27	–	–	–
GND321	GND	D27	–	–	–
GND322	GND	F27	–	–	–
GND323	GND	H27	–	–	–
GND324	GND	K27	–	–	–
GND325	GND	M27	–	–	–
GND326	GND	P27	–	–	–

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Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND327	GND	T27	–	–	–
GND328	GND	AK27	–	–	–
GND329	GND	A28	–	–	–
GND330	GND	C28	–	–	–
GND331	GND	E28	–	–	–
GND332	GND	J28	–	–	–
GND333	GND	L28	–	–	–
GND334	GND	N28	–	–	–
GND335	GND	R28	–	–	–
GND336	GND	T28	–	–	–
GND337	GND	U28	–	–	–
GND338	GND	W28	–	–	–
GND339	GND	AC28	–	–	–
GND340	GND	AE28	–	–	–
GND341	GND	AG28	–	–	–
GND342	GND	AJ28	–	–	–
GND343	GND	AK28	–	–	–
GND344	GND	A29	–	–	–
GND345	GND	B29	–	–	–
GND346	GND	D29	–	–	–
GND347	GND	F29	–	–	–
GND348	GND	H29	–	–	–
GND349	GND	K29	–	–	–
GND350	GND	M29	–	–	–
GND351	GND	P29	–	–	–
GND352	GND	T29	–	–	–
GND353	GND	V29	–	–	–
GND354	GND	Y29	–	–	–
GND355	GND	AB29	–	–	–
GND356	GND	AD29	–	–	–
GND357	GND	AF29	–	–	–
GND358	GND	AH29	–	–	–
GND359	GND	AK29	–	–	–
GND360	GND	A30	–	–	–

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Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND361	GND	C30	–	–	–
GND362	GND	E30	–	–	–
GND363	GND	G30	–	–	–
GND364	GND	J30	–	–	–
GND365	GND	L30	–	–	–
GND366	GND	N30	–	–	–
GND367	GND	R30	–	–	–
GND368	GND	T30	–	–	–
GND369	GND	U30	–	–	–
GND370	GND	W30	–	–	–
GND371	GND	AA30	–	–	–
GND372	GND	AC30	–	–	–
GND373	GND	AE30	–	–	–
GND374	GND	AG30	–	–	–
GND375	GND	AJ30	–	–	–
GND376	GND	AK30	–	–	–
GND377	GND	A31	–	–	–
GND378	GND	B31	–	–	–
GND379	GND	D31	–	–	–
GND380	GND	F31	–	–	–
GND381	GND	H31	–	–	–
GND382	GND	K31	–	–	–
GND383	GND	M31	–	–	–
GND384	GND	P31	–	–	–
GND385	GND	Y31	–	–	–
GND386	GND	AB31	–	–	–
GND387	GND	AD31	–	–	–
GND388	GND	AF31	–	–	–
GND389	GND	AH31	–	–	–
GND390	GND	AK31	–	–	–
GND391	GND	A32	–	–	–
GND392	GND	C32	–	–	–
GND393	GND	E32	–	–	–
GND394	GND	G32	–	–	–
GND395	GND	J32	–	–	–

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Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND396	GND	L32	–	–	–
GND397	GND	N32	–	–	–
GND398	GND	R32	–	–	–
GND399	GND	W32	–	–	–
GND400	GND	AA32	–	–	–
GND401	GND	AC32	–	–	–
GND402	GND	AE32	–	–	–
GND403	GND	AG32	–	–	–
GND404	GND	AJ32	–	–	–
GND405	GND	AK32	–	–	–
GND406	GND	A33	–	–	–
GND407	GND	B33	–	–	–
GND408	GND	D33	–	–	–
GND409	GND	F33	–	–	–
GND410	GND	H33	–	–	–
GND411	GND	K33	–	–	–
GND412	GND	M33	–	–	–
GND413	GND	P33	–	–	–
GND414	GND	Y33	–	–	–
GND415	GND	AB33	–	–	–
GND416	GND	AD33	–	–	–
GND417	GND	AF33	–	–	–
GND418	GND	AH33	–	–	–
GND419	GND	AK33	–	–	–
GND420	GND	A34	–	–	–
GND421	GND	C34	–	–	–
GND422	GND	E34	–	–	–
GND423	GND	G34	–	–	–
GND424	GND	J34	–	–	–
GND425	GND	L34	–	–	–
GND426	GND	N34	–	–	–
GND427	GND	R34	–	–	–
GND428	GND	W34	–	–	–
GND429	GND	AA34	–	–	–

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Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND430	GND	AC34	–	–	–
GND431	GND	AE34	–	–	–
GND432	GND	AG34	–	–	–
GND433	GND	AJ34	–	–	–
GND434	GND	AK34	–	–	–
GND435	GND	A35	–	–	–
GND436	GND	B35	–	–	–
GND437	GND	D35	–	–	–
GND438	GND	F35	–	–	–
GND439	GND	H35	–	–	–
GND440	GND	K35	–	–	–
GND441	GND	M35	–	–	–
GND442	GND	P35	–	–	–
GND443	GND	Y35	–	–	–
GND444	GND	AB35	–	–	–
GND445	GND	AD35	–	–	–
GND446	GND	AF35	–	–	–
GND447	GND	AH35	–	–	–
GND448	GND	AK35	–	–	–
GND449	GND	A36	–	–	–
GND450	GND	C36	–	–	–
GND451	GND	E36	–	–	–
GND452	GND	G36	–	–	–
GND453	GND	J36	–	–	–
GND454	GND	L36	–	–	–
GND455	GND	N36	–	–	–
GND456	GND	R36	–	–	–
GND457	GND	W36	–	–	–
GND458	GND	AA36	–	–	–
GND459	GND	AC36	–	–	–
GND460	GND	AE36	–	–	–
GND461	GND	AG36	–	–	–
GND462	GND	AJ36	–	–	–
GND463	GND	AK36	–	–	–
GND464	GND	A37	–	–	–

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Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND465	GND	B37	–	–	–
GND466	GND	D37	–	–	–
GND467	GND	F37	–	–	–
GND468	GND	H37	–	–	–
GND469	GND	K37	–	–	–
GND470	GND	M37	–	–	–
GND471	GND	P37	–	–	–
GND472	GND	Y37	–	–	–
GND473	GND	AB37	–	–	–
GND474	GND	AD37	–	–	–
GND475	GND	AF37	–	–	–
GND476	GND	AH37	–	–	–
GND477	GND	AK37	–	–	–
GND478	GND	A38	–	–	–
GND479	GND	C38	–	–	–
GND480	GND	E38	–	–	–
GND481	GND	G38	–	–	–
GND482	GND	J38	–	–	–
GND483	GND	L38	–	–	–
GND484	GND	N38	–	–	–
GND485	GND	R38	–	–	–
GND486	GND	W38	–	–	–
GND487	GND	AA38	–	–	–
GND488	GND	AC38	–	–	–
GND489	GND	AE38	–	–	–
GND490	GND	AG38	–	–	–
GND491	GND	AJ38	–	–	–
GND492	GND	AK38	–	–	–
GND493	GND	A39	–	–	–
GND494	GND	B39	–	–	–
GND495	GND	D39	–	–	–
GND496	GND	F39	–	–	–
GND497	GND	H39	–	–	–
GND498	GND	K39	–	–	–

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Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND499	GND	M39	–	–	–
GND500	GND	P39	–	–	–
GND501	GND	T39	–	–	–
GND502	GND	V39	–	–	–
GND503	GND	Y39	–	–	–
GND504	GND	AB39	–	–	–
GND505	GND	AD39	–	–	–
GND506	GND	AF39	–	–	–
GND507	GND	AH39	–	–	–
GND508	GND	AK39	–	–	–
GND509	GND	A40	–	–	–
GND510	GND	C40	–	–	–
GND511	GND	E40	–	–	–
GND512	GND	G40	–	–	–
GND513	GND	J40	–	–	–
GND514	GND	L40	–	–	–
GND515	GND	N40	–	–	–
GND516	GND	R40	–	–	–
GND517	GND	U40	–	–	–
GND518	GND	W40	–	–	–
GND519	GND	AA40	–	–	–
GND520	GND	AC40	–	–	–
GND521	GND	AE40	–	–	–
GND522	GND	AG40	–	–	–
GND523	GND	AJ40	–	–	–
GND524	GND	AK40	–	–	–
GND525	GND	A41	–	–	–
GND526	GND	B41	–	–	–
GND527	GND	D41	–	–	–
GND528	GND	F41	–	–	–
GND529	GND	H41	–	–	–
GND530	GND	K41	–	–	–
GND531	GND	M41	–	–	–
GND532	GND	P41	–	–	–
GND533	GND	T41	–	–	–

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Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND534	GND	V41	–	–	–
GND535	GND	Y41	–	–	–
GND536	GND	AB41	–	–	–
GND537	GND	AD41	–	–	–
GND538	GND	AF41	–	–	–
GND539	GND	AH41	–	–	–
GND540	GND	AK41	–	–	–
GND541	GND	A42	–	–	–
GND542	GND	C42	–	–	–
GND543	GND	E42	–	–	–
GND544	GND	G42	–	–	–
GND545	GND	J42	–	–	–
GND546	GND	L42	–	–	–
GND547	GND	N42	–	–	–
GND548	GND	R42	–	–	–
GND549	GND	U42	–	–	–
GND550	GND	W42	–	–	–
GND551	GND	AA42	–	–	–
GND552	GND	AC42	–	–	–
GND553	GND	AE42	–	–	–
GND554	GND	AG42	–	–	–
GND555	GND	AJ42	–	–	–
GND556	GND	AK42	–	–	–
GND557	GND	A43	–	–	–
GND558	GND	B43	–	–	–
GND559	GND	D43	–	–	–
GND560	GND	F43	–	–	–
GND561	GND	H43	–	–	–
GND562	GND	K43	–	–	–
GND563	GND	M43	–	–	–
GND564	GND	P43	–	–	–
GND565	GND	T43	–	–	–
GND566	GND	V43	–	–	–
GND567	GND	Y43	–	–	–

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Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND568	GND	AB43	–	–	–
GND569	GND	AD43	–	–	–
GND570	GND	AF43	–	–	–
GND571	GND	AH43	–	–	–
GND572	GND	AK43	–	–	–
GND573	GND	A44	–	–	–
GND574	GND	C44	–	–	–
GND575	GND	E44	–	–	–
GND576	GND	G44	–	–	–
GND577	GND	J44	–	–	–
GND578	GND	L44	–	–	–
GND579	GND	N44	–	–	–
GND580	GND	R44	–	–	–
GND581	GND	U44	–	–	–
GND582	GND	W44	–	–	–
GND583	GND	AA44	–	–	–
GND584	GND	AC44	–	–	–
GND585	GND	AE44	–	–	–
GND586	GND	AG44	–	–	–
GND587	GND	AJ44	–	–	–
GND588	GND	AK44	–	–	–
GND589	GND	A45	–	–	–
GND590	GND	B45	–	–	–
GND591	GND	D45	–	–	–
GND592	GND	F45	–	–	–
GND593	GND	H45	–	–	–
GND594	GND	K45	–	–	–
GND595	GND	M45	–	–	–
GND596	GND	P45	–	–	–
GND597	GND	T45	–	–	–
GND598	GND	V45	–	–	–
GND599	GND	Y45	–	–	–
GND600	GND	AB45	–	–	–
GND601	GND	AD45	–	–	–
GND602	GND	AF45	–	–	–

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Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND603	GND	AH45	–	–	–
GND604	GND	AK45	–	–	–
GND605	GND	A46	–	–	–
GND606	GND	C46	–	–	–
GND607	GND	E46	–	–	–
GND608	GND	G46	–	–	–
GND609	GND	J46	–	–	–
GND610	GND	L46	–	–	–
GND611	GND	N46	–	–	–
GND612	GND	R46	–	–	–
GND613	GND	U46	–	–	–
GND614	GND	W46	–	–	–
GND615	GND	AA46	–	–	–
GND616	GND	AC46	–	–	–
GND617	GND	AE46	–	–	–
GND618	GND	AG46	–	–	–
GND619	GND	AJ46	–	–	–
GND620	GND	AK46	–	–	–
GND621	GND	A47	–	–	–
GND622	GND	B47	–	–	–
GND623	GND	D47	–	–	–
GND624	GND	F47	–	–	–
GND625	GND	H47	–	–	–
GND626	GND	K47	–	–	–
GND627	GND	M47	–	–	–
GND628	GND	P47	–	–	–
GND629	GND	T47	–	–	–
GND630	GND	V47	–	–	–
GND631	GND	Y47	–	–	–
GND632	GND	AB47	–	–	–
GND633	GND	AD47	–	–	–
GND634	GND	AF47	–	–	–
GND635	GND	AH47	–	–	–
GND636	GND	AK47	–	–	–

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Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND637	GND	A48	–	–	–
GND638	GND	C48	–	–	–
GND639	GND	E48	–	–	–
GND640	GND	G48	–	–	–
GND641	GND	J48	–	–	–
GND642	GND	L48	–	–	–
GND643	GND	N48	–	–	–
GND644	GND	R48	–	–	–
GND645	GND	U48	–	–	–
GND646	GND	W48	–	–	–
GND647	GND	AA48	–	–	–
GND648	GND	AC48	–	–	–
GND649	GND	AE48	–	–	–
GND650	GND	AG48	–	–	–
GND651	GND	AJ48	–	–	–
GND652	GND	AK48	–	–	–
GND653	GND	A49	–	–	–
GND654	GND	B49	–	–	–
GND655	GND	D49	–	–	–
GND656	GND	F49	–	–	–
GND657	GND	H49	–	–	–
GND658	GND	K49	–	–	–
GND659	GND	M49	–	–	–
GND660	GND	P49	–	–	–
GND661	GND	T49	–	–	–
GND662	GND	V49	–	–	–
GND663	GND	Y49	–	–	–
GND664	GND	AB49	–	–	–
GND665	GND	AD49	–	–	–
GND666	GND	AF49	–	–	–
GND667	GND	AH49	–	–	–
GND668	GND	AK49	–	–	–
GND669	GND	A50	–	–	–
GND670	GND	C50	–	–	–
GND671	GND	E50	–	–	–

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Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND672	GND	G50	–	–	–
GND673	GND	J50	–	–	–
GND674	GND	L50	–	–	–
GND675	GND	N50	–	–	–
GND676	GND	U50	–	–	–
GND677	GND	W50	–	–	–
GND678	GND	AA50	–	–	–
GND679	GND	AC50	–	–	–
GND680	GND	AE50	–	–	–
GND681	GND	AG50	–	–	–
GND682	GND	AJ50	–	–	–
GND683	GND	AK50	–	–	–
GND684	GND	A51	–	–	–
GND685	GND	B51	–	–	–
GND686	GND	D51	–	–	–
GND687	GND	F51	–	–	–
GND688	GND	H51	–	–	–
GND689	GND	K51	–	–	–
GND690	GND	M51	–	–	–
GND691	GND	P51	–	–	–
GND692	GND	V51	–	–	–
GND693	GND	Y51	–	–	–
GND694	GND	AB51	–	–	–
GND695	GND	AD51	–	–	–
GND696	GND	AF51	–	–	–
GND697	GND	AH51	–	–	–
GND698	GND	AK51	–	–	–
SD_GND01	Serdes core logic GND	AB5	–	–	23
SD_GND02	Serdes core logic GND	AD5	–	–	23
SD_GND03	Serdes core logic GND	AE5	–	–	23
SD_GND04	Serdes core logic GND	AF5	–	–	23
SD_GND05	Serdes core logic GND	AH5	–	–	23
SD_GND06	Serdes core logic GND	AJ5	–	–	23
SD_GND07	Serdes core logic GND	AA6	–	–	23

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Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD_GND08	Serdes core logic GND	AD6	–	–	23
SD_GND09	Serdes core logic GND	AG6	–	–	23
SD_GND10	Serdes core logic GND	AA7	–	–	23
SD_GND11	Serdes core logic GND	AB7	–	–	23
SD_GND12	Serdes core logic GND	AC7	–	–	23
SD_GND13	Serdes core logic GND	AE7	–	–	23
SD_GND14	Serdes core logic GND	AF7	–	–	23
SD_GND15	Serdes core logic GND	AG7	–	–	23
SD_GND16	Serdes core logic GND	AH7	–	–	23
SD_GND17	Serdes core logic GND	AJ7	–	–	23
SD_GND18	Serdes core logic GND	AA8	–	–	23
SD_GND19	Serdes core logic GND	AD8	–	–	23
SD_GND20	Serdes core logic GND	AG8	–	–	23
SD_GND21	Serdes core logic GND	AA9	–	–	23
SD_GND22	Serdes core logic GND	AB9	–	–	23
SD_GND23	Serdes core logic GND	AC9	–	–	23
SD_GND24	Serdes core logic GND	AE9	–	–	23
SD_GND25	Serdes core logic GND	AF9	–	–	23
SD_GND26	Serdes core logic GND	AG9	–	–	23
SD_GND27	Serdes core logic GND	AH9	–	–	23
SD_GND28	Serdes core logic GND	AJ9	–	–	23
SD_GND29	Serdes core logic GND	AA10	–	–	23
SD_GND30	Serdes core logic GND	AB10	–	–	23
SD_GND31	Serdes core logic GND	AC10	–	–	23
SD_GND32	Serdes core logic GND	AD10	–	–	23
SD_GND33	Serdes core logic GND	AG10	–	–	23
SD_GND34	Serdes core logic GND	AC11	–	–	23
SD_GND35	Serdes core logic GND	AD11	–	–	23
SD_GND36	Serdes core logic GND	AG11	–	–	23
SD_GND37	Serdes core logic GND	AB12	–	–	23
SD_GND38	Serdes core logic GND	AE12	–	–	23
SD_GND39	Serdes core logic GND	AF12	–	–	23
SD_GND40	Serdes core logic GND	AH12	–	–	23
SD_GND41	Serdes core logic GND	AJ12	–	–	23
SD_GND42	Serdes core logic GND	AC14	–	–	23

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Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD_GND43	Serdes core logic GND	AE14	–	–	23
SD_GND44	Serdes core logic GND	AF14	–	–	23
SD_GND45	Serdes core logic GND	AH14	–	–	23
SD_GND46	Serdes core logic GND	AJ14	–	–	23
SD_GND47	Serdes core logic GND	AA15	–	–	23
SD_GND48	Serdes core logic GND	AB15	–	–	23
SD_GND49	Serdes core logic GND	AD15	–	–	23
SD_GND50	Serdes core logic GND	AG15	–	–	23
SD_GND51	Serdes core logic GND	AA16	–	–	23
SD_GND52	Serdes core logic GND	AC16	–	–	23
SD_GND53	Serdes core logic GND	AD16	–	–	23
SD_GND54	Serdes core logic GND	AG16	–	–	23
SD_GND55	Serdes core logic GND	AB17	–	–	23
SD_GND56	Serdes core logic GND	AC17	–	–	23
SD_GND57	Serdes core logic GND	AE17	–	–	23
SD_GND58	Serdes core logic GND	AF17	–	–	23
SD_GND59	Serdes core logic GND	AG17	–	–	23
SD_GND60	Serdes core logic GND	AH17	–	–	23
SD_GND61	Serdes core logic GND	AJ17	–	–	23
SD_GND62	Serdes core logic GND	AB18	–	–	23
SD_GND63	Serdes core logic GND	AD18	–	–	23
SD_GND64	Serdes core logic GND	AG18	–	–	23
SD_GND65	Serdes core logic GND	AB19	–	–	23
SD_GND66	Serdes core logic GND	AD19	–	–	23
SD_GND67	Serdes core logic GND	AG19	–	–	23
SD_GND68	Serdes core logic GND	AC20	–	–	23
SD_GND69	Serdes core logic GND	AE20	–	–	23
SD_GND70	Serdes core logic GND	AF20	–	–	23
SD_GND71	Serdes core logic GND	AH20	–	–	23
SD_GND72	Serdes core logic GND	AJ20	–	–	23
D1_VPP01	DDR4 activating power supply	B46			
D1_VPP02	DDR4 activating power supply	AH46			
D1_VPP03	DDR4 activating power supply	C47			
D1_VPP04	DDR4 activating power supply	AJ47			

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Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_VPP05	DDR4 activating power supply	B48			
D1_VPP06	DDR4 activating power supply	AH48			
D1_VPP07	DDR4 activating power supply	C49			
D1_VPP08	DDR4 activating power supply	AJ49			
D1_VPP09	DDR4 activating power supply	B50			
D1_VPP10	DDR4 activating power supply	AH50			
D1_VPP11	DDR4 activating power supply	C51			
D1_VPP12	DDR4 activating power supply	AJ51			
D1_VTT01	DDR4 termination	R50			
D1_VTT02	DDR4 termination	T50			
D1_VTT03	DDR4 termination	R51			
D1_VTT04	DDR4 termination	T51			
G1VDD01	DDR supply	B22			
G1VDD02	DDR supply	D22			
G1VDD03	DDR supply	F22			
G1VDD04	DDR supply	H22			
G1VDD05	DDR supply	K22			
G1VDD06	DDR supply	AB22			
G1VDD07	DDR supply	AD22			
G1VDD08	DDR supply	AF22			
G1VDD09	DDR supply	AH22			
G1VDD10	DDR supply	C23			
G1VDD11	DDR supply	E23			
G1VDD12	DDR supply	G23			
G1VDD13	DDR supply	J23			
G1VDD14	DDR supply	L23			
G1VDD15	DDR supply	AC23			
G1VDD16	DDR supply	AE23			
G1VDD17	DDR supply	AG23			
G1VDD18	DDR supply	AJ23			
G1VDD19	DDR supply	B24			
G1VDD20	DDR supply	D24			
G1VDD21	DDR supply	F24			
G1VDD22	DDR supply	H24			
G1VDD23	DDR supply	K24			

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Signal	Signal description	Package pin number	Pin type	Power supply	Notes
G1VDD24	DDR supply	M24			
G1VDD25	DDR supply	P24			
G1VDD26	DDR supply	T24			
G1VDD27	DDR supply	V24			
G1VDD28	DDR supply	Y24			
G1VDD29	DDR supply	C25			
G1VDD30	DDR supply	E25			
G1VDD31	DDR supply	G25			
G1VDD32	DDR supply	J25			
G1VDD33	DDR supply	L25			
G1VDD34	DDR supply	N25			
G1VDD35	DDR supply	R25			
G1VDD36	DDR supply	U25			
G1VDD37	DDR supply	W25			
G1VDD38	DDR supply	AA25			
G1VDD39	DDR supply	AC25			
G1VDD40	DDR supply	AE25			
G1VDD41	DDR supply	AG25			
G1VDD42	DDR supply	AJ25			
G1VDD43	DDR supply	B26			
G1VDD44	DDR supply	D26			
G1VDD45	DDR supply	V26			
G1VDD46	DDR supply	Y26			
G1VDD47	DDR supply	AB26			
G1VDD48	DDR supply	AD26			
G1VDD49	DDR supply	AF26			
G1VDD50	DDR supply	U27			
G1VDD51	DDR supply	W27			
G1VDD52	DDR supply	AA27			
G1VDD53	DDR supply	AC27			
G1VDD54	DDR supply	AE27			
G1VDD55	DDR supply	AG27			
G1VDD56	DDR supply	B28			
G1VDD57	DDR supply	D28			

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Signal	Signal description	Package pin number	Pin type	Power supply	Notes
G1VDD58	DDR supply	F28			
G1VDD59	DDR supply	G28			
G1VDD60	DDR supply	H28			
G1VDD61	DDR supply	K28			
G1VDD62	DDR supply	P28			
G1VDD63	DDR supply	V28			
G1VDD64	DDR supply	Y28			
G1VDD65	DDR supply	AA28			
G1VDD66	DDR supply	AB28			
G1VDD67	DDR supply	AD28			
G1VDD68	DDR supply	AF28			
G1VDD69	DDR supply	AH28			
G1VDD70	DDR supply	M22			
G1VDD71	DDR supply	N22			
G1VDD72	DDR supply	P22			
G1VDD73	DDR supply	R22			
G1VDD74	DDR supply	T22			
G1VDD75	DDR supply	U22			
G1VDD76	DDR supply	V22			
G1VDD77	DDR supply	W22			
G1VDD78	DDR supply	C27			
G1VDD79	DDR supply	E27			
G1VDD80	DDR supply	G27			
G1VDD81	DDR supply	J27			
G1VDD82	DDR supply	L27			
G1VDD83	DDR supply	N27			
G1VDD84	DDR supply	R27			
G1VDD85	DDR supply	V27			
G1VDD86	DDR supply	Y27			
G1VDD87	DDR supply	AB27			
G1VDD88	DDR supply	AD27			
G1VDD89	DDR supply	AF27			
G1VDD90	DDR supply	AH27			
G1VDD91	DDR supply	AJ27			
D1_VDD001	DDR4 module power supply	C29			

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Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_VDD002	DDR4 module power supply	E29			
D1_VDD003	DDR4 module power supply	G29			
D1_VDD004	DDR4 module power supply	J29			
D1_VDD005	DDR4 module power supply	L29			
D1_VDD006	DDR4 module power supply	N29			
D1_VDD007	DDR4 module power supply	R29			
D1_VDD008	DDR4 module power supply	U29			
D1_VDD009	DDR4 module power supply	W29			
D1_VDD010	DDR4 module power supply	AA29			
D1_VDD011	DDR4 module power supply	AC29			
D1_VDD012	DDR4 module power supply	AE29			
D1_VDD013	DDR4 module power supply	AG29			
D1_VDD014	DDR4 module power supply	AJ29			
D1_VDD015	DDR4 module power supply	B30			
D1_VDD016	DDR4 module power supply	D30			
D1_VDD017	DDR4 module power supply	F30			
D1_VDD018	DDR4 module power supply	H30			
D1_VDD019	DDR4 module power supply	K30			
D1_VDD020	DDR4 module power supply	M30			
D1_VDD021	DDR4 module power supply	P30			
D1_VDD022	DDR4 module power supply	V30			
D1_VDD023	DDR4 module power supply	Y30			
D1_VDD024	DDR4 module power supply	AB30			
D1_VDD025	DDR4 module power supply	AD30			
D1_VDD026	DDR4 module power supply	AF30			
D1_VDD027	DDR4 module power supply	AH30			
D1_VDD028	DDR4 module power supply	C31			
D1_VDD029	DDR4 module power supply	E31			
D1_VDD030	DDR4 module power supply	G31			
D1_VDD031	DDR4 module power supply	J31			
D1_VDD032	DDR4 module power supply	L31			
D1_VDD033	DDR4 module power supply	N31			
D1_VDD034	DDR4 module power supply	R31			
D1_VDD035	DDR4 module power supply	W31			

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Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_VDD036	DDR4 module power supply	AA31			
D1_VDD037	DDR4 module power supply	AC31			
D1_VDD038	DDR4 module power supply	AE31			
D1_VDD039	DDR4 module power supply	AG31			
D1_VDD040	DDR4 module power supply	AJ31			
D1_VDD041	DDR4 module power supply	B32			
D1_VDD042	DDR4 module power supply	D32			
D1_VDD043	DDR4 module power supply	AH32			
D1_VDD044	DDR4 module power supply	C33			
D1_VDD045	DDR4 module power supply	E33			
D1_VDD046	DDR4 module power supply	G33			
D1_VDD047	DDR4 module power supply	J33			
D1_VDD048	DDR4 module power supply	L33			
D1_VDD049	DDR4 module power supply	N33			
D1_VDD050	DDR4 module power supply	R33			
D1_VDD051	DDR4 module power supply	W33			
D1_VDD052	DDR4 module power supply	AA33			
D1_VDD053	DDR4 module power supply	AC33			
D1_VDD054	DDR4 module power supply	AE33			
D1_VDD055	DDR4 module power supply	AG33			
D1_VDD056	DDR4 module power supply	AJ33			
D1_VDD057	DDR4 module power supply	B34			
D1_VDD058	DDR4 module power supply	D34			
D1_VDD059	DDR4 module power supply	AH34			
D1_VDD060	DDR4 module power supply	C35			
D1_VDD061	DDR4 module power supply	E35			
D1_VDD062	DDR4 module power supply	G35			
D1_VDD063	DDR4 module power supply	J35			
D1_VDD064	DDR4 module power supply	L35			
D1_VDD065	DDR4 module power supply	N35			
D1_VDD066	DDR4 module power supply	R35			
D1_VDD067	DDR4 module power supply	W35			
D1_VDD068	DDR4 module power supply	AA35			
D1_VDD069	DDR4 module power supply	AC35			
D1_VDD070	DDR4 module power supply	AE35			

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Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_VDD071	DDR4 module power supply	AG35			
D1_VDD072	DDR4 module power supply	AJ35			
D1_VDD073	DDR4 module power supply	B36			
D1_VDD074	DDR4 module power supply	D36			
D1_VDD075	DDR4 module power supply	AH36			
D1_VDD076	DDR4 module power supply	C37			
D1_VDD077	DDR4 module power supply	E37			
D1_VDD078	DDR4 module power supply	G37			
D1_VDD079	DDR4 module power supply	J37			
D1_VDD080	DDR4 module power supply	L37			
D1_VDD081	DDR4 module power supply	N37			
D1_VDD082	DDR4 module power supply	R37			
D1_VDD083	DDR4 module power supply	W37			
D1_VDD084	DDR4 module power supply	AA37			
D1_VDD085	DDR4 module power supply	AC37			
D1_VDD086	DDR4 module power supply	AE37			
D1_VDD087	DDR4 module power supply	AG37			
D1_VDD088	DDR4 module power supply	AJ37			
D1_VDD089	DDR4 module power supply	B38			
D1_VDD090	DDR4 module power supply	D38			
D1_VDD091	DDR4 module power supply	AH38			
D1_VDD092	DDR4 module power supply	C39			
D1_VDD093	DDR4 module power supply	E39			
D1_VDD094	DDR4 module power supply	G39			
D1_VDD095	DDR4 module power supply	J39			
D1_VDD096	DDR4 module power supply	L39			
D1_VDD097	DDR4 module power supply	N39			
D1_VDD098	DDR4 module power supply	R39			
D1_VDD099	DDR4 module power supply	U39			
D1_VDD100	DDR4 module power supply	W39			
D1_VDD101	DDR4 module power supply	AA39			
D1_VDD102	DDR4 module power supply	AC39			
D1_VDD103	DDR4 module power supply	AE39			
D1_VDD104	DDR4 module power supply	AG39			

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Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_VDD105	DDR4 module power supply	AJ39			
D1_VDD106	DDR4 module power supply	B40			
D1_VDD107	DDR4 module power supply	D40			
D1_VDD108	DDR4 module power supply	AH40			
D1_VDD109	DDR4 module power supply	C41			
D1_VDD110	DDR4 module power supply	E41			
D1_VDD111	DDR4 module power supply	G41			
D1_VDD112	DDR4 module power supply	J41			
D1_VDD113	DDR4 module power supply	L41			
D1_VDD114	DDR4 module power supply	N41			
D1_VDD115	DDR4 module power supply	R41			
D1_VDD116	DDR4 module power supply	U41			
D1_VDD117	DDR4 module power supply	W41			
D1_VDD118	DDR4 module power supply	AA41			
D1_VDD119	DDR4 module power supply	AC41			
D1_VDD120	DDR4 module power supply	AE41			
D1_VDD121	DDR4 module power supply	AG41			
D1_VDD122	DDR4 module power supply	AJ41			
D1_VDD123	DDR4 module power supply	B42			
D1_VDD124	DDR4 module power supply	D42			
D1_VDD125	DDR4 module power supply	AH42			
D1_VDD126	DDR4 module power supply	C43			
D1_VDD127	DDR4 module power supply	E43			
D1_VDD128	DDR4 module power supply	G43			
D1_VDD129	DDR4 module power supply	J43			
D1_VDD130	DDR4 module power supply	L43			
D1_VDD131	DDR4 module power supply	N43			
D1_VDD132	DDR4 module power supply	R43			
D1_VDD133	DDR4 module power supply	U43			
D1_VDD134	DDR4 module power supply	W43			
D1_VDD135	DDR4 module power supply	AA43			
D1_VDD136	DDR4 module power supply	AC43			
D1_VDD137	DDR4 module power supply	AE43			
D1_VDD138	DDR4 module power supply	AG43			
D1_VDD139	DDR4 module power supply	AJ43			

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Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_VDD140	DDR4 module power supply	B44			
D1_VDD141	DDR4 module power supply	D44			
D1_VDD142	DDR4 module power supply	AH44			
D1_VDD143	DDR4 module power supply	C45			
D1_VDD144	DDR4 module power supply	E45			
D1_VDD145	DDR4 module power supply	G45			
D1_VDD146	DDR4 module power supply	J45			
D1_VDD147	DDR4 module power supply	L45			
D1_VDD148	DDR4 module power supply	N45			
D1_VDD149	DDR4 module power supply	R45			
D1_VDD150	DDR4 module power supply	U45			
D1_VDD151	DDR4 module power supply	W45			
D1_VDD152	DDR4 module power supply	AA45			
D1_VDD153	DDR4 module power supply	AC45			
D1_VDD154	DDR4 module power supply	AE45			
D1_VDD155	DDR4 module power supply	AG45			
D1_VDD156	DDR4 module power supply	AJ45			
D1_VDD157	DDR4 module power supply	D46			
D1_VDD158	DDR4 module power supply	E47			
D1_VDD159	DDR4 module power supply	G47			
D1_VDD160	DDR4 module power supply	J47			
D1_VDD161	DDR4 module power supply	L47			
D1_VDD162	DDR4 module power supply	N47			
D1_VDD163	DDR4 module power supply	R47			
D1_VDD164	DDR4 module power supply	U47			
D1_VDD165	DDR4 module power supply	W47			
D1_VDD166	DDR4 module power supply	AA47			
D1_VDD167	DDR4 module power supply	AC47			
D1_VDD168	DDR4 module power supply	AE47			
D1_VDD169	DDR4 module power supply	AG47			
D1_VDD170	DDR4 module power supply	D48			
D1_VDD171	DDR4 module power supply	E49			
D1_VDD172	DDR4 module power supply	G49			
D1_VDD173	DDR4 module power supply	J49			

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Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_VDD174	DDR4 module power supply	L49			
D1_VDD175	DDR4 module power supply	N49			
D1_VDD176	DDR4 module power supply	R49			
D1_VDD177	DDR4 module power supply	U49			
D1_VDD178	DDR4 module power supply	W49			
D1_VDD179	DDR4 module power supply	AA49			
D1_VDD180	DDR4 module power supply	AC49			
D1_VDD181	DDR4 module power supply	AE49			
D1_VDD182	DDR4 module power supply	AG49			
D1_VDD183	DDR4 module power supply	D50			
D1_VDD184	DDR4 module power supply	F50			
D1_VDD185	DDR4 module power supply	H50			
D1_VDD186	DDR4 module power supply	K50			
D1_VDD187	DDR4 module power supply	M50			
D1_VDD188	DDR4 module power supply	P50			
D1_VDD189	DDR4 module power supply	V50			
D1_VDD190	DDR4 module power supply	Y50			
D1_VDD191	DDR4 module power supply	AB50			
D1_VDD192	DDR4 module power supply	AD50			
D1_VDD193	DDR4 module power supply	AF50			
D1_VDD194	DDR4 module power supply	E51			
D1_VDD195	DDR4 module power supply	G51			
D1_VDD196	DDR4 module power supply	J51			
D1_VDD197	DDR4 module power supply	L51			
D1_VDD198	DDR4 module power supply	N51			
D1_VDD199	DDR4 module power supply	U51			
D1_VDD200	DDR4 module power supply	W51			
D1_VDD201	DDR4 module power supply	AA51			
D1_VDD202	DDR4 module power supply	AC51			
D1_VDD203	DDR4 module power supply	AE51			
D1_VDD204	DDR4 module power supply	AG51			
VDD01	Supply for cores and platform	L14			
VDD02	Supply for cores and platform	L16			
VDD03	Supply for cores and platform	L18			
VDD04	Supply for cores and platform	L20			

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Signal	Signal description	Package pin number	Pin type	Power supply	Notes
VDD05	Supply for cores and platform	M11			
VDD06	Supply for cores and platform	M13			
VDD07	Supply for cores and platform	M15			
VDD08	Supply for cores and platform	M17			
VDD09	Supply for cores and platform	M19			
VDD10	Supply for cores and platform	N10			
VDD11	Supply for cores and platform	N12			
VDD12	Supply for cores and platform	N14			
VDD13	Supply for cores and platform	N16			
VDD14	Supply for cores and platform	N18			
VDD15	Supply for cores and platform	P9			
VDD16	Supply for cores and platform	P11			
VDD17	Supply for cores and platform	P13			
VDD18	Supply for cores and platform	P15			
VDD19	Supply for cores and platform	P17			
VDD20	Supply for cores and platform	P19			
VDD21	Supply for cores and platform	R10			
VDD22	Supply for cores and platform	R12			
VDD23	Supply for cores and platform	R14			
VDD24	Supply for cores and platform	R16			
VDD25	Supply for cores and platform	R18			
VDD26	Supply for cores and platform	T9			
VDD27	Supply for cores and platform	T11			
VDD28	Supply for cores and platform	T13			
VDD29	Supply for cores and platform	T15			
VDD30	Supply for cores and platform	T17			
VDD31	Supply for cores and platform	T19			
VDD32	Supply for cores and platform	U10			
VDD33	Supply for cores and platform	U12			
VDD34	Supply for cores and platform	U14			
VDD35	Supply for cores and platform	U16			
VDD36	Supply for cores and platform	U18			
VDD37	Supply for cores and platform	V9			
VDD38	Supply for cores and platform	V11			

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Signal	Signal description	Package pin number	Pin type	Power supply	Notes
VDD39	Supply for cores and platform	V13			
VDD40	Supply for cores and platform	V15			
VDD41	Supply for cores and platform	V17			
VDD42	Supply for cores and platform	V19			
VDD43	Supply for cores and platform	W10			
VDD44	Supply for cores and platform	W12			
VDD45	Supply for cores and platform	W14			
VDD46	Supply for cores and platform	W16			
VDD47	Supply for cores and platform	W18			
VDD48	Supply for cores and platform	W20			
VDD49	Supply for cores and platform	Y11			
VDD50	Supply for cores and platform	Y17			
VDD51	Supply for cores and platform	Y19			
SENSEGND	GND Sense pin	H20	–	–	–
OVDD1	General I/O supply	K14	–	OVDD	–
OVDD2	General I/O supply	K15	–	OVDD	–
OVDD3	General I/O supply	K16	–	OVDD	–
OVDD4	General I/O supply	K17	–	OVDD	–
OVDD5	General I/O supply	K18	–	OVDD	–
OVDD6	General I/O supply	T7	–	OVDD	–
DVDD1	UART/I2C supply - switchable	P7	–	DVDD	–
DVDD2	UART/I2C supply - switchable	R7	–	DVDD	–
EVDD	eSDHC supply - switchable	T6	–	EVDD	–
LVDD1	Ethernet controller 1 & 2 supply	U7	–	LVDD	–
LVDD2	Ethernet controller 1 & 2 supply	V7	–	LVDD	–
LVDD3	Ethernet controller 1 & 2 supply	W7	–	LVDD	–
TVDD	1.2 V / LVDD supply for MDIO interface for 10G Fman (EC2)	Y6	–	TVDD	–
SVDD1	SerDes1 core logic supply	Y10	–	SVDD	–
SVDD2	SerDes1 core logic supply	Y13	–	SVDD	–
SVDD3	SerDes1 core logic supply	Y14	–	SVDD	–
SVDD4	SerDes1 core logic supply	Y15	–	SVDD	–
SVDD5	SerDes1 core logic supply	Y16	–	SVDD	–
SVDD6	SerDes1 core logic supply	AA17	–	SVDD	–
SVDD7	SerDes1 core logic supply	AA18	–	SVDD	–

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Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SVDD8	SerDes1 core logic supply	AA19	–	SVDD	–
XVDD1	SerDes1 transceiver supply	AD7	–	XVDD	–
XVDD2	SerDes1 transceiver supply	AD9	–	XVDD	–
XVDD3	SerDes1 transceiver supply	AD12	–	XVDD	–
XVDD4	SerDes1 transceiver supply	AD14	–	XVDD	–
XVDD5	SerDes1 transceiver supply	AD17	–	XVDD	–
XVDD6	SerDes1 transceiver supply	AD20	–	XVDD	–
FA_VL	Reserved	AC21	–	FA_VL	15
PROG_MTR	Reserved	G13	–	PROG_MTR	15
TA_PROG_SFP	SFP Fuse Programming Override supply	H13	–	TA_PROG_SFP	–
TH_VDD	Thermal Monitor Unit supply	H8	–	TH_VDD	–
TA_BB_VDD	Battery Backed Security Monitor supply	H12	–	TA_BB_VDD	–
AVDD_CGA1	CPU Cluster Group A PLL1 supply	J11	–	AVDD_CGA1	–
AVDD_CGA2	CPU Cluster Group A PLL2 supply	J10	–	AVDD_CGA2	–
AVDD_PLAT	Platform PLL supply	J9	–	AVDD_PLAT	–
AVDD_D1	DDR1 PLL supply	T21	–	AVDD_D1	–
AVDD_SD1_PLL1	SerDes1 PLL 1 supply	AB11	–	AVDD_SD1_PLL1	–
AVDD_SD1_PLL2	SerDes1 PLL 2 supply	AC6	–	AVDD_SD1_PLL2	–
AVDD_SD2_PLL1	SerDes2 PLL 1 supply	AC15	–	AVDD_SD2_PLL1	–
AVDD_SD2_PLL2	SerDes2 PLL 2 supply	AB16	–	AVDD_SD2_PLL2	–
SENSEVDD	Vdd Sense pin	H19	–	SENSEVDD	–
USB_HVDD1	3.3 V High Supply	L8	–	USB_HVDD	–
USB_HVDD2	3.3 V High Supply	M8	–	USB_HVDD	–
USB_SDVDD1	1.0 V Analog and digital HS supply	N7	–	USB_SDVDD	–
USB_SDVDD2	1.0 V Analog and digital HS supply	N8	–	USB_SDVDD	–
USB_SVDD1	1.0 V Analog and digital SS supply	L7	–	USB_SVDD	–
USB_SVDD2	1.0 V Analog and digital SS supply	M7	–	USB_SVDD	–

Notes:

1. Functionally, this pin is an output or an input, but structurally it is an I/O because it either sample configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.
2. This output is actively driven during reset rather than being tri-stated during reset.
3. MDIC[0] is grounded through a 162 Ω precision 1% resistor and MDIC[1] is connected to GV_{DD} through a 162 Ω precision 1% resistor. For either full or half driver strength calibration of DDR IOs, use the same MDIC resistor value of 162 Ω. The memory controller register setting can be used to determine automatic calibration is done to full or half drive strength. These pins are used for automatic calibration of the DDR4 IOs.

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4. This pin is a reset configuration pin. It has a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the processor is in its reset state. This pull-up is designed such that it can be overpowered by an external 4.7 kΩ resistor. However, if the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, a pull-up or active driver is needed.
5. Pin must **NOT** be pulled down during power-on reset. This pin may be pulled up, driven high, or if there are any externally connected devices, left in tristate. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.
6. Recommend that a weak pull-up resistor (2-10 kΩ) be placed on this pin to the respective power supply.
7. This pin is an open-drain signal.
8. Recommend that a weak pull-up resistor (1 kΩ) be placed on this pin to the respective power supply.
9. This pin has a weak (~20 kΩ) internal pull-up P-FET that is always enabled.
10. These are test signals for factory use only and must be pulled up (100Ω to 1-kΩ) to the respective power supply for normal operation.
11. This pin requires a 200Ω ± 1% pull-up to respective power-supply.
12. Do not connect. These pins should be left floating.
13.
14. This pin requires an external 1-kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.
15. These pins must be pulled to ground (GND).
16. This pin requires a 698Ω ± 1% pull-up to respective power-supply.
17. These pins should be tied to ground if the diode is not utilized for temperature monitoring.
18. This pin should be grounded through a 200Ω +/-1% 100ppm/°C precision resistor.
19. This pin must be pulled to OVDD through a 100-Ω to 1kΩ resistor for a four core QLS1046A device and tied to ground for a two core QLS1026A device.
20. In normal operation, this pin must be pulled high to OVDD with 4.7 kΩ.
21. DIFF_SYSCLK and DIFF_SYSCLK_B is tied to cfg_eng_use0, the configuration is described in section "Reset configuration word (RCW)" of *QorIQ QLS1046A Reference Manual*.
22. This pin should be connected to ground through 2-10 kΩ resistor when not used.
23. SD_GND must be directly connected to GND.
24. This pin must be pulled down to GND with a pull down resistor of value 1 KΩ
25. This pin will not be tested using JTAG Boundary scan operation.
26. For proper clock selection, terminate cfg_eng_use0 with a pull up or pull down of 4.7 kΩ to ensure that the signal will have a valid state as soon as the IO voltage reach its operating condition.

Warning

See **"Connection Recommendations"** for additional details on properly connecting these pins for specific applications.

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3 ELECTRICAL CHARACTERISTICS

This section describes the DC and AC electrical specifications for the chip. The chip is currently targeted to these specifications, some of which are independent of the I/O cell but are included for a more complete reference. These are not purely I/O buffer design specifications.

3.1 Overall DC electrical characteristics

This section describes the ratings, conditions, and other characteristics.

3.1.1 Absolute maximum ratings

This table provides the absolute maximum ratings.

Table 2. Absolute maximum ratings (1)(5)

Characteristic	Symbol	Max Value	Unit	Notes
Core and platform supply voltage	V_{DD}	-0.3 to 1.08	V	4
PLL supply voltage (core PLL, platform, DDR)	AV_{DD}_CGA1 AV_{DD}_CGA2 AV_{DD}_D1 AV_{DD}_PLAT	-0.3 to 1.98	V	–
PLL supply voltage (SerDes, filtered from X*n*V_{DD})	AVDD_SD*n*_PLL1 AVDD_SD*n*_PLL2	-0.3 to 1.48	V	–
SFP Fuse Programming	TA_PROG_SFP	-0.3 to 1.98	V	–
Thermal Unit Monitor supply	TH_V_{DD}	-0.3 to 1.98	V	–
Battery Backed Security Monitor supply	TA_BB_V_{DD}	-0.3 to 1.08	V	–
IFC, SPI, IRQ[0:2], Tamper Detect, System Control, SYSCLK, DDRCLK, RTC, EVT[0:4], DFT, JTAG, DIFF_SYSCLK, CLK_OUT, QSPI, FTM[5:7], eSDHC_DAT[4:7], eSDHC_CMD/DAT0_DIR, eSDHC_DAT123_DIR, eSDHC_SYNC_IN/OUT, SDHC_VS	OV_{DD}	-0.3 to 1.98	V	–
DUART, I2C, IRQ[3:10], USB2/3_PWRFAULT, USB2/3_DRVVBUS, EVT_B[5:8], LPUART[1:2], LPUART4, FTM3_CH[1:7], FTM4_CH[1:5], FTM8, eSDHC_CD/WP	DV_{DD}	-0.3 to 3.63 -0.3 to 1.98	V	–
eSDHC_DAT[0:3], eSDHC_CMD, eSDHC_CLK, FTM4_CH[6:7], LPUART[3:6]	EV_{DD}	-0.3 to 3.63 -0.3 to 1.98	V	–
DDR4 DRAM I/O voltage	$G1V_{DD}$	-0.3 to 1.32	V	–
DDR4 termination	D1_V_{TT}	$G1V_{DD}$/2	V	
DDR4 activating power supply	D1_V_{PP}	–0.4 to 3.0	V	
DDR4 module power supply	D1_V_{DD}	–0.4 to 1.5	V	
Main power supply for internal circuitry of SerDes and pad power supply for SerDes receivers	SV_{DD}	-0.3 to 1.08	V	–
Pad power supply for SerDes transmitter	XV_{DD}	-0.3 to 1.48	V	–
Ethernet interface, Ethernet management interface 1 (EMI1), 1588, IRQ11, FTM1, FTM2,	LV_{DD}	-0.3 to 2.75 -0.3 to 1.98	V	–

Characteristic	Symbol	Max Value	Unit	Notes
Ethernet management interface 2 (EMI2), GPIO2	TV_{DD}	-0.3 to 2.75 -0.3 to 1.98 -0.3 to 1.32	V	–
USB PHY Transceiver supply voltage	USB_HV_{DD}	-0.3 to 3.63	V	-
	USB_SDV_{DD}	-0.3 to 1.08	V	3
	USB_SV_{DD}	-0.3 to 1.08	V	2
Storage temperature range	T_{STG}	-55 to 150	°C	--

Notes:

1. Functional operating conditions are given in Table 4. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. Analog and Digital SS supply for USBPHY.
3. Analog and Digital HS supply for USBPHY.
4. Supply voltage specified at the voltage sense pin. Voltage input pins should be regulated to provide specified voltage at the sense pin.
5. Exposing device to Absolute Maximum Ratings conditions for long periods of time may affect reliability or cause permanent damage.

This table provides the absolute maximum ratings for input signal voltage levels.

Table 3. Absolute maximum ratings for input signal voltage levels (1)

Interface Input signals	Symbol	Max DC V_input range	Max undershoot andovershoot voltage range	Unit	Notes
DDR4 DRAM signals	$G1V_{IN}$	GND to ($G1V_{DD}$ x 1.05)	-0.3 to ($G1V_{DD}$ x 1.1)	V	2, 3, 4
Ethernet interface, Ethernet management interface 1 (EMI1), 1588, IRQ11, FTM1, FTM2	LV_{IN}	GND to (LV_{DD} x 1.1)	-0.3 to (LV_{DD} x 1.15)	V	2, 3
IFC, SPI, IRQ[0:2], Tamper Detect, System Control, SYSCLK, DDRCLK, RTC, EVT[0:4], DFT, JTAG, DIFF_SYSCLK, CLK_OUT, QSPI, FTM[5:7], eSDHC_DAT[4:7], eSDHC_CMD/DAT0_DIR, eSDHC_DAT123_DIR, eSDHC_SYNC_IN/OUT, SDHC_VS	OV_{IN}	GND to (OV_{DD} x 1.1)	-0.3 to (OV_{DD} x 1.15)	V	2, 3
DUART, I2C, IRQ[3:10], USB2/3_PWRFAULT, USB2/3_DRVVBUS, EVT_B[5:8], LPUART[1:2], LPUART4, FTM3_CH[1:7], FTM4_CH[1:5], FTM8, eSDHC_CD/WP	DV_{IN}	GND to (DV_{DD} x 1.1)	-0.3 to (DV_{DD} x 1.15)		
eSDHC_DAT[0:3], eSDHC_CMD, eSDHC_CLK, FTM4_CH[6:7], LPUART[3:6]	EV_{IN}	GND to (EV_{DD} x 1.1)	-0.3 to (EV_{DD} x 1.15)	V	2, 3
Main power supply for internal circuitry of SerDes	SnV_{IN}	GND to (SV_{DD} x 1.05)	-0.3 to (SnV_{DD} x 1.1)	V	2, 3
Ethernet management interface 2 (EMI2), GPIO2	TV_{IN}	GND to (TV_{DD} x 1.05)	-0.3 to (TV_{DD} x 1.15)	V	2, 3
USB PHY Transceiver signals	USB_HV_{IN}	GND to (USB_HV_{DD} x	-0.3 to (USB_HV_{DD} x	V	2, 3

	USB_SV_{IN}	GND to (USB_SV_{DD} x 1.1)	-0.3 to (USB_SV_{DD} x	V	2, 3

Notes:

1. Functional operating conditions are given in Table 4. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** The input voltage level of the signals must not exceed corresponding Max DC V_input range. For example DDR4 must not exceed 5% of $G1V_{DD}$.
3. **Caution:** (S, G, L, O, D, E, T) VIN, USB_HVIN, USB_SVIN may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 8.
4. Typical DDR interface uses ODT enabled mode. For tests purposes with ODT off mode, simulation should be done first so as to make sure that the overshoot signal level at the input pin does not exceed GVDD by more than 10%. The Overshoot/ Undershoot period should comply with JEDEC standards.

3.1.2 Recommended operating conditions

This table provides the recommended operating conditions for this chip.

NOTE
The values shown are the recommended operating conditions and proper device operation outside these conditions is not guaranteed.

Table 4. Recommended operating conditions

Characteristic	Symbol	Recommended value	Unit	Notes
Core and platform supply voltage	V_{DD}	1.0 V ± 30 mV	V	3, 4, 5, 8
0.9 V core and platform supply voltage				
PLL supply voltage (core PLL, platform, DDR)	AV_{DD}_CGA1	1.8 V ± 90 mV	V	9
	AV_{DD}_CGA2			
	AV_{DD}_D1			
	AV_{DD}_PLAT			
PLL supply voltage (SerDes, filtered from X*n*V_{DD})	AV_{DD}_SD1_PLL1 AV_{DD}_SD1_PLL2	1.35 V ± 67 mV	V	–
	AV_{DD}_SD2_PLL1 AV_{DD}_SD2_PLL2			
SFP fuse programming	TA_PROG_SFP	1.8 V ± 90 mV	V	2
Thermal monitor unit supply	TH_V_{DD}	1.8 V ± 90 mV	V	–
Battery Backed Security Monitor supply	TA_BB_V_{DD}	1.0 V ± 30 mV	V	8
		0.9 V ± 30 mV		
IFC, IRQ[0:2], Tamper Detect, System Control, SYSCLK, DDRCLK, RTC, EVT[0:4], DFT, JTAG, DIFF_SYSCLK, CLK_OUT, QSPI, FTM[5:7], SPI, SDHC_DAT[4:7], SDHC_CMD_DIR, SDHC_DAT0_DIR, SDHC_DAT123_DIR, SDHC_SYNC_IN/OUT, SDHC_VS	OV_{DD}	1.8 V ± 90 mV	V	–
DUART, I2C, IRQ[3:10], USB2/3_PWRFAULT, USB2/3_DRVVBUS, EVT_B[5:8], LPUART[1:2], LPUART4, FTM3_CH[1:7], FTM4_CH[1:5], FTM8, SDHC_CD/WP	DV_{DD}	3.3 V ± 165 mV 1.8 V ± 90 mV	V	–
SDHC_DAT[0:3], SDHC_CMD, SDHC_CLK, FTM4_CH[6:7], LPUART3, LPUART5, LPUART6	EV_{DD}	3.3 V ±165 mV 1.8 V ± 90 mV	V	–
DDR4 DRAM I/O voltage	$G1V_{DD}$	1.2 V ± 60 mV	V	–
DDR4 termination	D1_V_{TT}	$G1V_{DD}$/2 ± 1%	V	10
DDR4 activating power supply	D1_V_{PP}	2.5V ± 125 mV	V	11
DDR4 module power supply	D1_V_{DD}	1.2 ± 60 mV	V	

Characteristic		Symbol	Recommended value	Unit	Notes
Main power supply for internal circuitry of SerDes and pad power supply for SerDes receivers		SV_{DD}	1.0 V ± 50 mV	V	–
Pad power supply for SerDes transmitters		XV_{DD}	1.35 V ± 67 mV	V	–
Ethernet interface 1/2, Ethernet management interface 1 (EMI1), 1588, IRQ11, FTM1, FTM2		LV_{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	1
Ethernet management interface 2 (EMI2), GPIO2		TV_{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV 1.2V ± 60 mV	V	
USB PHY 3.3 V high supply voltage		USB_HV_{DD}	3.3 V ± 165 mV	V	
USB PHY analog and digital HS supply		USB_SDV_{DD}	1.0 V ± 50 mV	V	7, 8
USB PHY analog and digital SS supply		USB_SV_{DD}	1.0 V ± 50 mV	V	6, 8
Input voltage	DDR4 DRAM signals	$G1V_{IN}$	GND to $G1V_{DD}$	V	–
	Ethernet interface, Ethernet management interface 1 (EMI1), 1588, IRQ11, FTM1, FTM2	LV_{IN}	GND to LV_{DD}	V	–
	IFC, SPI, IRQ[0:2], Tamper Detect, System Control, SYSCLK, DDRCLK, RTC, EVT[0:4], DFT, JTAG, DIFF_SYSCLK, CLK_OUT, QSPI, FTM[5:7], SDHC_DAT[4:7], SDHC_CMD_DIR/ DAT0_DIR, SDHC_DAT123_DIR, SDHC_SYNC_IN/OUT, SDHC_VS	OV_{IN}	GND to OV_{DD}	V	–
	DUART, I2C, IRQ[3:10], USB2/3_PWRFAULT, USB2/3_DRVVBUS, EVT_B[5:8], LPUART[1:2], LPUART4, FTM3_CH[1:7], FTM4_CH[1:5], FTM8, SDHC_CD/WP	DV_{IN}	GND to DV_{DD}	V	–
	SDHC_DAT[0:3], SDHC_CMD, SDHC_CLK, FTM4_CH[6:7], LPUART[3:6]	EV_{IN}	GND to EV_{DD}	V	–
	Main power supply for internal circuitry of SerDes	SV_{IN}	GND to SV_{DD}	V	–
	Ethernet management interface 2 (EMI2), GPIO2	TV_{IN}	GND to TV_{DD}	V	–
PHY transceiver signals	USB transceiver supply for USB PHY	USB_HV_{IN}	GND to $USBn\_HV_{DD}$	V	–
	Analog and digital HS supply for USB PHY	USB_SV_{IN}	GND to USB_SV_{DD}	V	–
Teledyne e2v temperature range	A Range Temperature	T_C, T_J	T_C = -40°C (min) to T_J = 105°C (max)	°C	–
	F Range Temperature	T_C, T_J	T_C = -40°C (min) to T_J = 125°C (max)	°C	–
	M Range Temperature	T_C, T_J	T_C = -55°C (min) to T_J = 125°C (max)	°C	–
	Secure boot fuse programming	T_A, T_J	T_A = 0°C (min) to T_J = 105°C (max)	°C	2

Notes:

1. RGMII is supported at 2.5V or 1.8V.
2. TA_PROG_SFP must be supplied 1.8V and the chip must operate in the specified fuse programming temperature range only during secure boot fuse programming, subject to the power sequencing constraints shown in Power sequencing. For all other operating conditions, TA_PROG_SFP must be tied to GND.
3. For additional information, see the core and platform supply voltage filtering section in the chip design checklist.

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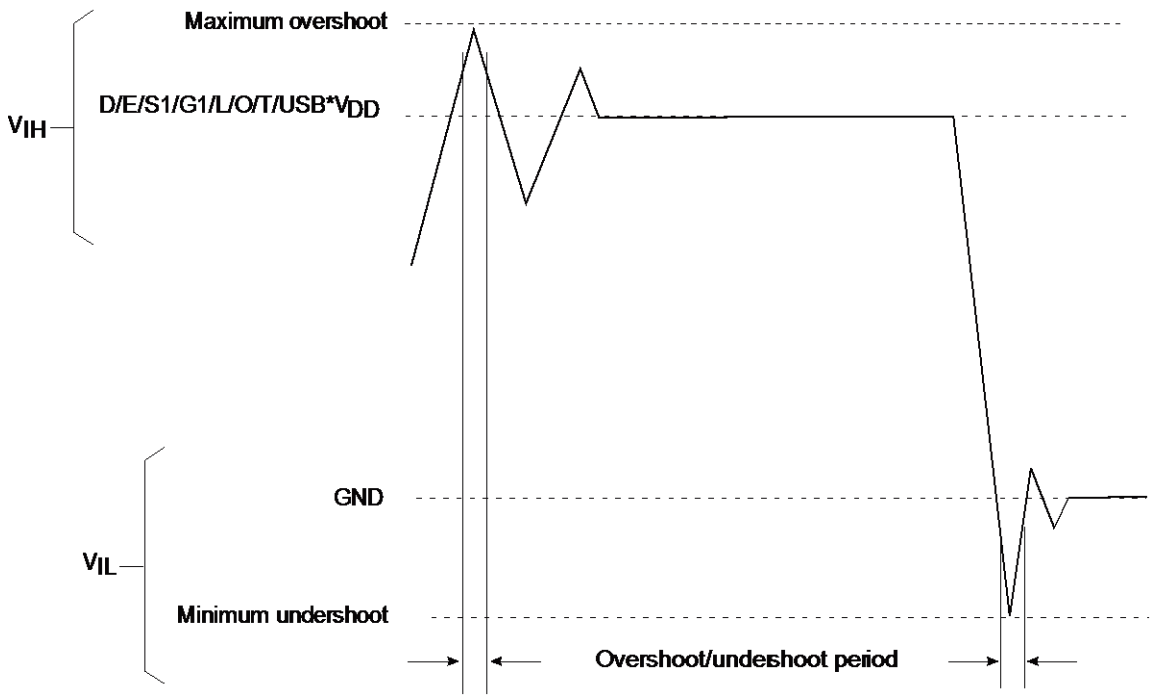
4. Supply voltage specified at the voltage sense pin. Voltage input pins should be regulated to provide specified voltage at the sense pin.
5. Operation at 1.08 V is allowable for up to 25 ms at initial power on.
6. Analog and Digital SS supply for USB PHY.
7. Analog and Digital HS supply for USB PHY.
8. For supported voltage requirement for a given part number, see Table 145.
9. AVDD_PLAT, AVDD_CGA1, AVDD_CGA2, and AVDD_D1 are measured at the input to the filter and not at the pin of the device.
10. This power supply needs a sink and source regulator
11. D1_V_{PP} must equal or greater than D1_V_{DD} at all times when powered.

This figure shows the undershoot and overshoot voltages at the interfaces of the chip.

Figure 8. Overshoot/undershoot voltage for G1V_{DD}/OV_{DD}/SV_{DD}/TV_{DD}/ LV_{DD}/EV_{DD}/DV_{DD}/ USB_HV_{DD}/USB_SV_{DD}



Notes:

The overshoot/undershoot period should be less than 10% of shortest possible toggling period of the input signal or per input signal specific protocol requirement. For GPIO input signal overshoot/undershoot period, it should be less than 10% of the SYSCLK period.

See Table 4 for actual recommended core voltage. Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in see Table 4. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD}, EV_{DD}, DV_{DD}, TV_{DD}, and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses differential receivers referenced by the internally supplied reference signal as is appropriate for the JEDEC DDR4 electrical signaling standard. The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

3.1.3 Output driver characteristics

This chip provides information on the characteristics of the output driver strengths.

NOTE
These values are preliminary estimates.

Table 5. Output drive capability

Driver type	Output impedance (Ω)			Supply Voltage	Notes
	Minimum (2)	Typical	Maximum (3)		
DDR4 signal	-	18(full-strength mode) 27(half-strength mode)	-	$G1V_{DD}$ = 1.2 V	1
Ethernet interface, Ethernet management interface 1 (EMI1), 1588, IRQ11, FTM1, FTM2	30	50	70	LV_{DD} = 2.5V	-
	30	45	60	LV_{DD} = 1.8V	-
MDC of Ethernet management interface 2 (EMI 2)	45	65	100	TV_{DD} = 1.2 V	-
	40	55	75	TV_{DD} = 1.8V	-
	40	60	90	TV_{DD} = 2.5V	-
MDIO of Ethernet management interface 2 (EMI 2)	30	40	60	TV_{DD} = 1.2 V	-
	25	33	44	TV_{DD} = 1.8V	-
	25	40	57	TV_{DD} = 2.5V	-
IFC, SPI, IRQ[0:2], Tamper Detect, System Control, SYSCLK, DDRCLK, RTC, EVT[0:4], DFT, JTAG, CLK_OUT, QSPI, FTM[5:7], eSDHC_DAT[4:7], eSDHC_CMD/DAT0_DIR, eSDHC_DAT123_DIR, eSDHC_SYNC_IN/OUT, SDHC_VS	30	45	60	OV_{DD} = 1.8 V	-
eSDHC_DAT[0:3], eSDHC_CMD, eSDHC_CLK, FTM4_CH[6:7], LPUART[3:6]	45	65	90	EV_{DD} = 3.3V	-
	40	55	75	EV_{DD} = 1.8V	
DUART, I2C, USB2/3_DRVVBUS, EVT_B[5:8], LPUART[1:2], LPUART4, FTM3_CH[1:7], FTM4_CH[1:5], FTM8	40	55	75	DV_{DD} = 1.8V	-
	45	65	90	DV_{DD} = 3.3V	

Notes
1. The drive strength of the DDR4 in half-strength mode is at T_J = 105°C and at $G1V_{DD}$ (min).
2. Estimated number based on best case processed device.
3. Estimated number based on worst case processed device.

3.1.4 General AC timing specifications

This table provides AC timing specifications for the sections not covered under the specific interface sections.

Table 6. AC Timing specifications

Parameter	Symbol	Min	Max	Unit	Notes
Input signal rise and fall times	t_R/t_F	-	5	ns	1

1. Rise time refers to signal transitions from 10% to 90% of supply; fall time refers to transitions from 90% to 10% of supply

3.2 Power sequencing

The chip requires that its power rails be applied in a specific sequence in order to ensure proper device operation. For power up, these requirements are as follows:

1. OV_{DD}, DV_{DD}, LV_{DD}, EV_{DD}, TV_{DD}, XV_{DD}, AV_{DD}_CGAn, AV_{DD}_PLAT, AV_{DD}_D1, AV_{DD}_SDn_PLL1, AV_{DD}_SDn_PLL2, USB_HV_{DD}. Drive TA_PROG_SFP = GND.
   - PORESET_B input must be driven asserted and held during this step.
2. V_{DD}, SV_{DD}, TA_BB_V_{DD}, USB_SDV_{DD}, USB_SV_{DD}
   - The 3.3 V (USB_HV_{DD}) in Step 1 and 1.0 V (USB_SDV_{DD}, USB_SV_{DD}) in Step 2 supplies can power up in any sequence provided all these USB supplies ramp up within 95 ms with respect to each other.
3. $G1V_{DD}$, D1_V_{TT}, D1_V_{PP}, D1_V_{DD}
   - D1_V_{PP} must be equal or greater than D1_V_{DD} at all times when powered.
   - D1_Vpp can raise at any time, step 1 or 2, as far as it raises before D1_Vdd

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of their value.

All supplies must be at their stable values within 400 ms.

Negate PORESET_B input when the required assertion/hold time has been met per Table 24.

NOTE

- While V_{DD} is ramping up, current may be supplied from VDD through QLS1046A to $G1V_{DD}$.
- If using Trust Architecture Security Monitor battery backed features, prior to VDD ramping up to the 0.5 V level, ensure that OV_{DD} is ramped to recommended operational voltage and SYSCLK or DIFF_SYSCLK/ DIFF_SYSCLK_B is running. These clocks should have a minimum frequency of 800 Hz and a maximum frequency not greater than the supported system clock frequency for the device.
- Ramp rate requirements should be met per Table 13.

Warning
Only 300,000 POR cycles are permitted per lifetime of a device. Note that this value is based on design estimates and is preliminary.

For secure boot fuse programming, use the following steps:

1. After negation of PORESET_B, drive TA_PROG_SFP = 1.8 V after a required minimum delay per Table 7.
2. After fuse programming is complete, it is required to return TA_PROG_SFP = GND before the system is power cycled or powered down (VDD ramp down) per the required timing specified in Table 7. See Security fuse processor for additional details.

Warning
No activity other than that required for secure boot fuse programming is permitted while TA_PROG_SFP is driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while TA_PROG_SFP = GND.

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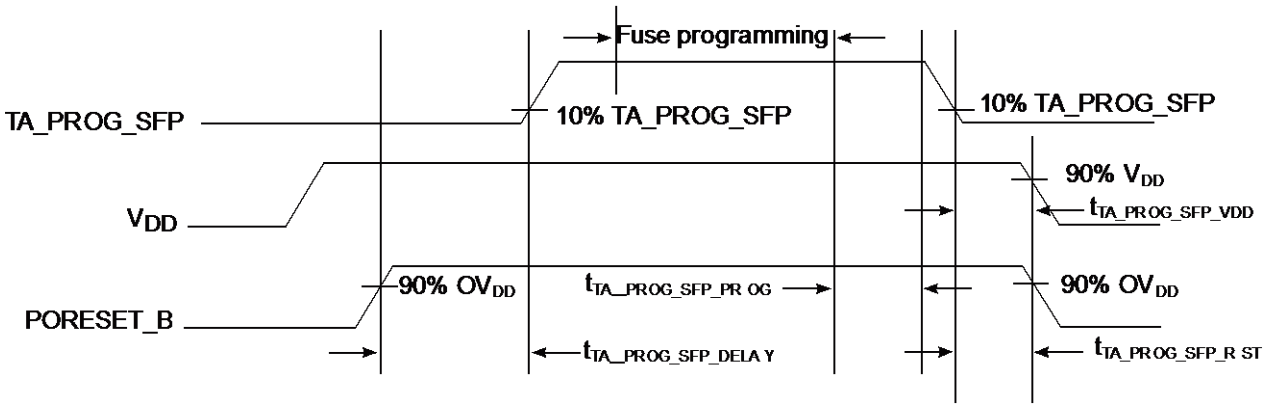
This figure shows the TA_PROG_SFP timing diagram.

Figure 9. TA_PROG_SFP timing diagram



NOTE: TA_PROG_SFP must be stable at 1.8 V prior to initiating fuse programming.

This table provides information on the power-down and power-up sequence parameters for TA_PROG_SFP.

Table 7. TA_PROG_SFP timing (5)

Driver type	Min	Max	Unit	Notes
$t_{TA\_PROG\_SFP\_DELAY}$	100	–	SYSCLKs	1
$t_{TA\_PROG\_SFP\_PROG}$	0	–	us	2
$t_{TA\_PROG\_SFP\_VDD}$	0	–	us	3
$t_{TA\_PROG\_SFP\_RST}$	0	–	us	4

Notes:

1. Delay required from the deassertion of PORESET_B to driving TA_PROG_SFP ramp up. Delay measured from PORESET_B deassertion at 90% OVDD to 10% TA_PROG_SFP ramp up.
2. Delay required from fuse programming completion to TA_PROG_SFP ramp down start. Fuse programming must complete while TA_PROG_SFP is stable at 1.8 V. No activity other than that required for secure boot fuse programming is permitted while TA_PROG_SFP is driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while TA_PROG_SFP = GND. After fuse programming is complete, it is required to return TA_PROG_SFP = GND.
3. Delay required from TA_PROG_SFP ramp-down complete to VDD ramp-down start. TA_PROG_SFP must be grounded to minimum 10% TA_PROG_SFP before VDD reaches 90% VDD.
4. Delay required from TA_PROG_SFP ramp-down complete to PORESET_B assertion. TA_PROG_SFP must be grounded to minimum 10% TA_PROG_SFP before PORESET_B assertion reaches 90% OVDD.
5. Only six secure boot fuse programming events are permitted per lifetime of a device.

3.3 Power-down requirements

The power-down cycle must complete such that power supply values are below 0.4 V before a new power-up cycle can be started.

If performing secure boot fuse programming per the requirements in Power sequencing, it is required that TA_PROG_SFP = GND before the system is power cycled (PORESET_B assertion) or powered down (V_{DD} ramp down) per the required timing specified in Power sequencing.

3.4 Power characteristics

This table provides the power dissipations of the V_{DD} supply and SerDes supply (SV_{DD}) for various operating platform clock frequencies versus the core and DDR clock frequencies.

Table 8. QLS1046A core power dissipation (9)

Core frequency (MHz)	Platform/ FMan frequency (MHz)	DDR frequency (MHz)	V_{DD} (V)	SV_{DD} (V)	Junction temperature (ºC)	Power mode	Power (W)		Total Core and platform power (W) (1)	Notes
							V_{DD}	SV_{DD} (8)		
1800	700/800	2100	1.0	1.0	65	Typical	8.5	0.9	9.4	2, 3
					85	Thermal	11.4	0.9	12.3	4, 7
						Maximum	14.3	0.9	15.2	5, 6, 7
					105	Thermal	14.4	0.9	15.3	4, 7
						Maximum	17.3	0.9	18.2	5, 6, 7
					125	Thermal	16.7	0.9	17.6	4, 7
						Maximum	19.6	0.9	20.5	5, 6, 7
1600	700/800	2100	1.0	1.0	65	Typical	7.7	0.9	8.7	2, 3
					85	Thermal	10.7	0.9	11.6	4, 7
						Maximum	13.2	0.9	14.2	5, 6, 7
					105	Thermal	13.7	0.9	14.6	4, 7
						Maximum	16.3	0.9	17.2	5, 6, 7
					125	Thermal	16.0	0.9	16.9	4, 7
						Maximum	18.6	0.9	19.5	5, 6, 7
1400	600/600	2100	1.0	1.0	65	Typical	7.3	0.9	8.2	2, 3
					85	Thermal	8.7	0.9	9.6	4, 7
						Maximum	11.1	0.9	12.0	5, 6, 7
					105	Thermal	10.5	0.9	11.5	4, 7
						Maximum	12.9	0.9	13.8	5, 6, 7
					125	Thermal	12.8	0.9	13.7	4, 7
						Maximum	15.2	0.9	16.1	5, 6, 7
1200	400/600	1600	1.0	1.0	65	Typical	5.2	0.9	6.2	2, 3, 10
					85	Thermal	6.4	0.9	7.3	4, 7, 10
						Maximum	8.0	0.9	9.0	5, 6, 7, 10
					105	Thermal	8.3	0.9	9.2	4, 7, 10
						Maximum	9.9	0.9	10.8	5, 6, 7, 10
					125	Thermal	8.4	0.9	9.3	4, 7, 10
						Maximum	9.6	0.9	10.5	5, 6, 7, 10

Notes:

1. Combined power of V_{DD} and SV_{DD} with DDR controller and all SerDes banks active. Does not include I/O power.
2. Typical power assumes Dhrystone running with activity factor of 70% (on all cores) and executing DMA on the platform with 100% activity factor.
3. Typical power based on nominal, processed device.
4. Thermal power assumes Dhrystone running with activity factor of 70% (on all cores) and executing DMA on the platform at 100% activity factor.

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5. Maximum power assumes Dhrystone running with activity factor at 100% (on all cores) and executing DMA on the platform at 115% activity factor.
6. Maximum power is provided for power supply design sizing.
7. Thermal and maximum power are based on worst case processed device.
8. Total SV_{DD} Power conditions:
   a. SerDes 1 : XFI x2, 10 Gbaud
   b. SerDes 1 : SGMII x2, 1.25 Gbaud
   c. SerDes 2 : PEX x2, 5 Gbaud
9. Power numbers are only applicable to part numbering offering from Table 144. For example: A 1.8GHz offering part when runs at 1.4GHz will have power numbers higher than listed for a 1.4GHz part number.
10. These power numbers are valid when purchasing the 1400MHz device and running the clocks at these conditions.

Table 9. QLS1026A core power dissipation (9)

Core frequency (MHz)	Platform/ FMan frequency (MHz)	DDR frequency (MHz)	V_{DD} (V)	S V_{DD} (V)	Junction temperature (ºC)	Power mode	Power (W)		Total Core and platform power (W) (1)	Notes
							V_{DD}	SV_{DD} (8)		
1800	700/800	2100	1.0	1.0	65	Typical	6.7	0.9	7.6	2, 3
					85	Thermal	9.3	0.9	10.2	4, 7
						Maximum	11.5	0.9	12.4	5, 6, 7
					105	Thermal	12.3	0.9	13.2	4, 7
						Maximum	14.5	0.9	15.4	5, 6, 7
					125	Thermal	14.6	0.9	15.5	4, 7
						Maximum	16.8	0.9	17.7	5, 6, 7
1600	700/800	2100	1.0	1.0	65	Typical	6.2	0.9	7.1	2, 3
					85	Thermal	8.7	0.9	9.6	4, 7
						Maximum	10.7	0.9	11.6	5, 6, 7
					105	Thermal	11.7	0.9	12.6	4, 7
						Maximum	13.7	0.9	14.6	5, 6, 7
					125	Thermal	14.0	0.9	14.9	4, 7
						Maximum	16.0	0.9	16.9	5, 6, 7
1400	600/600	2100	1.0	1.0	65	Typical	6.0	0.9	6.9	2, 3
					85	Thermal	7.2	0.9	8.1	4, 7
						Maximum	9.1	0.9	10.0	5, 6, 7
					105	Thermal	9.0	0.9	10.0	4, 7
						Maximum	10.9	0.9	11.8	5, 6, 7
					125	Thermal	11.3	0.9	12.2	4, 7
						Maximum	13.2	0.9	14.1	5, 6, 7
1200	400/600	1600	1.0	1.0	65	Typical	3.9	0.7	4.7	2, 3
					85	Thermal	4.7	0.7	5.5	4, 7
						Maximum	6.0	0.7	6.7	5, 6, 7
					105	Thermal	6.1	0.7	6.9	4, 7
						Maximum	7.3	0.7	8.1	5, 6, 7
					125	Thermal	8.4	0.7	9.1	4, 7
						Maximum	9.6	0.7	10.3	5, 6, 7

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Notes:
1. Combined power of V_{DD} and SV_{DD} with DDR controller and all SerDes banks active. Does not include I/O power.
2. Typical power assumes Dhrystone running with activity factor of 80% (on all cores) and executing DMA on the platform with 100% activity factor.
3. Typical power based on nominal, processed device.
4. Thermal power assumes Dhrystone running with activity factor of 80% (on all cores) and executing DMA on the platform at 100% activity factor.
5. Maximum power assumes Dhrystone running with activity factor at 100% (on all cores) and executing DMA on the platform at 115% activity factor.
6. Maximum power is provided for power supply design sizing.
7. Thermal and maximum power are based on worst case processed device.
8. Total SV_{DD} power conditions:
   SerDes 1 : XFI x2, 10 Gbaud
   SerDes 1 : SGMII x2, 1.25 Gbaud
   SerDes 2 : PEX x2, 5 Gbaud
9. Power numbers are only applicable to part numbering offering from Table 144. For example: A 1.8GHz offering part when runs at 1.4GHz will have power numbers higher than listed for a 1.4GHz part number.
10. These power numbers are valid when purchasing the 1400MHz device and running the clocks at these conditions.

3.4.1 Low-power mode saving estimation

See this table for low-power mode savings.

Table 10. Low-power mode savings, 65C (1, 2, 3)

Mode	Core Frequency = 1.2 GHz (VDD =0.9V)	Core Frequency = 1.4 GHz (VDD =1.0V)	Core Frequency = 1.6 GHz (VDD =1.0V)	Core Frequency = 1.8 GHz (VDD =1.0V)	Units	Comments	Notes
PW15	0.71	0.77	0.88	0.99	Watts	Saving realized moving from run to PW15 state, single core. Arm in STANDBYWFI/WFE	4
PH20	0.05	0.21	0.24	0.26	Watts	Saving realized moving from run to PH20 state, single core. Arm in STANDBYWFI/ WFE-retain	
LPM20	1.02	1.70	1.94	2.18	Watts	Saving realized moving from PH20 to LPM20 per device	5

Notes:
1. Power for VDD only
2. Typical power assumes Dhrystone running with activity factor of 70%
3. Typical power based on nominal process distribution for this device.
4. PW15 power savings with 1 core. Maximum savings would be N times, where N is the number of used cores.
5. LPM20 has all platform clocks disabled.

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3.5 DDR4 power consumption

The DDR4 power consumption during normal operation strongly depends on the usage profile (transfer speed, write and read duty cycles, …). For this reason, it is not possible to provide power key figures fitting all applications. Teledyne e2vprovides a power consumption estimation spreadsheet that should be used to estimate the power drawn by the DDR4 on D1_V_{DD} and D1_V_{PP} supplies. This power calculation tool is available upon request.

The maximum D1_V_{DD} current consumed by the DDR4 memory during the initialization is provided in the following table:

Symbol	DDR4-2100	Unit
Iddinit: DDR4 initialization current on D1_V_{DD} (1)	1600	mA
Ippinit: DDR4 initialization current on D1_Vpp (2)	N/S (2)	mA

(1) : Current during initialization of the DDR4 done by the LS1046A DDR4 controller during the boot of Qormino (ex: initialization under U-Boot). Maximum duration: 1s

(2) : The initialization current on D1_VPP is not specified. It is lower or equal than the current drawn in normal operation, which can be estimated with the power consumption estimation spreadsheet.

D1_V_{TT} corresponds to the termination voltage for the Address/Control/Command signals of the DDR4 (to which the integrated termination resistors are connected). The current on this supply can be either positive or negative, meaning that the voltage regulation must have sink and source capability. The maximum current on D1_VTT is reached when all Address/Control/Command signals are in the same state, and it is given in the next table.

VREFCA is not a supply, and it is used as a voltage reference. Its maximum leakage current is also provided in the table.

Supply	Maximum	Unit
D1_V_{TT}	±223	mA
VREFCA 4GB	±10	µA
VREFCA 8GB	±18	µA

Power supply sizing depends on the memory DDR4 controller. For the QLS1046, typical power sizing is provided in the following table:

Memory controller	DDR4	Power supply sizing
LS1046	4GB (Rev A)	1.2 A
	8GB (Rev B)	1.6 A

3.6 I/O power dissipation

This table provides the estimated I/O power numbers for each block: DDR, PCI Express, IFC, Ethernet controller, SGMII, eSDHC, USB, SPI, DUART, IIC, SATA, and GPIO. Note that these numbers are based on design estimates only.

Table 11. IO power supply estimated values

Interface	Parameter	Symbol	Typical	Unit	Notes
DDR4	x64 2100 MT/s data rate	G1VDD (1.2 V)	761	mW	1
PCI Express	x1, 2.5 Gbaud	XVDD (1.35 V)	79	mW	1, 2
	x2, 2.5 Gbaud		132	mW	
	x4, 2.5 Gbaud		237	mW	
	x1, 5 Gbaud		80	mW	
	x2, 5 Gbaud		133	mW	
	x4, 5 Gbaud		239	mW	
	x1, 8 Gbaud		81	mW	
	x2, 8 Gbaud		136	mW	
	x4, 8 Gbaud		245	mW	
SGMII	x1, 1.25 Gbaud	XVDD (1.35 V)	77	mW	1, 2
	x2, 1.25 Gbaud		127	mW	
	x3, 1.25 Gbaud		177	mW	
	x4, 1.25 Gbaud		227	mW	
	x1, 3.125 Gbaud		79	mW	
	x2, 3.125 Gbaud		132	mW	
	x3, 3.125 Gbaud		184	mW	
QSGMII	x1, 5 Gbaud	XVDD (1.35 V)	80	mW	1, 2
XFI	x1, 10 Gbaud	XVDD (1.35 V)	81	mW	1, 2
	x2, 10 Gbaud		136	mW	
SATA (per port)	3.0 Gbaud	XVDD (1.35 V)	73	mW	1, 2
	6.0 Gbaud		74	mW	
USB1/USB2/USB3 (per PHY)	x1 Super speed mode	USB_HVDD (3.3 V)	46	mW	1, 4
		USB_SVDD (1 V)	37	mW	
		USB_SDVDD (1 V)	4	mW	
USB1/USB2/USB3 (per PHY)	x1 High speed mode	USB_HVDD (3.3 V)	79	mW	1, 4
		USB_SVDD (1 V)	0.31	mW	
		USB_SDVDD (1 V)	4.9	mW	
IFC	16-bit, 100 MHz	OVDD (1.8 V)	60	mW	1
DUART	.	DVDD (3.3 V)	18	mW	1
		DVDD (1.8 V)	9	mW	
I2C	.	DVDD (3.3 V)	17	mW	1
		DVDD (1.8 V)	9	mW	

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Interface	Parameter	Symbol	Typical	Unit	Notes
SPI	.	OVDD (1.8 V)	8	mW	1, 6
eSDHC	.	EVDD (3.3 V)	19	mW	1, 6
	.	EVDD (1.8V)	21	mW	
System control	.	OVDD (1.8 V)	16	mW	1, 6
EC1	RGMII	LVDD (2.5 V)	24	mW	1, 6
		LVDD (1.8 V)	17	mW	
EC2	RGMII	LVDD (2.5 V)	24	mW	
		LVDD (1.8 V)	17	mW	
QSPI	.	OVDD (1.8V)	17	mW	1, 6
IEEE1588	.	LVDD (2.5 V)	14	mW	1, 6
		LVDD (1.8 V)	10	mW	
JTAG + DFT	.	OVDD (1.8V)	10	mW	1, 6
GPIO	x8	3.3 V	5	mW	1, 3, 6
		2.5 V	4	mW	
		1.8 V	3	mW	
PLL core and system (per PLL)	.	AVDD_CGA1, AVDD_CGA2, AVDD_PLAT (1.8 V)	30	mW	1, 6
PLL DDR	.	AVDD_D1 (1.8 V)	30	mW	1, 6
PLL SerDes	.	AVDD_SD1_PLL1, AVDD_SD1_PLL2, AVDD_SD2_PLL1, AVDD_SD2_PLL2 (1.35 V)	100	mW	1, 6
Interrupts (IRQ)	.	OVDD (1.8 V)	4	mW	1
		DVDD (1.8 V)	9	mW	
		DVDD (3.3 V)	18	mW	
		LVDD (2.5 V)	2	mW	
		LVDD (1.8 V)	1	mW	
Ethernet management interface 1	.	LVDD (2.5 V)	3	mW	1
		LVDD (1.8 V)	2	mW	
Ethernet management interface 2	.	TVDD (2.5 V)	3	mW	1
		TVDD (1.8 V)	2	mW	
		TVDD (1.2 V)	2	mW	
TA_PROG_SFP	.	TA_PROG_SFP (1.8 V)	173	mW	5
TH_VDD	.	TH_VDD (1.8 V)	18	mW	

Notes:

1. The typical values are estimates and based on simulations at nominal recommended voltage for the I/O power supply and assuming 105°C junction temperature.
2. The total power numbers of XVDD is dependent on customer application use case. This table lists all the SerDes configurations possible for the device. To get the X1VDD power numbers, the user should add the combined lanes to match to the total SerDes Lanes used, not simply multiply the power numbers by the number of lanes.
3. GPIOs are supported on OVDD, LVDD, DVDD, TVDD and EVDD power rails.
4. USB power supply pins are shared between three USB controllers.

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5. The maximum power requirement is during programming. No active power beyond leakage levels should be drawn and the supply must be grounded when not programming.
6. Assuming 15 pF total capacitance load per pin.

Table 12. TA_BB_VDD power dissipation

Supply	Maximum	Unit	Notes
TA_BB_VDD (SoC off, 40°C)	40	µW	1
TA_BB_VDD (SoC off, 70°C)	55	µW	1

Note:

1. When SoC is off, TA_BB_VDD may be supplied by battery power to retain the Zeroizable Master Key and other trust architecture state. Board should implement a PMIC, which switches TA_BB_VDD to battery when SoC is powered down. See the Device reference manual trust architecture chapter for more information.

3.7 Power-on ramp rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum power-on ramp rate is required to avoid excess in-rush current.

This table provides the power supply ramp rate specifications.

Table 13. Power supply ramp rate

Parameter	Min	Max	Unit	Notes
Required ramp rate for all voltage supplies (including OV_{DD}/DV_{DD}/$G1V_{DD}$/ SV_{DD}/XV_{DD}/LV_{DD}/EV_{DD}/TV_{DD} all core and platform V_{DD} supplies, TA_PROG_SFP, and all AV_{DD} supplies.)	–	25	V/ms	1, 2
Required ramp rate for TA_PROG_SFP	–	25	V/ms	1, 2
Required ramp rate for USB_HVDD	–	26.7	V/ms	1, 2

Notes:

1. Ramp rate is specified as a linear ramp from 10% to 90%. If non-linear (for example, exponential), the maximum rate of change from 200 mV to 500 mV is the most critical as this range might falsely trigger the ESD circuitry.
2. Over full recommended operating temperature range. See Table 4.

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3.8 Input clocks

3.8.1 System clock (SYSCLK)

This section describes the system clock DC electrical characteristics and AC timing specifications.

3.8.1.1 SYSCLK DC electrical characteristics

This table provides the SYSCLK DC characteristics.

Table 14. SYSCLK DC electrical characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	–	–	V	1
Input low voltage	V_{IL}	–	–	0.3 x OV_{DD}	V	1
Input capacitance	C_{IN}	–	7	12	pF	–
Input current (V_{IN}= 0 V or V_{IN} =	I_{IN}	–	–	± 50	µA	2

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 4.
2. At recommended operating conditions with OV_{DD}= 1.8 V. See Table 4.

3.8.1.2 SYSCLK AC timing specifications

This table provides the SYSCLK AC timing specifications.

Table 15. SYSCLK AC timing specifications (1, 5)

Parameter/condition	Symbol	Min	Typ	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}		100.0		MHz	2
SYSCLK cycle time	t_{SYSCLK}		10.0		ns	1, 2
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	–	60	%	2
SYSCLK slew rate	–	1	–	4	V/ns	3
SYSCLK peak period jitter	–	–	–	± 150	ps	–
SYSCLK jitter phase noise at -56 dBc	–	–	–	500	kHz	4
AC Input Swing Limits at 1.8 V OV_{DD}	ΔV_{AC}	1.08	–	1.8	V	–

Notes:
1. **Caution:** The relevant clock ratio settings must be chosen such that the resulting SYSCLK frequencies do not exceed their respective maximum or minimum operating frequencies.
2. Measured at the rising edge and/or the falling edge at $OV_{DD}/2$.
3. Slew rate as measured from 0.35 x OV_{DD} to 0.65 x OV_{DD}.
4. Phase noise is calculated as FFT of TIE jitter.
5. At recommended operating conditions with OV_{DD} = 1.8 V. See Table 4.

3.8.1.3 USB 3.0 reference clock requirements

This table summarizes the requirements of the reference clock provided to the USB 3.0 SSPHY. There are two options for the reference clock of USB PHY: SYSCLK or DIFF_SYSCLK/DIFF_SYSCLK_B. The following table provides the additional requirements when SYSCLK or DIFF_SYSCLK/DIFF_SYSCLK_B is used as USB REFCLK. This table can also be used for 100 MHz reference clock requirements.

Table 16. Reference clock requirements

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Reference clock frequency offset	FREF_OFFSET	-300	–	300	ppm	–
Reference clock random jitter (RMS)	RMSJREF_CLK	–	–	3	ps	1, 2
Reference clock deterministic jitter	DJREF_CLK	–	–	150	ps	3
Duty cycle	DCREF_CLK	40	–	60	%	–

Notes:

1. 1.5 MHz to Nyquist frequency. For example, for 100 MHz reference clock, the Nyquist frequency is 50 MHz.
2. The peak-to-peak Rj specification is calculated as 14.069 times the RMS Rj for 10-12 BER.
3. DJ across all frequencies.

3.8.2 Spread-spectrum sources

Spread-spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter to diffuse the EMI spectral content.

The jitter specification given in this table considers short-term (cycle-to-cycle) jitter only. The clock generator's cycle-to-cycle output jitter should meet the chip's input cycle-to- cycle jitter requirement.

Frequency modulation and spread are separate concerns; the chip is compatible with spread-spectrum sources if the recommendations listed in this table are observed.

Table 17. Spread-spectrum clock source recommendations[3]

Parameter	Min	Max	Unit	Notes
Frequency modulation	–	60	kHz	–
Frequency spread	–	1.0	%	1, 2

Notes:

1. SYSCLK frequencies that result from frequency spreading and the resulting core frequency must meet the minimum and maximum specifications given in Table 15.
2. Maximum spread-spectrum frequency may not result in exceeding any maximum operating frequency of the device.
3. At recommended operating conditions with OVDD = 1.8 V. See Table 4.

CAUTION

The processor's minimum and maximum SYSCLK and core/ platform/DDR frequencies must not be exceeded, regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated core/platform/DDR frequency should use only down-spreading to avoid violating the stated limits.

3.8.3 Real-time clock timing (RTC)

The real-time clock timing (RTC) input is sampled by the platform clock. The output of the sampling latch is then used as an input to the Watchdog, Flextimer, 1588 Timer and snvs unit; there is no need for jitter specification. The minimum period of the RTC signal should be greater than or equal to 16x the period of the platform clock with a 50% duty cycle. There is no minimum RTC frequency; RTC may be pulled to ground, if not needed.

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3.8.4 Gigabit Ethernet reference clock timing

This table provides the Ethernet gigabit reference clock DC electrical characteristics with LV_{DD} = 2.5 V / 1.8 V.

Table 18. EC*n*_GTX_CLK125 DC electrical characteristics (LV_{DD} = 2.5 V / 1.8 V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x LV_{DD}	–	–	V	2
Input low voltage	V_{IL}	–	–	0.2 x LV_{DD}	V	2
Input capacitance	C_{IN}	–	–	6	pF	–
Input current (VIN = 0 V or VIN = LVDD)	I_{IN}	–	–	± 50	µA	3

Notes:
1. For recommended operating conditions, see Table 4.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max V_{IN} values found in Table 4.
3. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 4.

This table provides the Ethernet gigabit reference clock AC timing specifications.

Table 19. EC*n*_GTX_CLK125 AC timing specifications (1)

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC*n*_GTX_CLK125 frequency	f_{G125}	125 - 100 ppm	125	125 + 100 ppm	MHz	–
EC*n*_GTX_CLK125 cycle time	t_{G125}	--	8	--	ns	–
EC*n*_GTX_CLK125 rise and fall time	t_{G125R}/t_{G125F}	–	–	0.75	ns	2
EC*n*_GTX_CLK125 duty cycle 1000Base-T for RGMII	t_{G125H}/t_{G125}	40	–	60	%	3

Notes:
1. At recommended operating conditions with LV_{DD} = 1.8 V ± 90mV / 2.5 V ± 125 mV. See Table 4.
2. Rise times are measured from 20% of LV_{DD} to 80% of LV_{DD}. Fall times are measured from 80% of LV_{DD} to 20% of LV_{DD}.
3. EC*n*_GTX_CLK125 is used to generate the GTX clock for the Ethernet transmitter. See RGMII AC timing specifications for duty cycle for the 10Base-T and 100Base-T reference clocks.

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3.8.5 DDR clock (DDRCLK)

This section provides the DDRCLK DC electrical characteristics and AC timing specifications.

3.8.5.1 DDRCLK DC electrical characteristics

This table provides the DDRCLK DC electrical characteristics.

Table 20. DDRCLK DC electrical characteristics[3]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	–	–	V	1
Input low voltage	V_{IL}	–	–	0.3 x OV_{DD}	V	1
Input capacitance	C_{IN}	–	7	12	pF	–
Input current (V_{IN}= 0V or V_{IN} = OV_{DD})	I_{IN}	–	–	± 50	µA	2

Notes:
1. The min VIL and max VIH values are based on the respective min and max OVIN values found in Table 4.
2. The symbol OVIN, in this case, represents the OVIN symbol referenced in Table 4.
3. At recommended operating conditions with OVDD = 1.8 V. See Table 4.

3.8.5.2 DDRCLK AC timing specifications

This table provides the DDRCLK AC timing specifications.

Table 21. DDRCLK AC timing specifications[5]

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
DDRCLK frequency	f_{DDRCLK}		100.0		MHz	1, 2
DDRCLK cycle time	t_{DDRCLK}		10.0		ns	1, 2
DDRCLK duty cycle	t_{KHK}/t_{DDRCLK}	40	–	60	%	2
DDRCLK slew rate	–	1	–	4	V/ns	3
DDRCLK peak period jitter	–	–	–	± 150	ps	–
DDRCLK jitter phase noise at -56 dBc	–	–	–	500	kHz	4
AC Input Swing Limits at 1.8 V OV_{DD}	ΔV_{AC}	1.08	–	1.8	V	–

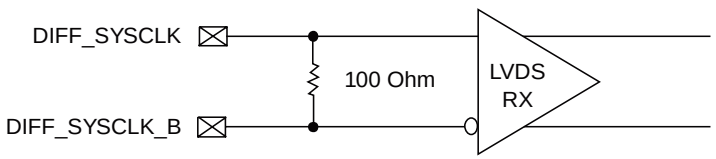
Notes:
1. **Caution:** The relevant clock ratio settings must be chosen such that the resulting DDRCLK frequencies do not exceed their respective maximum or minimum operating frequencies.
2. Measured at the rising edge and/or the falling edge at OV_{DD}/2.
3. Slew rate as measured from 0.35 x OV_{DD} to 0.65 x OV_{DD}.
4. Phase noise is calculated as FFT of TIE jitter.
5. At recommended operating conditions with OV_{DD} = 1.8V. See Table 4.

3.8.6 Differential system clock (DIFF_SYSCLK/DIFF_SYSCLK_B) timing specifications

Single Source clocking mode requires single onboard oscillator to provide reference clock input to Differential System clock pair (DIFF_SYSCLK/DIFF_SYSCLK_B).

This Differential clock pair input provides clock to Core, Platform, DDR and USB PLL's This figure shows a receiver reference diagram of the Differential System clock.

Figure 10. LVDS receiver



This section provides the differential system clock DC and AC timing specifications.

3.8.6.1 Differential system clock DC electrical characteristics

The differential system clock receiver voltage requirements are as specified in the Recommended operating conditions table.

The differential system clock can also be single-ended. For this, DIFF_SYSCLK_B should be connected to $OV_{DD}/2$.

This table provides the differential system clock (DIFF_SYSCLK/DIFF_SYSCLK_B) DC specifications.

Table 22. Differential system clock DC electrical characteristics[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input differential voltage swing	V_{id}	100	-	600	mV	2
Input common mode voltage	V_{icm}	50	-	1570	mV	-
Power supply current	I_{cc}	-	-	5	mA	-
Input capacitance	C_{in}	1.45	1.5	1.55	pF	-

Note:

1. At recommended operating conditions with OVDD = 1.8 V, see Table 4 for details.
2. Input differential voltage swing (Vid) specified is equal to |VDIFF_SYSCLK_P - VDIFF_SYSCLK_N|

3.8.6.2 Differential system clock AC timing specifications

Spread spectrum clocking is not supported on differential system clock pair input.

This table provides the differential system clock (DIFF_SYSCLK/DIFF_SYSCLK_B) AC specifications.

Table 23. Differential system clock AC electrical characteristics[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
DIFF_SYSCLK/DIFF_SYSCLK_B frequency range	t_{DIFF_SYSCLK}	-	100	-	MHz	-
DIFF_SYSCLK/DIFF_SYSCLK_B frequency tolerance	t_{DIFF_TOL}	-300	-	+300	ppm	-
Duty cycle	t_{DIFF_DUTY}	40	50	60	%	-

Notes:

1. This is evaluated with supply noise profile at +/- 5% sine wave
2. At recommended operating conditions with OV_{DD} = 1.8 V, see Table 4.

3.8.7 Other input clocks

A description of the overall clocking of this device is available in the chip reference manual in the form of a clock subsystem block diagram. For information about the input clock requirements of functional sourced external of the chip, such as SerDes, Ethernet management, eSDHC, and IFC, see the specific interface section.

3.9 RESET initialization

This table provides the AC timing specifications for the RESET initialization timing.

Table 24. RESET Initialization timing specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of PORESET_B after all power rails are stable	1	–	ms	1
Required input assertion time of HRESET_B	32	–	SYSCLKs	2, 3
Maximum rise/fall time of HRESET_B	–	10	SYSCLK	4
Maximum rise/fall time of PORESET_B	–	1	SYSCLK	4
Input setup time for POR configs (other than cfg_eng_use0) with respect to negation of PORESET_B	4	–	SYSCLKs	2, 5
Input hold time for all POR configs with respect to negation of PORESET_B	2	–	SYSCLKs	2
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of PORESET_B	–	5	SYSCLKs	2

Notes:

1. PORESET_B must be driven asserted before the core and platform power supplies are powered up.
2. SYSCLK is the primary clock input for the chip.
3. The device asserts HRESET_B as an output when PORESET_B is asserted to initiate the power-on reset process. The device releases HRESET_B sometime after PORESET_B is deasserted. The exact sequencing of HRESET_B deassertion is documented in the reference manual's "Power-on Reset Sequence" section.
4. The system/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.
5. For proper clock selection, terminate cfg_eng_use0 with a pull up or pull down of 4.7 kΩ to ensure that the signal will have a valid state as soon as the IO voltage reach its operating condition.

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3.9.1 Power-Up and Initialization Sequence of the DDR4

1. Apply power (MRST_N must be maintained below 0.2 × D1_V_{DD} while supplies ramp up; all other inputs may be undefined). When supplies have ramped to a valid stable level, MRST_N must be maintained below 0.2 × D1_V_{DD} for a minimum of tPW_RESET. CKE is pulled LOW anytime before MRST_N is de-asserted (minimum time of 10ns). The power voltage ramp time between 300mV to D1_V_{DD} min must be no greater than 200ms. D1_V_{PP} must ramp at the same time or before D1_V_{DD}, and D1_V_{PP} must be equal to or higher than D1_V_{DD} at all times. After D1_V_{DD} has ramped and reached the stable level, the initialization sequence must be started within 3s.

– Apply D1_V_{PP} without any slope reversal before or at the same time as D1_V_{DD}
– D1_V_{DD} is driven from a single-power converter output and apply D1_V_{DD} without any slope reversal before or at the same time as D1_V_{TT} and VREFCA.
– The voltage levels on all balls of the DDR interface other than D1_V_{DD} and GND must be less than or equal to D1_V_{DD} on one side and must be greater than or equal to GND on the other side.
– D1_V_{TT} is limited to 0.76V MAX when the power ramp is complete.
– VREFCA tracks D1_V_{DD} /2.

2. After MRST_N is de-asserted, wait for another 500µs until CKE becomes active. During this time, the device will start internal state initialization; this will be done independently of external clocks. A reasonable attempt was made in the design to power up with the following default MR settings: gear-down mode (MR3 A[3]): 0 = 1/2 rate; per-DRAM addressability (MR3 A[4]): 0 = disable; maximum power-down (MR4 A[1]): 0 = disable; CS to command/address latency (MR4 A[8:6]): 000 = disable; CA parity latency mode (MR5 A[2:0]): 000 = disable. However, it should be assumed that at power up the MR settings are undefined and should be programmed as shown below.

3. Clocks (CK_t, CK_c) need to be started and stabilized for at least 10ns or 5 tCK (whichever is larger) before CKE goes active. Because CKE is a synchronous signal, the corresponding setup time to clock (tIS) must be met. Also, a DESELECT command must be registered (with tIS setup time to clock) at clock edge Td. After the CKE is registered HIGH after RESET, CKE needs to be continuously registered HIGH until the initialization sequence is finished, including expiration of tDLLK and tZQINIT.

4. The device keeps its ODT in High-Z state as long as MRST_N is asserted. Further, the SDRAM keeps its ODT in High-Z state after MRST_N de-assertion until CKE is registered HIGH. The ODT input signal may be in an undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held either LOW or HIGH. If RTT(NOM) is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power-up initialization sequence is finished, including the expiration of tDLLK and tZQINIT.

5. After CKE is registered HIGH, wait a minimum of RESET CKE EXIT time, tXPR, before issuing the first MRS command to load mode register (tXPR = MAX (tXS; 5 × tCK).
6. Issue MRS command to load MR3 with all application settings, wait tMRD.
7. Issue MRS command to load MR6 with all application settings, wait tMRD.
8. Issue MRS command to load MR5 with all application settings, wait tMRD.
9. Issue MRS command to load MR4 with all application settings, wait tMRD.
10. Issue MRS command to load MR2 with all application settings, wait tMRD.
11. Issue MRS command to load MR1 with all application settings, wait tMRD.
12. Issue MRS command to load MR0 with all application settings, wait tMOD.
13. Issue a ZQCL command to start ZQ calibration.
14. Wait for tDLLK and tZQINIT to complete.
15. The device will be ready for normal operation.

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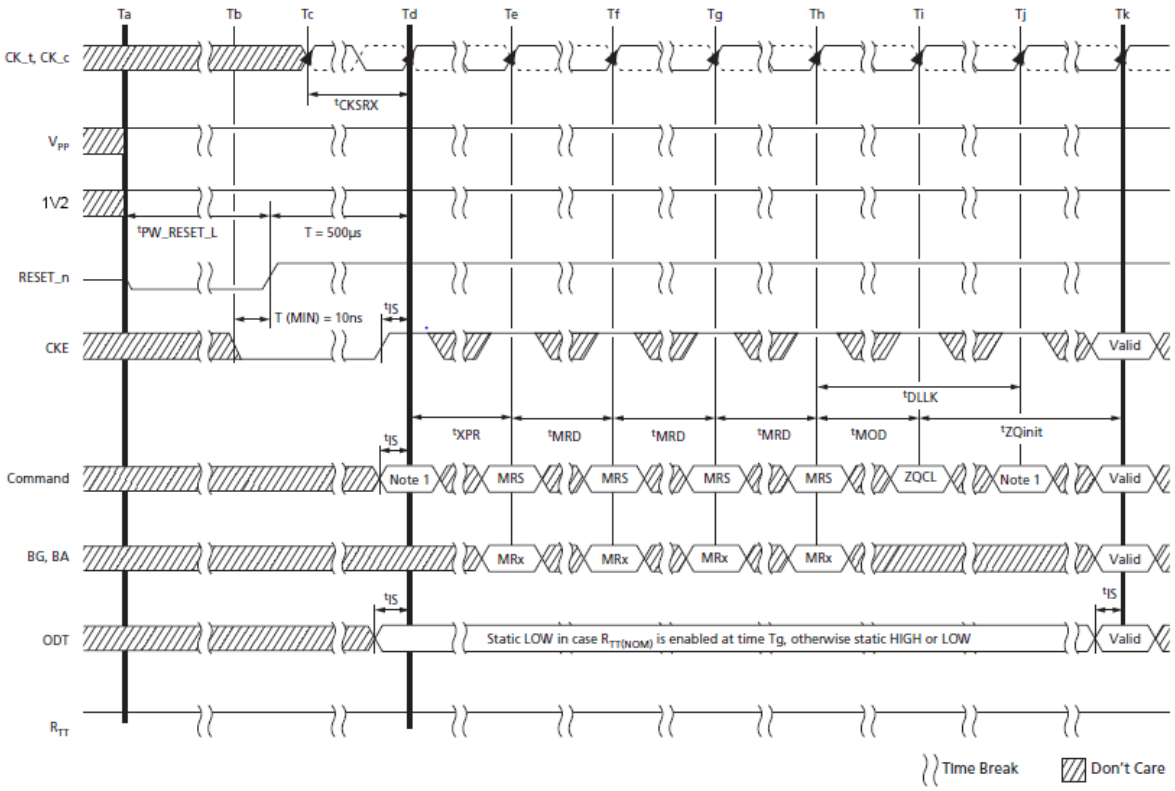
A stable valid D1_V_{DD} level is a set DC level (0 Hz to 20 MHz) and must be no less than D1_V_{DD} ,min and no greater than D1_V_{DD} ,max. If the set DC level is altered anytime after initialization, the DLL reset and calibrations must be performed again after the new set DC level is stable. AC noise of ±60mV (greater than 20 MHz) is allowed on D1_V_{DD} provided the noise doesn't alter D1_V_{DD} to less than D1_V_{DD} ,min or greater than D1_V_{DD} ,max.
A stable valid D1_V_{PP} level is a set DC level (0 Hz to 20 MHz) and must be no less than D1_V_{PP},min and no greater than D1_V_{PP},max. If the set DC level is altered anytime after initialization, the DLL reset and calibrations must be performed again after the new set DC level is stable. AC noise of ±120mV (greater than 20 MHz) is allowed on D1_V_{PP} provided the noise doesn't alter D1_V_{PP} to less than D1_V_{PP},min or greater than D1_V_{PP},max.



3.10 DDR4 SDRAM controller

This section describes the DC and AC electrical specifications for the DDR4 SDRAM controller interface. Note that the required $G1V_{DD}$(typ) voltage is 1.2 V when interfacing to DDR4 SDRAM.

3.10.1 DDR4 SDRAM interface DC electrical characteristics

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR4 SDRAM.

Table 25. DDR4 SDRAM interface DC electrical characteristics ($G1V_{DD}$ = 1.2 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input low	V_{IL}	–	0.7 x $G1V_{DD}$ - 0.175	V	3
Input high	V_{IH}	0.7 x $G1V_{DD}$ + 0.175	–	V	3
I/O leakage current	I_{OZ}	-200	200	µA	

Notes:

1. $G1V_{DD}$ is expected to be within 60 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
2. V_{TT} and VREFCA are applied directly to the DRAM device. Both V_{TT} and VREFCA voltages must track $G1V_{DD}/2$.
3. Input capacitance load for DQ, DQS, and DQS_B are available in the IBIS models.
4. See the IBIS model for the complete output IV curve characteristics.
5. Output leakage is measured with all outputs disabled, 0V ≤ VOUT ≤ $G1V_{DD}$
6. For recommended operating conditions, see Table 4.

3.10.2 DDR4 SDRAM interface AC timing specifications

This section provides the AC timing specifications for the DDR SDRAM controller interface. The DDR controller supports DDR4 memories. Note that the required GV_{DD}(typ) voltage is 1.2 V when interfacing to DDR4 SDRAM.

3.10.2.1 DDR4 SDRAM interface input AC timing specifications

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR4 SDRAM.

Table 26. DDR4 SDRAM interface input AC timing specifications [1]

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage ≤ 2100 MT/s data rate	V_{ILAC}	–	0.7 x $G1V_{DD}$ - 0.175	V	–
AC input high voltage ≤ 2100 MT/s data rate	V_{IHAC}	0.7 x $G1V_{DD}$ + 0.175	–	V	–

Note:

1. For recommended operating conditions, see Table 4.

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR4 SDRAM.

Table 27. DDR4 SDRAM interface input AC timing specifications [3]

Parameter	Symbol	Min	Max	Unit	Notes
Controller skew for MDQS-MDQ/MECC	t_{CISKEW}	–	–	ps	1
2100 MT/s data rate		-80	80		
1800 MT/s data rate		-93	93		
1600 MT/s data rate		-112	112		
1300 MT/s data rate		-125	125		
Tolerated Skew for MDQS-MDQ/MECC	t_{DISKEW}	–	–	ps	2
2100 MT/s data rate		-154	154		
1800 MT/s data rate		-175	175		
1600 MT/s data rate		-200	200		
1300 MT/s data rate		-250	250		

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This must be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: $t_{DISKEW} = \pm(T \div 4 - abs(t_{CISKEW}))$ where T is the clock period and abs(t_{CISKEW}) is the absolute value of t_{CISKEW}.
3. For recommended operating conditions, see Table 4.

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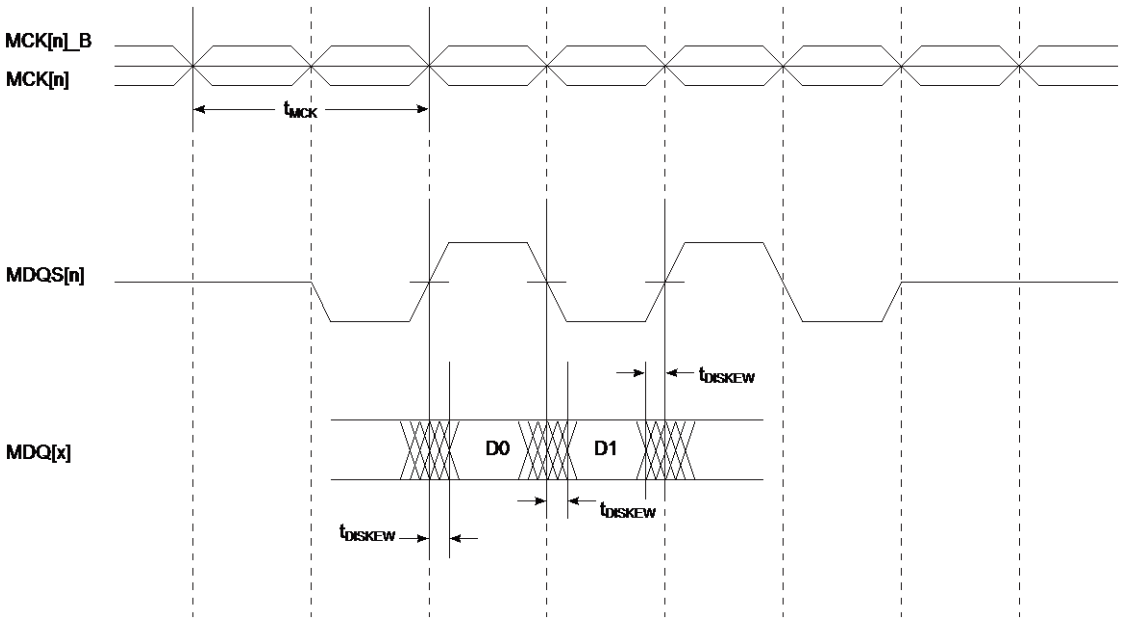
This figure shows the DDR4 SDRAM interface input timing diagram.

Figure 11. DDR4 SDRAM interface input timing diagram



3.10.2.2 DDR4 SDRAM interface output AC timing specifications

This table contains the output AC timing targets for the DDR4 SDRAM interface.

Table 28. DDR4 SDRAM interface output AC timing specifications ($G1V_{DD}$ = 1.2 V)[7]

Parameter	Symbol[1]	Min	Max	Unit	Notes
MCK[n] cycle time	t_{MCK}	952	1538	ps	2
ADDR/CMD/CNTL output setup with respect to MCK	t_{DDKHAS}	–	–	ps	3
2100 MT/s data rate		350	–		
1800 MT/s data rate		410	–		
1600 MT/s data rate		495	–		
1300 MT/s data rate		606	–		
ADDR/CMD/CNTL output hold with respect to MCK	t_{DDKHAX}	–	–	ps	3
2100 MT/s data rate		350	–		
1800 MT/s data rate		390	–		
1600 MT/s data rate		495	–		
1300 MT/s data rate		606	–		
MCK to MDQS Skew	t_{DDKHMH}	-150	150	ps	4,7
MDQ/MECC/MDM output data eye	$t_{DDKXDEYE}$	–	–	ps	5
2100 MT/s data rate		320	–		
1800 MT/s data rate		350	–		
1600 MT/s data rate		400	–		
1300 MT/s data rate		500	–		

Parameter	Symbol[1]	Min	Max	Unit	Notes
MDQS preamble	t_{DDKHMP}	0.9 x t_{MCK}	–	ps	–
MDQS postamble	t_{DDKHME}	0.4 x t_{MCK}	0.6 x t_{MCK}	ps	–

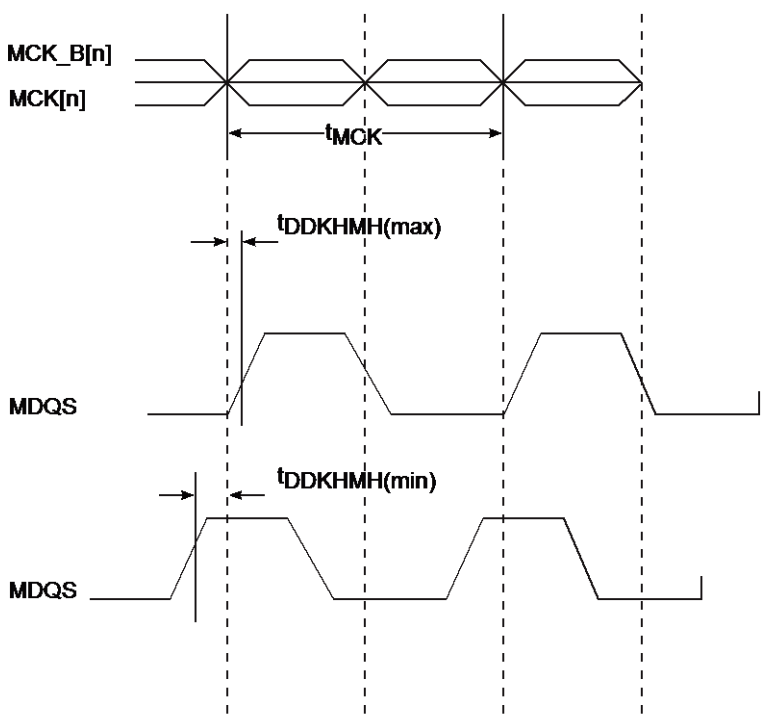
Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time tMCK memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/MCK_B and MDQS/MDQS_B referenced measurements are made from the crossing of the two signals.
3. ADDR/CMD/CNTL includes all DDR SDRAM output signals except MCK/MCK_B, MCS_B, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This is typically set to the same delay as in DDR_SDRAM_CLK_CNTL[CLK_ADJUST]. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the chip reference manual for a description and explanation of the timing modifications enabled by the use of these bits.
5. Available eye for data (MDQ), ECC (MECC), and data mask (MDM) outputs at the pin of the processor. Memory controller will center the strobe (MDQS) in the available data eye at the DRAM (end point) during the initialization.
6. Note that this is required to program the start value of the DQS adjust for write leveling.
7. For recommended operating conditions, see Table 4.

NOTE
For the ADDR/CMD/CNTL setup and hold specifications in Table 28, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.

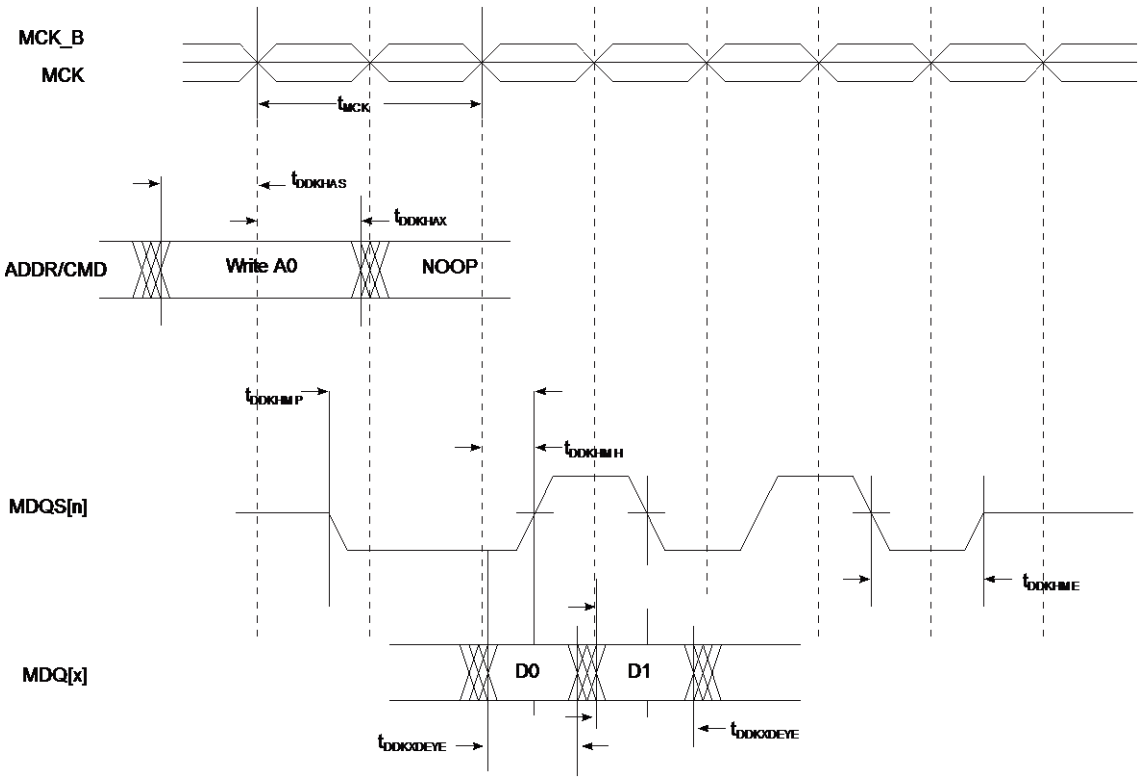
This figure shows the DDR4 SDRAM interface output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

Figure 12. t_{DDKHMH} timing diagram



This figure shows the DDR4 SDRAM output timing diagram.

Figure 13. DDR4 output timing diagram



3.11 Ethernet interface, Ethernet management interface, IEEE Std 1588™

This section describes the DC and AC electrical characteristics for the Ethernet controller, Ethernet management, and IEEE Std 1588 interfaces.

3.11.1 SGMII interface

Each SGMII port features a 4-wire AC-coupled serial link from the SerDes interface of the chip, as shown in Figure 14, where C_{TX} is the external (on board) AC-coupled capacitor. Each SerDes transmitter differential pair features 100-Ω output impedance.

Each input of the SerDes receiver differential pair features 50-Ω on-die termination to GND*n*. The reference circuit of the SerDes transmitter and receiver is shown in Figure 84.

3.11.1.1 SGMII clocking requirements for SD*n*_REF_CLK1_P and SD*n*_REF_CLK1_N

When operating in SGMII mode, the EC*n*_GTX_CLK125 clock is not required for this port. Instead, a SerDes reference clock is required on SD*n*_REF_CLK[1:2]_P and SD*n*_REF_CLK[1:2]_N pins. SerDes lanes may be used for SerDes SGMII configurations based on the RCW Configuration field SRDS_PRTCL.

For more information on these specifications, see SerDes reference clocks

3.11.1.2 SGMII DC electrical characteristics

This section describes the electrical characteristics for the SGMII interface.

3.11.1.2.1 SGMII and SGMII 2.5G transmit DC specifications

This table describes the SGMII SerDes transmitter AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD*n*_TX*n*_P and SD*n*_TX*n*_N) as shown in Figure 15.

Table 29. SGMII DC transmitter electrical characteristics (X*n*V_{DD} = 1.35 V) (4)

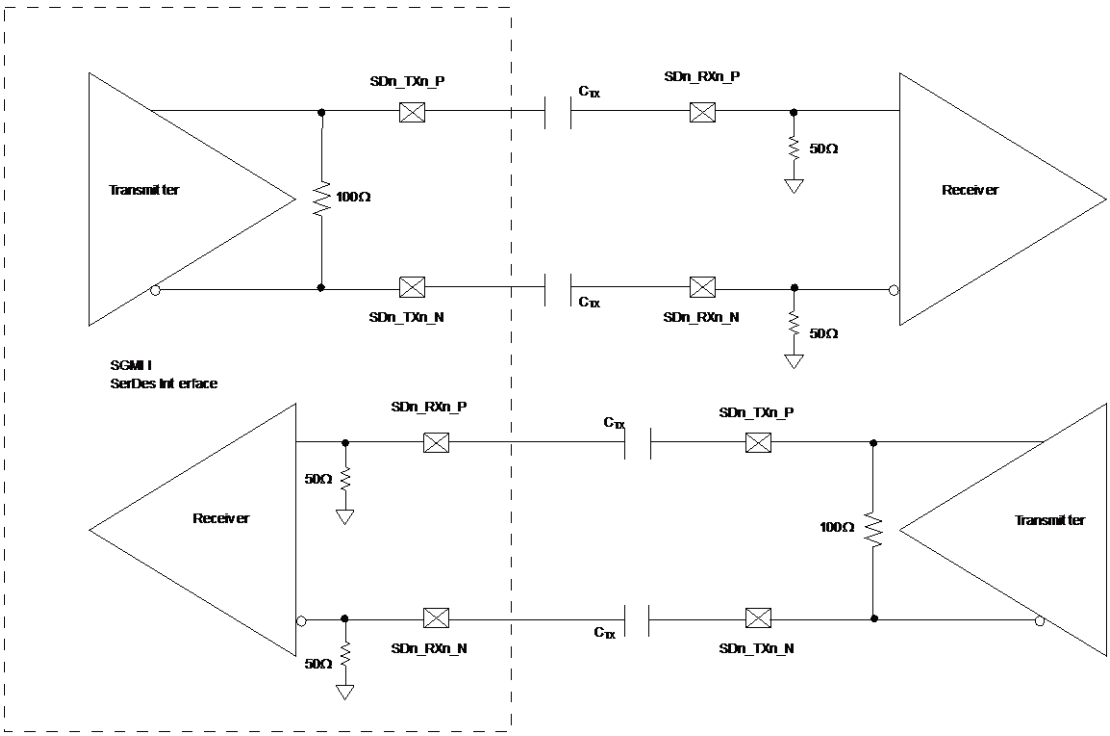
Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output high voltage	V_{OH}	-	-	1.5 x $\lvert V_{OD} \rvert$-max	mV	1
Output low voltage	V_{OL}	$\lvert V_{OD} \rvert$-min/2	-	-	mV	1
Output differential voltage (2,3,5) (XV_{DD}-Typ at 1.35 V)	$\lvert V_{OD} \rvert$	320	500.0	725.0	mV	TECR0[AMP_RED]=0b000000
		293.8	459.0	665.6		TECR0[AMP_RED]=0b000001
		266.9	417.0	604.7		TECR0[AMP_RED]=0b000011
		240.6	376.0	545.2		TECR0[AMP_RED]=0b000010
		213.1	333.0	482.9		TECR0[AMP_RED]=0b000110
		186.9	292.0	423.4		TECR0[AMP_RED]=0b000111
		160.0	250.0	362.5		TECR0[AMP_RED]=0b010000
Output impedance (differential)	R_O	80	100	120	Ω	-

Notes:

1. This does not align to DC-coupled SGMII.
2. $\lvert V_{OD} \rvert = \lvert V_{SD\_TXn\_P} - V_{SD\_TXn\_N} \rvert$. $\lvert V_{OD} \rvert$ is also referred to as output differential peak voltage. $V_{TX\text{-}DIFFp\text{-}p} = 2 \times \lvert V_{OD} \rvert$.
3. The $\lvert V_{OD} \rvert$ value shown in the Typ column is based on the condition of XVDD_SRDSn-Typ = 1.35 V, no common mode offset variation. SerDes transmitter is terminated with 100-Ω differential load between SDn _TXn_P and SDn_TXn_N.
4. For recommended operating conditions, see Table 4.
5. Example amplitude reduction setting for SGMII on SerDes1 lane A: LNATECR0[AMP_RED] = 0b000001 for an output differential voltage of 459 mV typical.

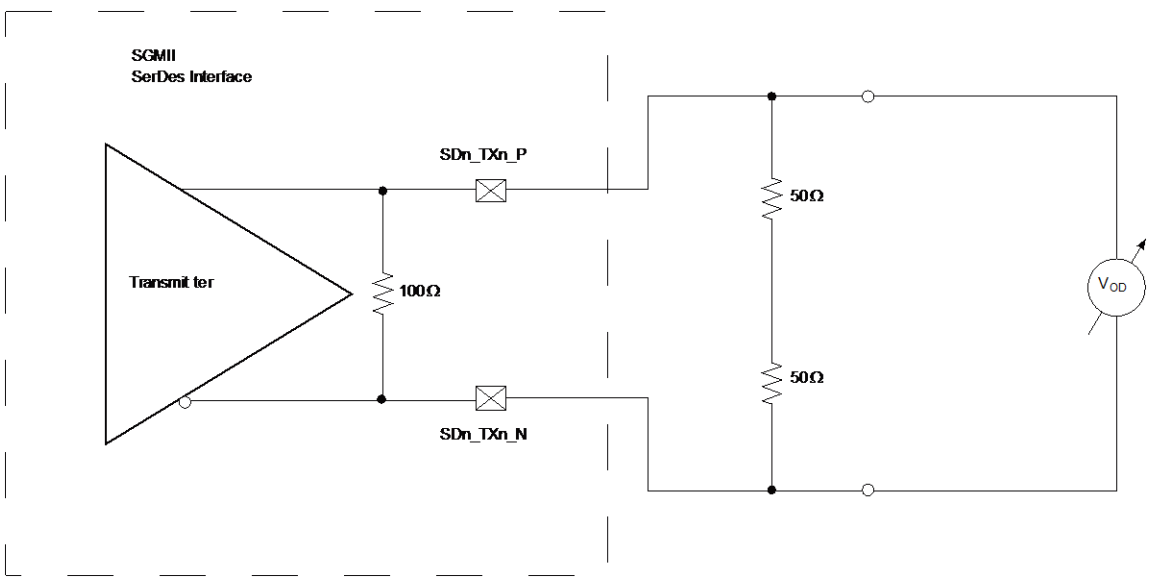
This figure shows an example of a 4-wire AC-coupled SGMII serial link connection.

Figure 14. 4-wire AC-coupled SGMII serial link connection example



This figure shows the SGMII transmitter DC measurement circuit.

Figure 15. SGMII transmitter DC measurement circuit



This table defines the SGMII 2.5G transmitter DC electrical characteristics for 3.125 GBaud.

Table 30. SGMII 2.5G transmitter DC electrical characteristics (X*n*V_{DD} = 1.35 V)(1)

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Output differential voltage	$\lvert V_{OD} \rvert$	400	-	600	mV	
Output impedance (differential)	R_O	80	100	120	Ω	-

Notes:
1. For recommended operating conditions, see Table 4.

3.11.1.2.2 SGMII and SGMII 2.5G DC receiver electrical characteristics

This table lists the SGMII DC receiver electrical characteristics. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 31. SGMII DC receiver electrical characteristics (4)

Parameter		Symbol	Min	Typ	Max	Unit	Notes
DC input voltage range		-	N/A			-	1
Input differential voltage	REIDL_TH = 001	$V_{RX\_DIFFp-p}$	100	-	1200	mV	2, 5
	REIDL_TH = 100		175	-			
Loss of signal threshold	REIDL_TH = 001	V_{LOS}	30	-	100	mV	3, 5
	REIDL_TH = 100		65	-	175		
Receiver differential input impedance		Z_{RX_DIFF}	80	-	120	Ω	-

Notes:
1. Input must be externally AC coupled.
2. $V_{RX\_DIFFp-p}$ is also referred to as peak-to-peak input differential voltage.
3. The concept of this parameter is equivalent to the electrical idle detect threshold parameter in PCI Express. See PCI Express DC physical layer receiver specifications, and PCI Express AC physical layer receiver specifications, for further explanation.
4. For recommended operating conditions, see Table 4.
5. The REIDL_TH shown in the table refers to the chip's SRDSxLNmGCR1[REIDL_TH] bit field.

This table defines the SGMII 2.5G receiver DC electrical characteristics for 3.125 GBaud.

Table 32. SGMII 2.5G receiver DC timing specifications (1)

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input differential voltage	$V_{RX\_DIFFp-p}$	200	-	1200	mV	-
Loss of signal threshold	V_{LOS}	75	-	200	mV	-
Receiver differential input impedance	Z_{RX_DIFF}	80	-	120	Ω	-

Note:
1. For recommended operating conditions, see Table 4.

3.11.1.3 SGMII AC timing specifications

This section describes the AC timing specifications for the SGMII interface.

3.11.1.3.1 SGMII and SGMII 2.5G transmit AC timing specifications

This table provides the SGMII and SGMII 2.5G transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include RefClk jitter.

Table 33. SGMII transmit AC timing specifications (4)

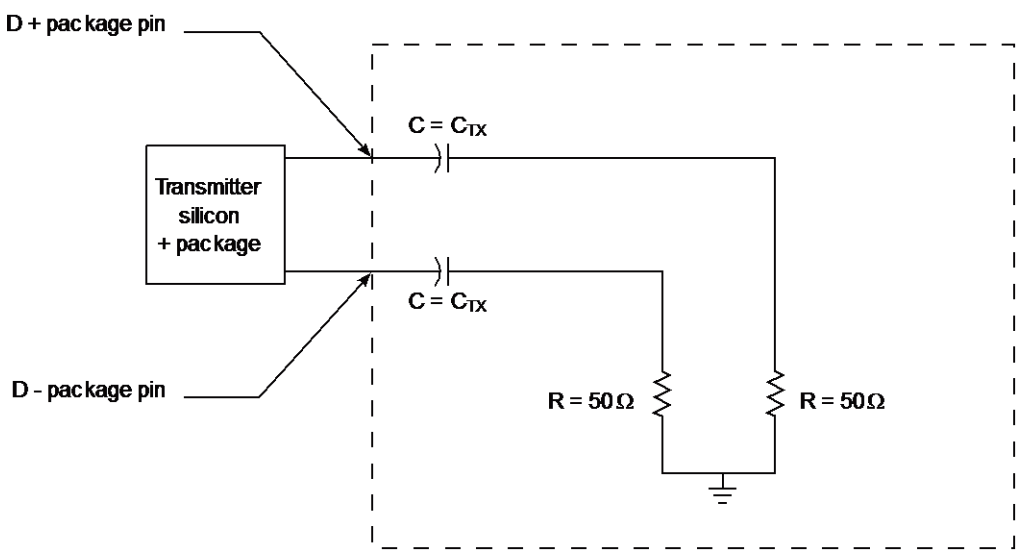
Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter	JD	-	-	0.17	UI p-p	-
Total jitter	JT	-	-	0.35	UI p-p	2
Unit Interval: 1.25 GBaud (SGMII)	UI	800 - 100 ppm	800	800 + 100 ppm	ps	1
Unit Interval: 3.125 GBaud (2.5G SGMII])	UI	320 - 100 ppm	320	320 + 100 ppm	ps	1
AC coupling capacitor	C_{TX}	10	-	200	nF	3

Notes:
1. Each UI is 800 ps ± 100 ppm or 320 ps ± 100 ppm.
2. See Figure 17 for single frequency sinusoidal jitter measurements.
3. The external AC coupling capacitor is required. It is recommended that it be placed near the device transmitter output.
4. For recommended operating conditions, see Table 4.

3.11.1.3.2 SGMII AC measurement details

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SD*n*_TX*n*_P and SD*n*_TX*n*_N) or at the receiver inputs (SD*n*_RX*n*_P and SD*n*_RX*n*_N) respectively, as shown in this figure.

Figure 16. SGMII AC test/measurement load



3.11.1.3.3 SGMII and SGMII 2.5G receiver AC timing specifications

This table provides the SGMII and SGMII 2.5G receiver AC timing specifications. The AC timing specifications do not include RefClk jitter. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 34. SGMII receiver AC timing specifications (3)

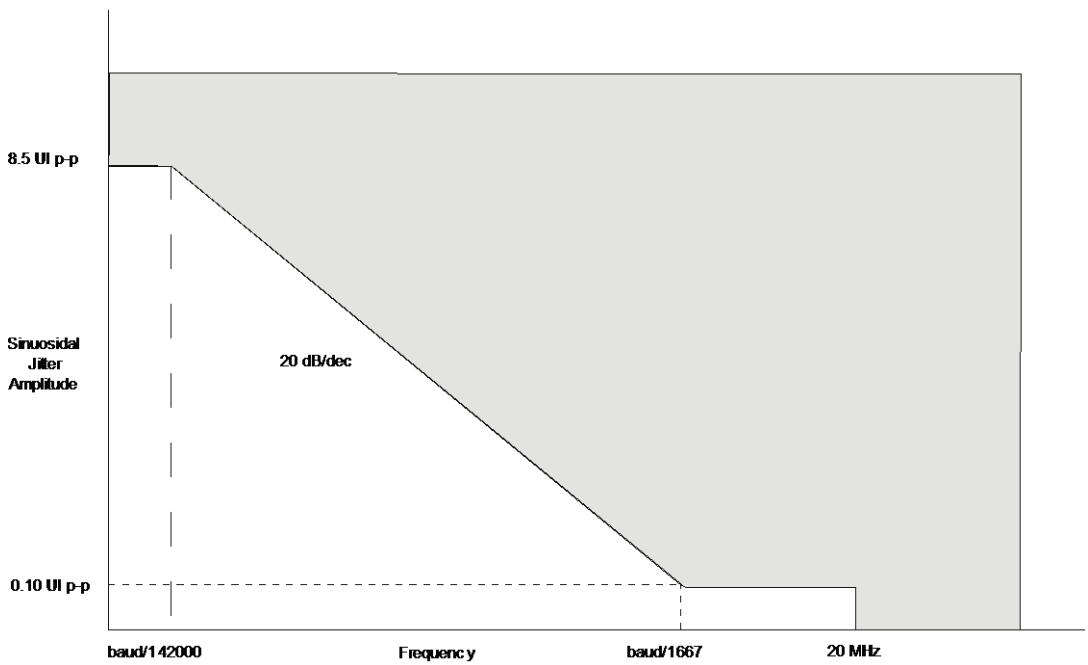
Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter tolerance	J_D	-	-	0.37	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	-	-	0.55	UI p-p	1
Total jitter tolerance	J_T	-	-	0.65	UI p-p	1, 2
Bit error ratio	BER	-	-	10^{-12}	-	-
Unit Interval: 1.25 GBaud (SGMII)	UI	800 - 100 ppm	800	800 + 100 ppm	ps	1
Unit Interval: 3.125 GBaud (2.5G SGMII])	UI	320 - 100 ppm	320	320 + 100 ppm	ps	1

Notes:

1. Measured at receiver
2. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 1. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.
3. For recommended operating conditions, see Table 4.

The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of this figure.

Figure 17. Single-frequency sinusoidal jitter limits



3.11.2 QSGMII interface

This section describes the QSGMII clocking and its DC and AC electrical characteristics.

3.11.2.1 QSGMII clocking requirements for SD*n*_REF_CLK*n* and SD*n*_REF_CLK*n*_B

For more information on these specifications, see SerDes reference clocks.

3.11.2.2 QSGMII DC electrical characteristics

This section discusses the electrical characteristics for the QSGMII interface.

3.11.2.2.1 QSGMII transmitter DC specifications

This table describes the QSGMII SerDes transmitter AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD*n*_TX*n* and SD*n*_TX*n*_B).

Table 35. QSGMII DC transmitter electrical characteristics (X*n*V_{DD} = 1.35V) (1)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output differential voltage	V_{DIFF}	400	-	900	mV	-
Differential resistance	T_{RD}	80	100	120	Ω	-

Notes:
1. For recommended operating conditions, see Table 4.

3.11.2.2.2 QSGMII DC receiver electrical characteristics

This table defines the QSGMII receiver DC electrical characteristics.

Table 36. QSGMII receiver DC timing specifications (1)

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input differential voltage	V_{DIFF}	100	-	900	mV	-
Differential resistance	R_{RDIN}	80	100	120	Ω	-

Notes:
1. For recommended operating conditions, see Table 4.

3.11.2.3 QSGMII AC timing specifications

This section discusses the AC timing specifications for the QSGMII interface.

3.11.2.3.1 QSGMII transmit AC timing specifications

This table provides the QSGMII transmitter AC timing specifications.

Table 37. QSGMII transmit AC timing specifications (1)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Transmitter baud rate	T_{BAUD}	5.000 - 100 ppm	5.000	5.000 + 100 ppm	Gb/s	-
Uncorrelated high probability jitter	T_{UHPJ}	-	-	0.15	UI p-p	-
Total jitter tolerance	J_T	-	-	0.30	UI p-p	-

Notes:
1. For recommended operating conditions, see Table 4.

3.11.2.3.2 QSGMII receiver AC timing Specification

This table provides the QSGMII receiver AC timing specifications.

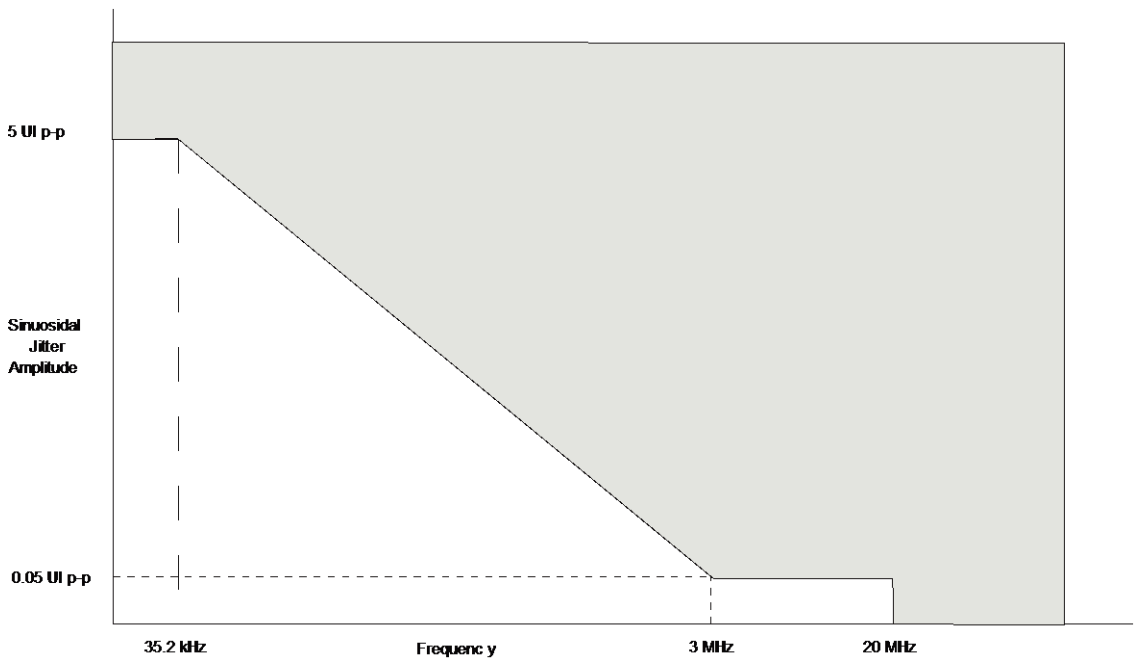
Table 38. QSGMII receive AC timing specifications (2)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Receiver baud rate	R_{BAUD}	5.000 - 100 ppm	5.000	5.000 + 100 ppm	Gb/s	-
Uncorrelated bounded high probability jitter	R_{DJ}	-	-	0.15	UI p-p	-
Correlated bounded high probability jitter	R_{CBHPJ}	-	-	0.30	UI p-p	1
Bounded high probability jitter	R_{BHPJ}	-	-	0.45	UI p-p	-
Sinusoidal jitter, maximum	R_{SJ-max}	-	-	5.00	UI p-p	-
Sinusoidal jitter, high frequency	R_{SJ-hf}	-	-	0.05	UI p-p	-
Total jitter (does not include sinusoidal jitter)	R_{Tj}	-	-	0.60	UI p-p	-

Notes:
1. The jitter (R_{CBHPJ}) and amplitude have to be correlated, for example, by a PCB trace.
2. For recommended operating conditions, see Table 4.

The sinusoidal jitter may have any amplitude and frequency in the unshaded region of this figure.

Figure 18. QSGMII single-frequency sinusoidal jitter limits



3.11.3 XFI interface

This section describes the XFI clocking requirements and its DC and AC electrical characteristics.

3.11.3.1 XFI clocking requirements for SD*n*_REF_CLK*n*_P and SD*n*_REF_CLK*n*_N

Only SerDes 1 (SD1_REF_CLK[1:2]_P and SD1_REF_CLK[1:2]_N) may be used for SerDes XFI configurations based on the RCW configuration field SRDS_PRTCL.

For more information on these specifications, see SerDes reference clocks.

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3.11.3.2 XFI DC electrical characteristics

This section describes the DC electrical characteristics for XFI.

3.11.3.2.1 XFI transmitter DC electrical characteristics

This table defines the XFI transmitter DC electrical characteristics.

Table 39. XFI transmitter DC electrical characteristics (XV_{DD} = 1.35 V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Output differential voltage	$V_{TX-DIFF}$	360	-	770	mV	- LNmTECR 0[AMP_RED]= 0b000111
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-1.14dB}$	0.6	1.1	1.6	dB	- LNmTECR 0[RATIO_PST1Q]=0b0 0011
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-3.5dB}$	3	3.5	4	dB	- LNmTECR 0[RATIO_PST1Q]=0b0 1000
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-4.66dB}$	4.1	4.6	5.1	dB	- LNmTECR 0[RATIO_PST1Q]=0b0 1010
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	- LNmTECR 0[RATIO_PST1Q]=0b0 1100
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-9.5dB}$	9	9.5	10	dB	- LNmTECR 0[RATIO_PST1Q]=0b1 0000
Differential resistance	T_{RD}	80	100	120	Ω	-

Notes:
1. For recommended operating conditions, see Table 4.

3.11.3.2.2 XFI receiver DC electrical characteristics

This table defines the XFI receiver DC electrical characteristics.

Table 40. XFI receiver DC electrical characteristics [2]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input differential voltage	$V_{RX-DIFF}$	110	-	1050	mV	1
Differential resistance	R_{RD}	80	100	120	Ω	-

1. Measured at receiver
2. For recommended operating conditions, see Table 4.

3.11.3.3 XFI AC timing specifications

This section describes the AC timing specifications for XFI.

3.11.3.3.1 XFI transmitter AC timing specifications

This table defines the XFI transmitter AC timing specifications. RefClk jitter is not included.

Table 41. XFI transmitter AC timing specifications[1]

Parameter	Symbol	Min	Typical	Max	Unit
Transmitter baud rate	T_{BAUD}	10.3125 - 100ppm	10.3125	10.3125 + 100ppm	Gb/s
Unit Interval	UI	-	96.96	-	ps
Deterministic jitter	D_J	-	-	0.15	UI p-p
Total jitter	T_J	-	-	0.30	UI p-p

Note:

1. For recommended operating conditions, see Table 4.

3.11.3.3.2 XFI receiver AC timing specifications

This table defines the XFI receiver AC timing specifications. RefClk jitter is not included.

Table 42. XFI receiver AC timing specifications[3]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Receiver baud rate	R_{BAUD}	10.3125 - 100ppm	10.3125	10.3125 + 100ppm	Gb/s	-
Unit Interval	UI	-	96.96	-	ps	-
Total non-EQJ jitter	T_{NON-}	-	-	0.45	UI p-p	1
Total jitter tolerance	T_J	-	-	0.65	UI p-p	1, 2

Notes:

1. The total jitter (T_J) consists of Random Jitter (R_J), Duty Cycle Distortion (DCD), Periodic Jitter (P_J), and Inter symbol Interference (ISI). Non-EQJ jitter can include duty cycle distortion (DCD), random jitter (R_J), and periodic jitter (P_J). Non-EQJ jitter is uncorrelated to the primary data stream with exception of the DCD and so cannot be equalized by the receiver under test. It can exhibit a wide spectrum. Non - EQJ = T_J - ISI = R_J + DCD + P_J
2. The XFI channel has a loss budget of 9.6 dB @5.5GHz. The channel loss including connector @ 5.5GHz is 6dB. The channel crosstalk and reflection margin is 3.6dB. Manual tuning of TX Equalization and amplitude will be required for performance optimization.
3. For recommended operating conditions, see Table 4.

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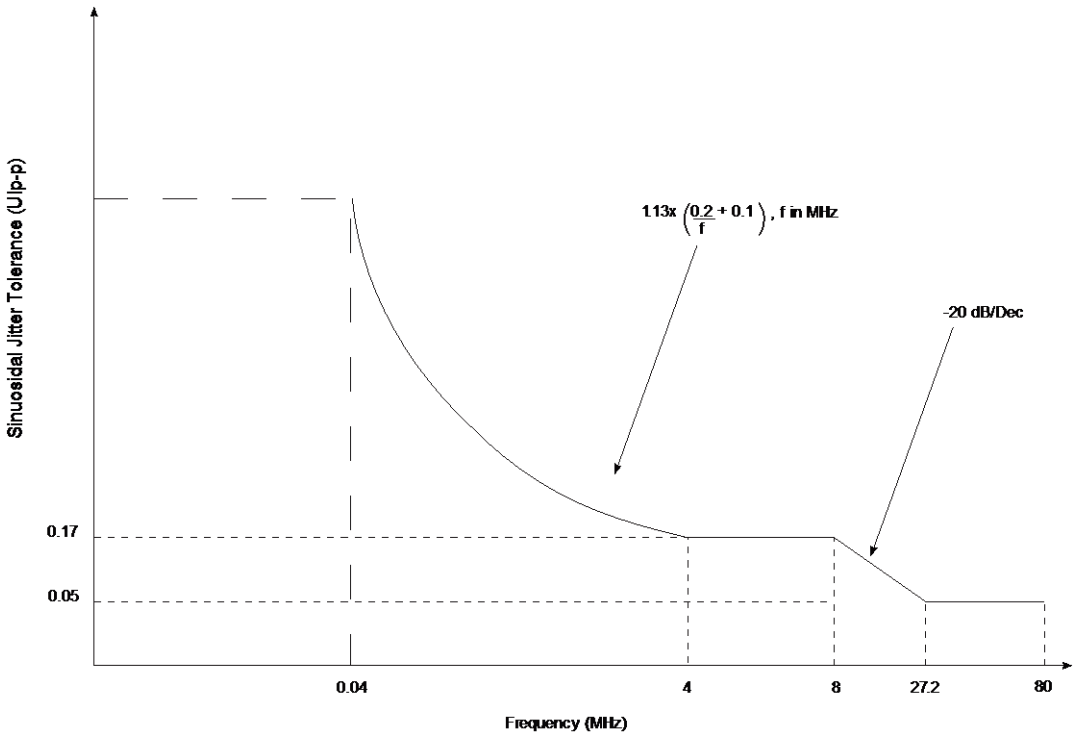
This figure shows the sinusoidal jitter tolerance of XFI receiver.

Figure 19. XFI host receiver input sinusoidal jitter tolerance



3.11.4 10GBase-KR interface

This section describes the 10GBase-KR clocking requirements and its DC and AC electrical characteristics.

3.11.4.1 10GBase-KR clocking requirements for SD*n*_REF_CLK*n*_P and SD*n*_REF_CLK*n*_N

Only SerDes 1 (SD1_REF_CLK1_P and SD1_REF_CLK1_N) may be used for SerDes 10GBase-KR configurations based on the RCW Configuration field SRDS_PRTCL.

For more information on these specifications, see SerDes reference clocks.

3.11.4.2 10GBase-KR DC electrical characteristics

This section describes the DC electrical characteristics for 10GBase-KR.

3.11.4.2.1 10GBase-KR transmitter DC electrical characteristics

This table defines the 10GBase-KR transmitter DC electrical characteristics.

Table 43. 10GBaseKR transmitter DC electrical characteristics (XV_{DD} = 1.35 V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Output differential voltage	$V_{TX-DIFF}$	800	-	1200	mV	- LNmTECR 0[AMP_RE D]= 0b000000
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-1.14dB}$	0.6	1.1	1.6	dB	- LNmTECR 0[RATIO_P ST1Q]=0b0 0011
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-3.5dB}$	3	3.5	4	dB	- LNmTECR 0[RATIO_P ST1Q]=0b0 1000
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-4.66dB}$	4.1	4.6	5.1	dB	- LNmTECR 0[RATIO_P ST1Q]=0b0 1010
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	- LNmTECR 0[RATIO_P ST1Q]=0b0 1100
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-9.5dB}$	9	9.5	10	dB	- LNmTECR 0[RATIO_P ST1Q]=0b1 0000
Differential resistance	T_{RD}	80	100	120	Ω	-

1. For recommended operating conditions, see Table 4.

3.11.4.2.2 10GBase-KR receiver DC electrical characteristics

This table defines the 10GBase-KR receiver DC electrical characteristics.

Table 44. 10GBase-KR receiver DC electrical characteristics[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input differential voltage	$V_{RX-DIFF}$	-	-	1200	mV	-
Differential resistance	R_{RD}	80	-	120	Ω	-

1. For recommended operating conditions, see Table 4.

3.11.4.3 10GBase-KR AC timing specifications

This section describes the AC timing specifications for 10GBase-KR.

3.11.4.3.1 10GBase-KR transmitter AC timing specifications

This table defines the 10GBase-KR transmitter AC timing specifications. RefClk jitter is not included.

Table 45. 10GBase-KR transmitter AC timing specifications[1]

Parameter	Symbol	Min	Typical	Max	Unit
Transmitter baud rate	T_{BAUD}	10.3125 – 100 ppm	10.3125	10.3125 + 100 ppm	Gb/s
Uncorrelated high probability jitter/Random jitter	U_{HPJ}/R_J	-	-	0.15	UI p-p
Deterministic jitter	D_J	-	-	0.15	UI p-p
Total jitter	T_J	-	-	0.30	UI p-p

1. For recommended operating conditions, see Table 4.

3.11.4.3.2 10GBase-KR receiver AC timing specifications

This table defines the 10GBase-KR receiver AC timing specifications. RefClk jitter is not included.

Table 46. 10GBase-KR receiver AC timing specifications[2]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Receiver baud rate	R_{BAUD}	10.3125 – 100 ppm	10.3125	10.3125 + 100 ppm	Gb/s	-
Random jitter	R_J	-	-	0.130	UI p-p	-
Sinusodial jitter, maximum	S_{J-max}	-	-	0.115	UI p-p	-
Duty cycle distortion	D_{CD}	-	-	0.035	UI p-p	-
Total jitter	T_J	-	-	See Note 1	UI p-p	1

1. The total jitter (T_J) is per Interference tolerance test IEEE Standard 802.3ap-2007 specified in Annex 69A.
2. For recommended operating conditions, see Table 4.

3.11.5 1000Base-KX interface

This section discusses the electrical characteristics for the 1000Base-KX. Only AC- coupled operation is supported.

3.11.5.1 1000Base-KX DC electrical characteristics

3.11.5.1.1 1000Base-KX Transmitter DC Specifications

This table describes the 1000Base-KX SerDes transmitter DC specification at TP1 per IEEE Std 802.3ap-2007. Transmitter DC characteristics are measured at the transmitter outputs (SD*n*_TXn_P and SD*n*_TXn_N).

Table 47. 1000Base-KX Transmitter DC Specifications

Parameter	Symbols	Min	Typ	Max	Units	Notes
Output differential voltage	$V_{TX-DIFFp-p}$	800	-	1600	mV	1
Differential resistance	T_{RD}	80	100	120	ohm	-

Notes:
1. SRDSxLNmTECR0[AMP_RED]=00_0000.
2. For recommended operating conditions, see Table 4.

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3.11.5.1.2 1000Base-KX Receiver DC Specifications

This table provides the 1000Base-KX receiver DC timing specifications.

Table 48. 1000Base-KX Receiver DC Specifications

Parameter	Symbols	Min	Typical	Max	Units	Notes
Input differential voltage	$V_{RX-DIFFp-p}$	-	-	1600	mV	1
Differential resistance	T_{RDIN}	80	-	120	ohm	-

Notes:

1. For recommended operating conditions, see Table 4.

3.11.5.2 1000Base-KX AC electrical characteristics

3.11.5.2.1 1000Base-KX Transmitter AC Specifications

This table provides the 1000Base-KX transmitter AC specification.

Table 49. 1000Base-KX Transmitter AC Specifications

Parameter	Symbols	Min	Typical	Max	Units	Notes
Baud Rate	T_{BAUD}	1.25-100ppm	1.25	1.25+100ppm	Gb/s	-
Uncorrelated High Probability Jitter/ Random Jitter	$T_{UHPJ}T_{RJ}$	-	-	0.15	UI p-p	-
Deterministic Jitter	T_{DJ}	-	-	0.10	UI p-p	-
Total Jitter	T_{TJ}	-	-	0.25	UI p-p	1

Notes:

1. Total jitter is specified at a BER of 10^{-12}.
2. For recommended operating conditions, see Table 4.

3.11.5.2.2 1000Base-KX Receiver AC Specifications

This table provides the 1000Base-KX receiver AC specification with parameters guided by IEEE Std 802.3ap-2007.

Table 50. 1000Base-KX Receiver AC Specifications

Parameter	Symbols	Min	Typical	Max	Units	Notes
Receiver Baud Rate	T_{BAUD}	1.25-100ppm	1.25	1.25+100ppm	Gb/s	-
Random Jitter	R_{RJ}	-	-	0.15	UI p-p	1
Sinusoidal Jitter, maximum	R_{SJ-max}	-	-	0.10	UI p-p	2
Total Jitter	R_{TJ}	-	-	See Note 3	UI p-p	2

Notes:

1. Random jitter is specified at a BER of 10^{-12}.
2. The receiver interference tolerance level of this parameter shall be measured as described in Annex 69A of the IEEE Std 802.3ap-2007.
3. Per IEEE 802.3ap-clause 70.
4. The AC specifications do not include Refclk jitter.
5. For recommended operating conditions, see Table 4.

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3.11.6 RGMII electrical specifications

This section describes the electrical characteristics for the RGMII interface.

3.11.6.1 RGMII DC electrical characteristics

This table provides the DC electrical characteristics for the RGMII interface at LV_{DD} = 2.5 V.

Table 51. RGMII DC electrical characteristics (LV_{DD} = 2.5 V)[3]

Parameters	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x LV_{DD}	–	V	1
Input low voltage	V_{IL}	–	0.2 x LV_{DD}	V	1
Input current (LV_{IN}=0 V or LV_{IN}= LV_{DD})	I_{IH}	–	±50	µA	2
Output high voltage (LV_{DD} = min,I_{OH} = -1.0 mA)	V_{OH}	2.00	–	V	
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	–	0.4	V	

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 4.
2. The symbol LV_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 4.
3. For recommended operating conditions, see Table 4.

This table provides the DC electrical characteristics for the RGMII interface at LV_{DD} = 1.8 V.

Table 52. RGMII DC electrical characteristics (LV_{DD} = 1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x LV_{DD}	–	V	1
Input low voltage	V_{IL}	–	0.2 x LV_{DD}	V	1
Input current (LV_{IN} = 0 V or LV_{IN}= LV_{DD})	I_{IN}	–	±50	µA	2
Output high voltage (LV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	–	V	
Output low voltage (LV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	–	0.4	V	

Notes:
1. The min V_{IL} and max V_{IH} values are based on the min and max LV_{IN} values found in Table 4.
2. The symbol LV_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 4.
3. For recommended operating conditions, see Table 4.

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3.11.6.2 RGMII AC timing specifications

This table provides the RGMII AC timing specifications.

Table 53. RGMII AC timing specifications (LV_{DD} = 2.5 /1.8 V)[8]

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
Data to clock output skew (at transmitter)	t_{SKRGT_TX}	-500	0	500	ps	7
Data to clock input skew (at receiver)	t_{SKRGT_RX}	1.0	–	2.6	ns	2, 9
Clock period duration	t_{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40	50	60	%	3, 4
Duty cycle for Gigabit	t_{RGTH}/t_{RGT}	45	50	55	%	–
Rise time (20%-80%)	t_{RGTR}	–	–	– 0.75	ns	5, 6
Fall time (20%-80%)	t_{RGTF}	–	–	– 0.75	ns	5, 6

Notes:

1. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII timing. Note that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal. Many PHY vendors already incorporate the necessary delay inside their device. If so, additional PCB delay is probably not needed.
3. For 10 Mbps and 100 Mbps, tRGT scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Applies to inputs and outputs.
6. The system/board must be designed to ensure this input requirement to the chip is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.
7. The frequency of ECn_RX_CLK (input) should not exceed the frequency of ECn_GTX_CLK (output) by more than 300 ppm.
8. For recommended operating conditions, see Table 4.
9. For 10 Mbps and 100 Mbps, the max value is unspecified.

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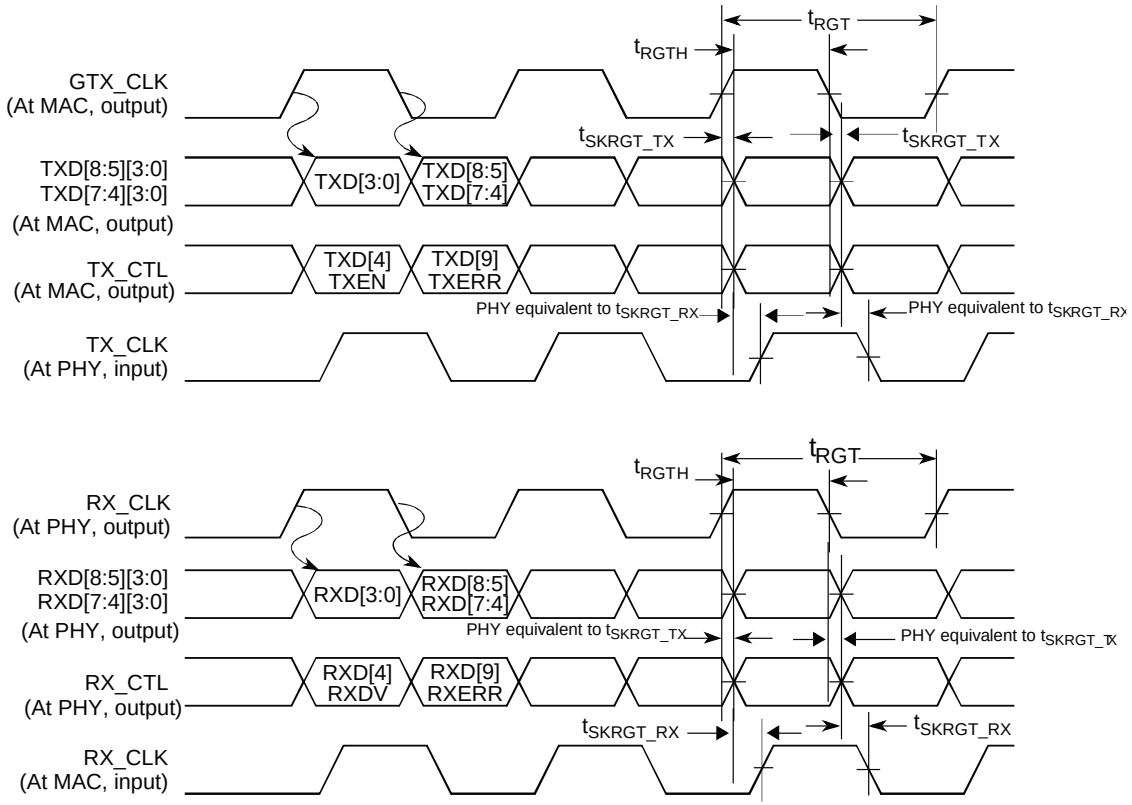
This figure shows the RGMII AC timing and multiplexing diagrams.

Figure 20. RGMII AC timing and multiplexing diagrams



Warning

Teledyne e2v guarantees timings generated from the MAC. Board designers must ensure delays needed at the PHY or the MAC.

3.11.7 Ethernet management interface (EMI)

This section describes the electrical characteristics for the Ethernet Management Interface (EMI) interface.

Both the interfaces (EMI1 and EMI2) interface timing is compatible with IEEE Std 802.3™ clause 22.

3.11.7.1 Ethernet management interface 1 (EMI1)

This section describes the electrical characteristics for the EMI1 interface. The EMI1 interface timing is compatible with IEEE Std 802.3™ clause 22.

3.11.7.1.1 EMI1 DC electrical characteristics

This section describes the DC electrical characteristics for EMI1_MDIO and EMI1_MDC. The pins are available on LV_{DD}. See Table 4 for operating voltages.

This table provides the EMI1 DC electrical characteristics when LV_{DD} = 2.5 V.

Table 54. EMI1 DC electrical characteristics (LV_{DD} = 2.5 V)[3]

Parameters	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x LV_{DD}	–	V	1
Input low voltage	V_{IL}	–	0.2 x LV_{DD}	V	1
Input current (LV_{IN} = 0 or LV_{IN} = LV_{DD})	I_{IN}	–	±50	µA	2
Output high voltage (LV_{DD} = min, I_{OH} = -1.0 mA)	V_{OH}	2.00	–	V	–
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	–	0.40	V	–

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 4.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbols referenced in Table 4.
3. For recommended operating conditions, see Table 4.

This table provides the EMI1 DC electrical characteristics when LV_{DD} = 1.8 V.

Table 55. EMI1 DC electrical characteristics (LV_{DD} = 1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x LV_{DD}	–	V	1
Input low voltage	V_{IL}	–	0.2 x LV_{DD}	V	1
Input current (LV_{IN} = 0 V or LV_{IN} = LV_{DD})	I_{IN}	–	±50	µA	2
Output high voltage (LV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	–	V	
Output low voltage (LV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	–	0.4	V	

Notes:
1. The min V_{IL} and max V_{IH} values are based on the min and max LV_{IN} respective values found in Table 4.
2. The symbol LV_{IN} represents the LV_{IN} symbols referenced in Table 4.
3. For recommended operating conditions, see Table 4.

3.11.7.1.2 EMI1 AC timing specifications

This table provides the EMI1 AC timing specifications.

Table 56. EMI1 AC timing specifications[5]

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	–	–	2.5	MHz	2
MDC clock pulse width high	t_{MDCH}	160	–	–	ns	–
MDC to MDIO delay	t_{MDKHDX}	(Y+5) x t_{enet_clk} - 4	–	(Y+5) x t_{enet_clk} + 4	ns	3
MDIO to MDC setup time	t_{MDDVKH}	8	–	–	ns	
MDIO to MDC hold time	t_{MDDXKH}	2.6	–	–	ns	6

Notes:
1. The symbols used for timing specifications follow these patterns: $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state

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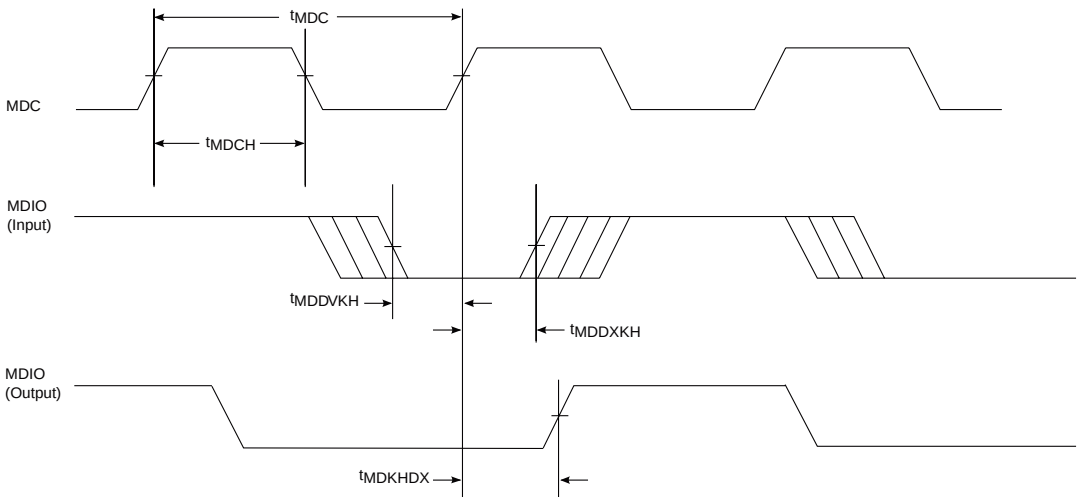
2. (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time.
3. This parameter is dependent on the Ethernet clock frequency. The MDIO_CFG[MDIO_CLK_DIV] field determines the clock frequency of the MgmtClk Clock EC_MDC.
4. Ethernet clock period (t_{enet_clk}) is equal to Frame Manager Clock period (t_{FMAN_clk})
5. Y is the value programmed to adjust hold time by MDIO_CFG[MDIO_HOLD].
6. For recommended operating conditions, see Table 4.
7. See Ethernet A-010717 erratum.

This figure shows the Ethernet management interface 1 timing diagram

Figure 21. Ethernet management interface 1 timing diagram



3.11.7.2 Ethernet management interface 2 (EMI2)

This section describes the electrical characteristics for the EMI2 interface.

The EMI2 interface timing is compatible with IEEE Std 802.3™ clause 45.

3.11.7.2.1 EMI2 DC electrical characteristics

This section describes the DC electrical characteristics for EMI2_MDIO and EMI2_MDC. The pins are available on TV_{DD}. See Table 4 for operating voltages.

This table provides the EMI2 DC electrical characteristics when TV_{DD} = 2.5 V.

Table 57. EMI2 DC electrical characteristics (TV_{DD} = 2.5 V)[4]

Parameters	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x TV_{DD}	–	V	1
Input low voltage	V_{IL}	–	0.2 x TV_{DD}	V	1
Input current (TV_{IN} = 0 or TV_{IN} = TV_{DD})	I_{IN}	–	±50	µA	2, 3
Output high voltage (TV_{DD} = min, I_{OH} = -1.0 mA)	V_{OH}	2.00	–	V	–
Output low voltage (TV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	–	0.4	V	–

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max TV_{IN} values found in Table 4.
2. The symbol V_{IN}, in this case, represents the TV_{IN} symbols referenced in Recommended operating conditions.

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3. The symbol TV_{DD}, in this case, represents the TV_{DD} symbols referenced in Recommended operating conditions.
4. For recommended operating conditions, see Table 4.

This table provides the EMI2 DC electrical characteristics when TV_{DD} = 1.8 V.

Table 58. EMI2 DC electrical characteristics (TV_{DD} = 1.8 V)[4]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x TV_{DD}	–	V	1
Input low voltage	V_{IL}	–	0.2 x TV_{DD}	V	1
Input current (TV_{IN} = 0 V or TV_{IN} = TV_{DD})	I_{IN}	–	±50	µA	2, 3
Output high voltage (TV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	–	V	3
Output low voltage (TV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	–	0.4	V	3

Notes:
1. The min V_{IL} and max V_{IH} values are based on the min and max TV_{IN} respective values found in Table 4.
2. The symbol TV_{IN} represents the TV_{IN} symbols referenced in Recommended operating conditions.
3. The symbol TV_{DD}, in this case, represents the TV_{DD} symbols referenced in Recommended operating conditions.
4. For recommended operating conditions, see Table 4.

This table provides the EMI2 DC electrical characteristics when TV_{DD} = 1.2 V.

Table 59. EMI2 DC electrical characteristics (TV_{DD} = 1.2 V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x TV_{DD}	–	V	–
Input low voltage	V_{IL}	–	0.2 x TV_{DD}	V	–
Output low current (V_{OL} = 0.2 V)	I_{OL}	4		mA	–
Output high voltage (TV_{DD} = min, I_{OH} = -100uA)	V_{OH}	1.0	–	V	–
Output low voltage (TV_{DD} = min, I_{OL} = 100 uA)	V_{OL}	–	0.2	V	–
Input Capacitance	C_{IN}	–	10	pF	–

Notes:
1. For recommended operating conditions, see Table 4.

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3.11.7.2.2 EMI2 AC timing specifications

This table provides the EMI2 AC timing specifications.

Table 60. EMI2 AC timing specifications[6]

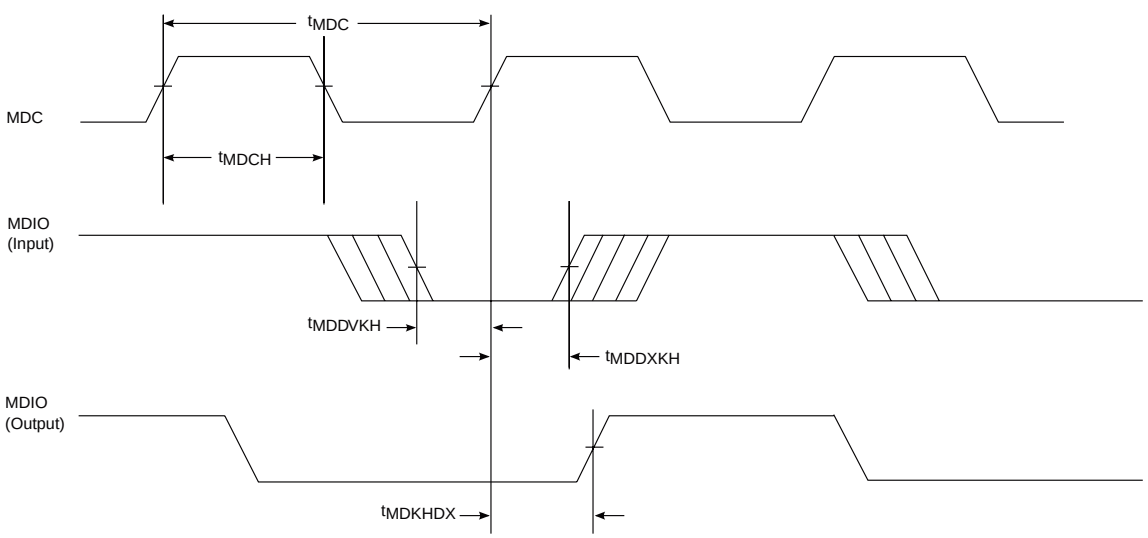
Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	–	–	2.5	MHz	2
MDC clock pulse width high	t_{MDCH}	160	–	–	ns	–
MDC to MDIO delay	t_{MDKHDX}	(Y+5) x t_{enet_clk} - 25	–	(Y+5) x t_{enet_clk}) + 25	ns	3, 4
MDIO to MDC setup time	t_{MDDVKH}	36	–	–	ns	5
MDIO to MDC hold time (TV_{DD}=1.2V)	t_{MDDXKH}	2.6	–	–	ns	7
MDIO to MDC hold time (TV_{DD}=1.8V / 2.5V)	t_{MDDXKH}	1.1	–	–	ns	7

Notes:

1. The symbols used for timing specifications follow these patterns: $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state
2. (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time.
3. This parameter is dependent on the Ethernet clock frequency. The MDIO_CFG [MDIO_CLK_DIV] field determines the clock frequency of the MgmtClk Clock EC_MDC.
4. Ethernet clock period (tenet_clk) is equal to Frame Manager Clock period (tFMAN_clk)
5. Y is the value programmed to adjust hold time by MDIO_CFG[MDIO_HOLD].
6. The setup time tMDDVKH is measured at following load conditions
7. For MDC = 65 pf and for MDIO =75 pf @1.2 V open drain configuration
8. For recommended operating conditions, see Table 4.
9. See Ethernet A-010717 erratum.

This figure shows the Ethernet management interface 2 timing diagram

Figure 22. Ethernet management interface 2 timing diagram



3.11.8 IEEE 1588 electrical specifications

3.11.8.1 IEEE 1588 DC electrical characteristics

This table provides the IEEE 1588 DC electrical characteristics when operating at LV_{DD} = 2.5 V supply.

Table 61. IEEE 1588 DC electrical characteristics(LV_{DD} = 2.5 V)[3]

Parameters	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x LV_{DD}	–	V	1
Input low voltage	V_{IL}	–	0.2 x LV_{DD}	V	1
Input current (LV_{IN}= 0 V or LV_{IN}= LV_{DD})	I_{IH}	–	±50	µA	2
Output high voltage (LV_{DD} = min, I_{OH} = -1.0 mA)	V_{OH}	2.00	–	V	–
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	–	0.40	V	–

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 4.
2. The symbol LV_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 4.
3. For recommended operating conditions, see Table 4.

This table provides the IEEE 1588 DC electrical characteristics when operating at LV_{DD} = 1.8 V supply.

Table 62. IEEE 1588 DC electrical characteristics(LV_{DD} = 1.8 V)[3]

Parameters	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x LV_{DD}	–	V	1
Input low voltage	V_{IL}	–	0.2 x LV_{DD}	V	1
Input current (LV_{IN}= 0 V or LV_{IN}= LV_{DD})	I_{IH}	–	±50	µA	2
Output high voltage (LV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	–	V	–
Output low voltage (LV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	–	0.40	V	–

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 4.
2. The symbol LV_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 4.
3. For recommended operating conditions, see Table 4.

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3.11.8.2 IEEE 1588 AC timing specifications

This table provides the IEEE 1588 AC timing specifications.

Table 63. IEEE 1588 AC timing specifications[5]

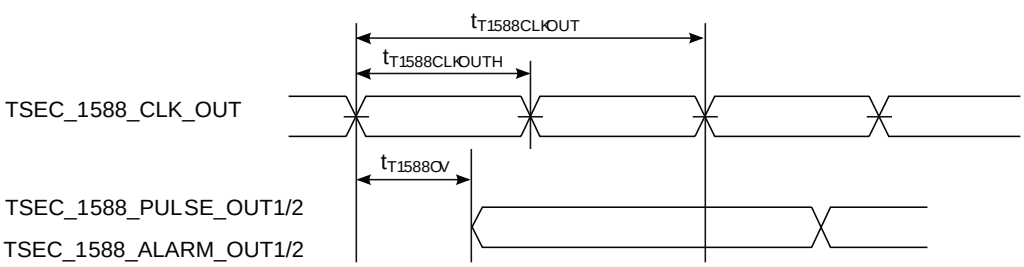
Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
TSEC_1588_CLK_IN clock period	$t_{T1588CLK}$	5.0	–	T_{RX_CLK}	ns	1, 3
TSEC_1588_CLK_IN duty cycle	$t_{T1588CLKH}$/ $t_{T1588CLK}$	40	50	60	%	2
TSEC_1588_CLK_IN peak-to-peak jitter	$t_{T1588CLKINJ}$	–	–	250	ps	–
Rise time TSEC_1588_CLK_IN (20%-80%)	$t_{T1588CLKINR}$	1.0	–	2.0	ns	–
Fall time TSEC_1588_CLK_IN (80%-20%)	$t_{T1588CLKINF}$	1.0	–	2.0	ns	–
TSEC_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	5.0	–	–	ns	4
TSEC_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}$/ $t_{T1588CLKOUT}$	30	50	70	%	–
TSEC_1588_PULSE_OUT1/2, TSEC_1588_ALARM_OUT1/2	$t_{T1588OV}$	0	–	4.0	ns	–
TSEC_1588_TRIG_IN1/2 pulse width	$t_{T1588TRIGH}$	2 x $t_{T1588CLK\_MAX}$	–	–	ns	3

Notes:

1. T_{RX_CLK} is the maximum clock period of the ethernet receiving clock selected by TMR_CTRL[CKSEL]. See the chip reference manual for a description of TMR_CTRL registers.
2. This needs to be at least two times the clock period of the clock selected by TMR_CTRL[CKSEL]. See the chip reference manual for a description of TMR_CTRL registers.
3. The maximum value of $t_{T1588CLK}$ is not only defined by the value of T_{RX_CLK}, but also defined by the recovered clock. For example, for 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ will be 2800, 280, and 56 ns, respectively.
4. There are three input clock sources for 1588: TSEC_1588_CLK_IN, RTC, and MAC clock / 2. When using TSEC_1588_CLK_IN, the minimum clock period is 2 x $t_{T1588CLK}$.
5. For recommended operating conditions, see Table 4.

This figure shows the data and command output AC timing diagram.

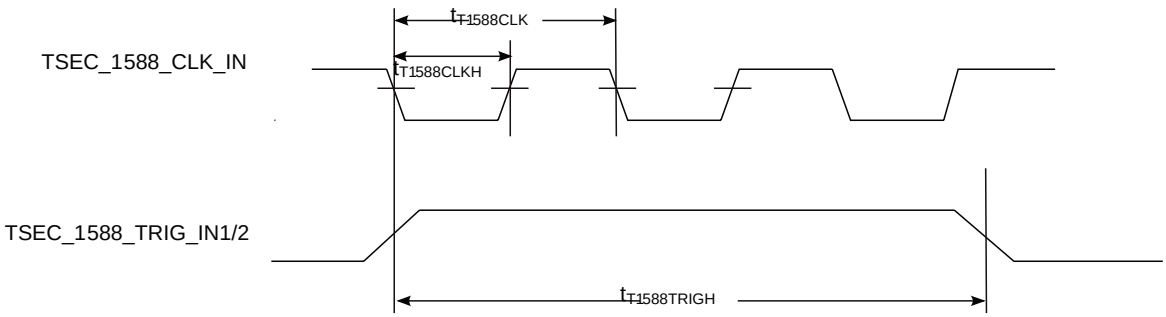
Figure 23. IEEE 1588 output AC timing



Note: The output delay is counted starting at the rising edge if tT1588CLKOUT is non-inverting. Otherwise, it is counted starting at the falling edge.

This figure shows the data and command input AC timing diagram.

Figure 24. IEEE 1588 input AC timing



3.12 USB 3.0 interface

This section describes the DC and AC electrical specifications for the USB 3.0 interface.

3.12.1 USB 3.0 PHY transceiver supply DC voltage

This table provides the DC electrical characteristics for the USB 3.0 interface when operating at USB_HV_{DD} = 3.3 V.

Table 64. USB 3.0 PHY transceiver supply DC voltage (USB_HV_{DD} = 3.3 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	–	V	1
Input low voltage	V_{IL}	–	0.8	V	1
Input current (USB_HV_{IN} = 0 V or USB_HV_{IN}= USB_HV_{DD})	I_{IN}	–	±50	µA	2
Output high voltage (USB_HV_{DD} = min, I_{OH} = -2 mA)	V_{OH}	2.8	–	V	–
Output low voltage (USB_HV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	–	0.3	V	–

Notes:
1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max USB_HV_{IN} values found in Table 4.
2. The symbol USB_HV_{IN}, in this case, represents the USB_HV_{IN} symbol referenced in Table 4.
3. For recommended operating conditions, see Table 4.

3.12.2 USB 3.0 DC electrical characteristics

This table provides the USB 3.0 transmitter DC electrical characteristics at package pins.

Table 65. USB 3.0 transmitter DC electrical characteristics[1]

Characteristic	Symbol	Min	Nom	Max	Unit
Differential output voltage	$V_{tx\text{-}diff\text{-}pp}$	800	1000	1200	$mV_{p\text{-}p}$
Low-power differential output voltage	$V_{tx\text{-}diff\text{-}pp\text{-}low}$	400	–	1200	$mV_{p\text{-}p}$
Tx de-emphasis	$V_{tx\text{-}de\text{-}ratio}$	3	–	4	dB
Differential impedance	Z_{diffTX}	72	100	120	Ohm
Tx common mode impedance	$R_{TX\text{-}DC}$	18	–	30	Ohm
Absolute DC common mode voltage between U1 and U0	$T_{TX\text{-}CM\text{-}DC\text{-}ACTIVEIDLE\text{-}DELTA}$	–	–	200	mV
DC electrical idle differential output voltage	$V_{TX\text{-}IDLE\text{-}DIFF\text{-}DC}$	0	–	10	mV

1. For recommended operating conditions, see Table 4.

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This table provides the USB 3.0 receiver DC electrical characteristics at the Rx package pins.

Table 66. USB 3.0 receiver DC electrical characteristics

Characteristic	Symbol	Min	Nom	Max	Unit	Notes
Differential Rx input impedance	$R_{RX-DIFF-DC}$	72	100	120	Ohm	–
Receiver DC common mode impedance	R_{RX-DC}	18	–	30	Ohm	–
DC input CM input impedance for V > 0 during reset or power down	ZRX- HIGH-IMP- DC	25 K	–	–	Ohm	–
LFPS detect threshold	VRX-IDLE- DET-DC-$DIFF_{pp}$	100	–	300	mV	1

Note:

1. Below the minimum is noise. Must wake up above the maximum.

3.12.3 USB 3.0 AC timing specifications

This table provides the USB 3.0 transmitter AC timing specifications at package pins.

Table 67. USB 3.0 transmitter AC timing specifications[1]

Parameter	Symbol	Min	Nom	Max	Unit	Notes
Speed	–	–	5.0	–	Gb/s	–
Transmitter eye	t_{TX-Eye}	0.625	–	–	UI	–
Unit interval	UI	199.94	–	200.06	ps	2
AC coupling capacitor	AC coupling capacitor	75	–	200	nF	–

Notes:

1. For recommended operating conditions, see Table 4.
2. UI does not account for SSC-caused variations.

This table provides the USB 3.0 receiver AC timing specifications at Rx package pins.

Table 68. USB 3.0 receiver AC timing specifications[1]

Parameter	Symbol	Min	Nom	Max	Unit	Notes
Unit interval	UI	199.94	–	200.06	ps	2

Notes:
1. For recommended operating conditions, see Table 4.
2. UI does not account for SSC-caused variations.

3.12.4 USB 3.0 reference clock requirements

There are two options for the reference clock of USB PHY: SYSCLK or DIFF_SYSCLK/DIFF_SYSCLK_B. For more information, see USB 3.0 reference clock requirements.

3.12.5 USB 3.0 LFPS specifications

This table provides the key LFPS electrical specifications at the transmitter.

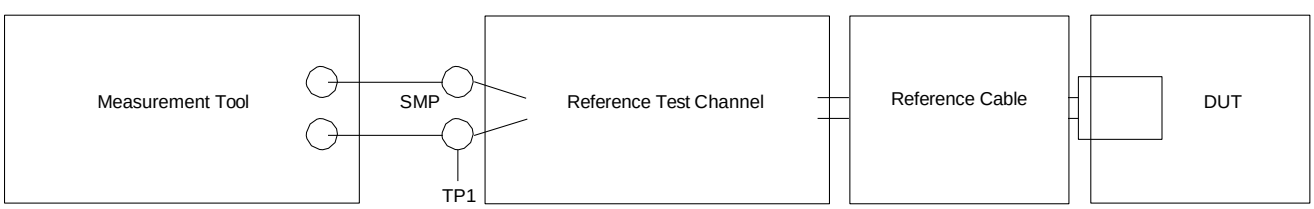
Table 69. LFPS electrical specifications at the transmitter

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Period	t_{Period}	20	–	100	ns	–
Peak-to-peak differential amplitude	$V_{TX-DIFF-PP-LFPS}$	800	–	1200	mV	–
Rise/fall time	$t_{RiseFall20-80}$	–	–	4	ns	1
Duty cycle	Duty cycle	40	–	60	%	1

Note:
1. Measured at compliance TP1. See Figure 25 for details.

This figure shows the transmit normative setup with reference channel as per USB 3.0 specifications.

Figure 25. Transmit normative setup



3.13 Integrated Flash Controller

This section describes the DC and AC electrical specifications for the integrated flash controller.

3.13.1 Integrated Flash Controller DC electrical characteristics

This table provides the DC electrical characteristics for the integrated flash controller.

Table 70. Integrated Flash Controller DC electrical characteristics (1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	1
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	1
Input current	I_{IN}	-	±50	µA	2
(V_{IN} = 0 V or V_{IN} = OV_{DD})					
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.6	-	V	-
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.32	V	-

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 4.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 4.
3. For recommended operating conditions, see Table 4.

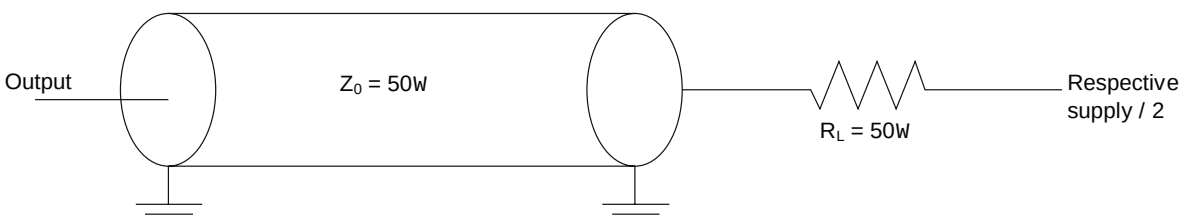
3.13.2 Integrated Flash Controller AC timing specifications

This section describes the AC timing specifications for the integrated flash controller.

3.13.2.1 Test condition

The figure below provides the AC test load for the integrated flash controller.

Figure 26. Integrated Flash Controller AC test load



3.13.2.2 IFC AC timing specifications (GPCM/GASIC)

This table describes the input AC timing specifications for the IFC-GPCM and IFC- GASIC interface.

Table 71. Integrated flash controller input timing specifications for GPCM and GASIC mode (OV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input setup	$t_{IBIVKH1}$	4	-	ns	-
Input hold	$t_{IBIXKH1}$	1	-	ns	-

Note:
1. For recommended operating conditions, see Table 4.

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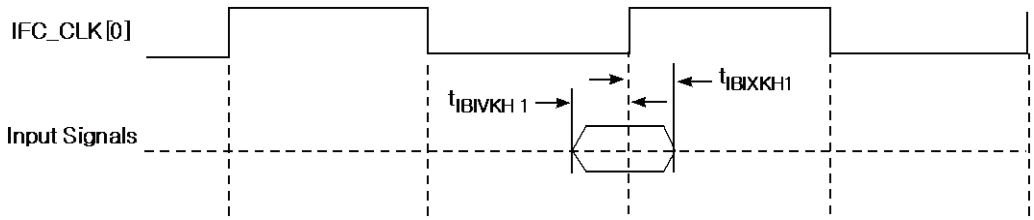
This figure shows the input AC timing diagram for the IFC-GPCM, IFC-GASIC interface.

Figure 27. IFC-GPCM, IFC-GASIC input AC timing specifictions



This table describes the output AC timing specifications for the IFC-GPCM and IFC- GASIC interfaces.

Table 72. Integrated flash controller IFC-GPCM and IFC-GASIC interface output timing specifications (OVDD = 1.8 V) (2)

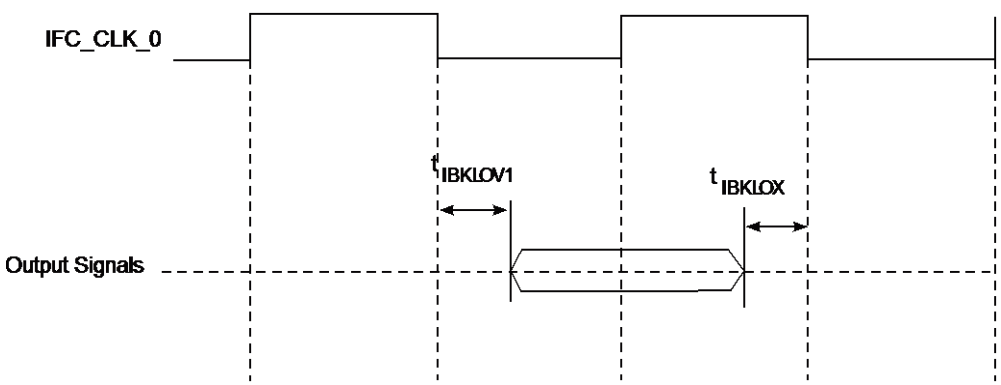
Parameter	Symbol	Min	Max	Unit	Notes
IFC_CLK cycle time	t_{IBK}	10	-	ns	-
IFC_CLK duty cycle	t_{IBKH}/t_{IBK}	45	55	%	-
Output delay	$t_{IBKLOV1}$	-	1.5	ns	-
Output hold	t_{IBKLOX}	-	-2	ns	1
IFC_CLK[0] to IFC_CLK[m] skew	$t_{IBKSKEW}$	0	±75	ps	-

Note:

1. The output hold is negative. This means that output transition happens earlier than the falling edge of IFC_CLK.
2. For recommended operating conditions, see Table 4.

This figure shows the output AC timing diagram for the IFC-GPCM and IFC-GASIC interface.

Figure 28. IFC-GPCM, IFC-GASIC signals



3.13.2.3 IFC AC timing specifications (NOR)

This table describes the input timing specifications for the IFC-NOR interface.

Table 73. Integrated flash controller input timing specifications for NOR mode (OV_{DD} = 1.8 V)[2]

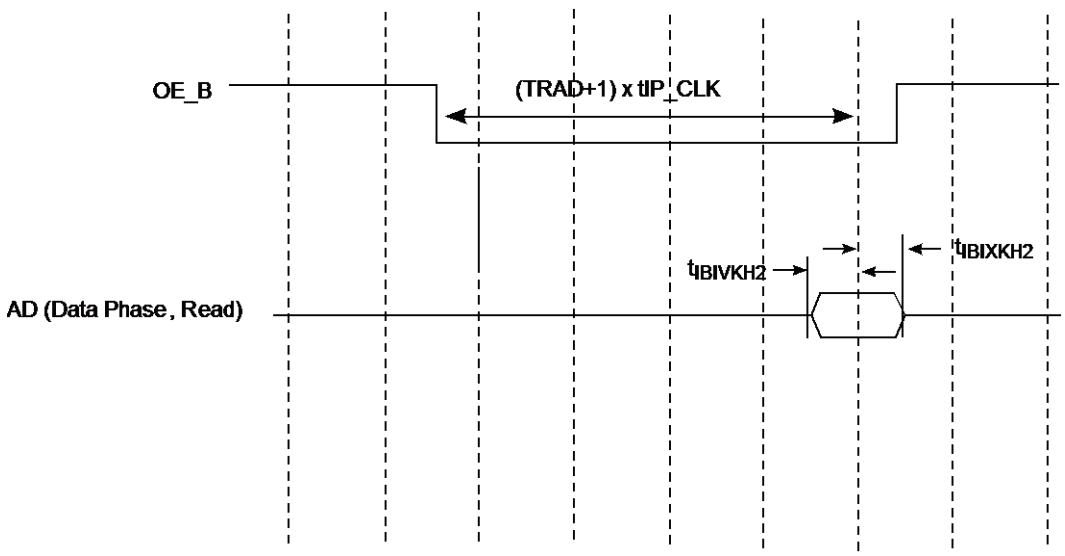
Parameter	Symbol	Min	Max	Unit	Notes
Input setup	$t_{IBIVKH2}$	(2 x t_{IP_CLK}) + 2	-	ns	1
Input hold	$t_{IBIXKH2}$	(1 x t_{IP_CLK}) + 1	-	ns	1

Notes:

1. t_{IP_CLK} is the period of ip clock (not the IFC_CLK) on which IFC is running.
2. For recommended operating conditions, see Table 4.

The figure below shows the AC input timing diagram for input signals for the IFC-NOR interface. Here TRAD is a programmable delay parameter. See the IFC section of the chip reference manual for more information.

Figure 29. IFC-NOR interface input AC timings



This table describes the output AC timing specifications of IFC-NOR interface.

Table 74. Integrated flash controller IFC-NOR interface output timing specifications (OV_{DD} = 1.8 V)[2]

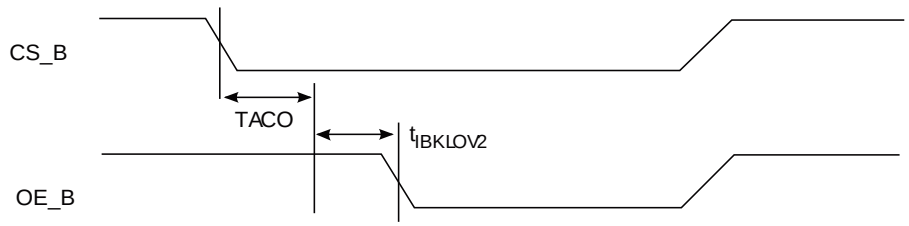
Parameter	Symbol	Min	Max	Unit	Notes
Output delay	$t_{IBKLOV2}$	-	±1.5	ns	1

NOTE:

1. This effectively means that a signal change may appear anywhere within ±$t_{IBKLOV2}$ (max) duration, from the point where it's expected to change.
2. For recommended operating conditions, see Table 4.

The figure below shows the AC timing diagram for IFC-NOR interface output signals. The timing specs have been illustrated here by taking timings between two signals, CS_B and OE_B as an example. In a read operation, OE_B is supposed to change the TACO (a programmable delay; see the IFC section of the chip reference manual for more information) time after CS_B. Because of the skew between the signals, OE_B may change anywhere within the window of time defined by tIBKLOV2. This concept applies to other IFC-NOR interface output signals as well. The diagram is an example that shows the skew between any two chronological toggling signals as per the protocol. The list of IFC-NOR output signals is as follows: NRALE, NRAVD_B, NRWE_B, NROE_B, CS_B, AD (Address phase).

Figure 30. IFC-NOR interface output AC timings



3.13.2.4 IFC AC timing specifications (NAND)

This table describes the input timing specifications of the IFC-NAND interface.

Table 75. Integrated flash controller input timing specifications for NAND mode (OV_{DD} = 1.8 V)[2]

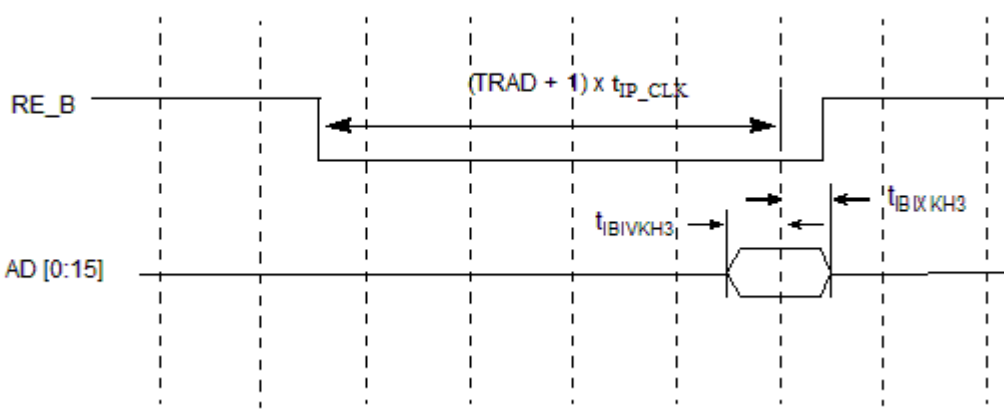
Parameter	Symbol	Min	Max	Unit	Notes
Input setup	$t_{IBIVKH3}$	(2 x t_{IP_CLK}) + 2	-	ns	1
Input hold	$t_{IBIXKH3}$	1	-	ns	1
IFC_RB_B pulse width	t_{IBCH}	2	-	t_{IP_CLK}	1

NOTE:

1. t_{IP_CLK} is the period of ip clock on which IFC is running.
2. For recommended operating conditions, see Table 4.

The figure below shows the AC input timing diagram for input signals of IFC-NAND interface. Here TRAD is a programmable delay parameter. See the IFC section of the chip reference manual for more information.

Figure 31. IFC-NAND interface input AC timings



NOTE

t_{IP_CLK} is the period of ip clock (not the IFC_CLK) on which IFC is running.

This table describes the output AC timing specifications for the IFC-NAND interface.

Table 76. Integrated flash controller IFC-NAND interface output timing specifications (OV_{DD}= 1.8 V)[2]

Parameter	Symbol	Min	Max	Unit	Notes
Output delay	$t_{IBKLOV3}$	-	±1.5	ns	1

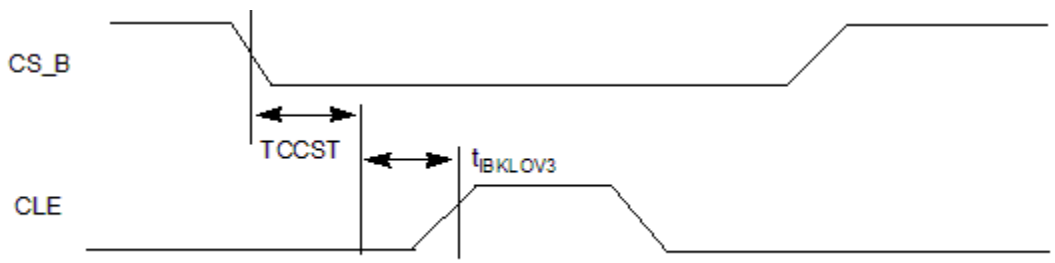
Note:

1. This effectively means that a signal change may appear anywhere within $t_{IBKLOV3}$ (min) to $t_{IBKLOV3}$ (max) duration, from the point where it's expected to change.
2. For recommended operating conditions, see Table 4.

The figure below shows the AC timing diagram for output signals of IFC-NAND interface.The timing specs are shown here by taking the timings between two signals, CS_B and CLE as an example. CLE is supposed to change TCCST (a programmable

delay; see the IFC section of the chip reference manual for more information) time after CS_B. Because of the skew between the signals, CLE may change anywhere within window of time defined by $t_{IBKLOV3}$. This concept applies to other output signals of the IFC-NAND interface as well. The diagram is an example to show the skew between any two chronological toggling signals as per the protocol. The list of output signals is as follows: NDWE_B, NDRE_B, NDALE, WP_B, NDCLE, CS_B, and AD.

Figure 32. IFC-NAND interface output AC timings



3.13.2.5 IFC-NAND SDR AC timing specifications

This table describes the AC timing specifications for the IFC-NAND SDR interface. These specifications are compliant to the SDR mode of the ONFI specification revision 3.0.

Table 77. Integrated flash controller IFC-NAND SDR interface AC timing specifications (OVDD = 1.8 V)

Parameter	Symbol	I/O	Min	Max	Unit	Notes
Address cycle to data loading time	t_{ADL}	O	TADLE - 1500(ps)	TADLE + 1500(ps)	t_{IP_CLK}	Figure 33
ALE hold time	t_{ALH}	O	TWCHT - 1500(ps)	TWCHT + 1500(ps)	t_{IP_CLK}	Figure 34
ALE setup time	t_{ALS}	O	TWP - 1500(ps)	TWP + 1500(ps)	t_{IP_CLK}	Figure 34
ALE to RE_n delay	t_{AR}	O	TWHRE - 1500(ps)	TWHRE + 1500(ps)	t_{IP_CLK}	Figure 35
CE_n hold time	t_{CH}	O	5 + 1500(ps)	-	ns	Figure 34
CE_n high to input hi-Z	t_{CHZ}	I	TRHZ - 1500(ps)	TRHZ + 1500(ps)	t_{IP_CLK}	Figure 36
CLE hold time	t_{CLH}	O	TWCHT - 1500(ps)	TWCHT + 1500(ps)	t_{IP_CLK}	Figure 34
CLE to RE_n delay	t_{CLR}	O	TWHRE - 1500(ps)	TWHRE - 1500(ps)	t_{IP_CLK}	Figure 37

Parameter	Symbol	I/O	Min	Max	Unit	Notes
CLE setup time	t_{CLS}	O	TWP - 1500(ps)	TWP + 1500(ps)	t_{IP_CLK}	Figure 34
CE_n high to input hold	t_{COH}	I	150 - 1500(ps)	-	ns	Figure 36
CE_n setup time	t_{CS}	O	TCS - 1500(ps)	TCS + 1500(ps)	t_{IP_CLK}	Figure 34
Data hold time	t_{DH}	O	TWCHT - 1500(ps)	TWCHT + 1500(ps)	t_{IP_CLK}	Figure 34
Data setup time	t_{DS}	O	TWP - 1500(ps)	TWP + 1500(ps)	t_{IP_CLK}	Figure 34
Busy time for Set Features and Get Features	t_{FEAT}	O	-	FTOCNT	t_{IP_CLK}	Figure 38
Output hi-Z to RE_n low	t_{IR}	O	TWHRE - 1500(ps)	TWHRE + 1500(ps)	t_{IP_CLK}	Figure 39
Interface and Timing Mode Change time	t_{ITC}	O	-	FTOCNT	t_{IP_CLK}	Figure 38
RE_n cycle time	t_{RC}	O	TRP + TREH - 1500(ps)	TRP + TREH + 1500(ps)	t_{IP_CLK}	Figure 36
RE_n access time	t_{REA}	I	-	(TRAD - 1) + 2(ns)	t_{IP_CLK}	Figure 36
RE_n high hold time	t_{REH}	I	TREH	TREH	t_{IP_CLK}	Figure 36
RE_n high to input hold	t_{RHOH}	I	0	-	ns	Figure 36
RE_n high to WE_n low	t_{RHW}	O	100 + 1500(ps)	-	ns	Figure 40
RE_n high to input hi-Z	t_{RHZ}	I	TRHZ - 1500(ps)	TRHZ + 1500(ps)	t_{IP_CLK}	Figure 36
RE_n low to input data hold	t_{RLOH}	I	0	-	ns	Figure 41
RE_n pulse width	t_{RP}	O	TRP	TRP	t_{IP_CLK}	Figure 36
Ready to data input cycle (data only)	t_{RR}	O	TRR - 1500(ps)	TRR + 1500(ps)	t_{IP_CLK}	Figure 36
Device reset time, measured from the falling edge of R/B_n to the rising edge of R/B_n.	t_{RST} (raw NAND)	O	-	FTOCNT	t_{IP_CLK}	Figure 42
Device reset time, measured from the falling edge of R/B_n to the rising edge of R/B_n.	t_{RST2} (EZ NAND)	O	-	FTOCNT	t_{IP_CLK}	Figure 42
(WE_n high or CLK rising edge) to SR[6] low	t_{WB}	O	TWBE + TWH - 1500(ps)	TWBE + TWH + 1500(ps)	t_{IP_CLK}	Figure 34
WE_n cycle time	t_{WC}	O	TWP + TWH	TWP + TWH	t_{IP_CLK}	Figure 43
WE_n high hold time	t_{WH}	O	TWH	TWH	t_{IP_CLK}	Figure 43
Command, address, or data input cycle to data output cycle	t_{WHR}	O	TWHRE + TWH - 1500(ps)	TWHRE + TWH + 1500(ps)	t_{IP_CLK}	Figure 44
WE_n pulse width	t_{WP}	O	TWP	TWP	t_{IP_CLK}	Figure 34
WP_n transition to command cycle	t_{WW}	O	TWW - 1500(ps)	TWW + 1500(ps)	t_{IP_CLK}	Figure 45
Data Input hold	$t_{IBIXKH4}$	I	1	-	t_{IP_CLK}	Figure 46

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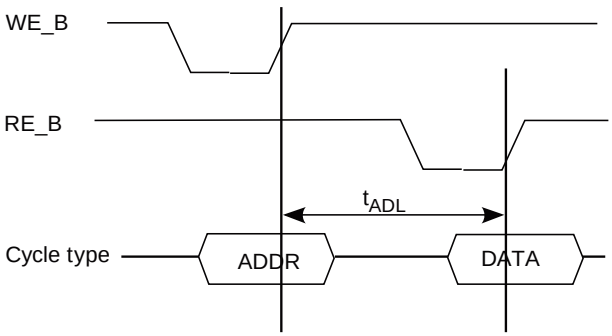
NOTE:

1. t_{IP_CLK} is the clock period of the IP clock (on which the IFC IP is running). Note that the IFC IP clock does not come out of the device.

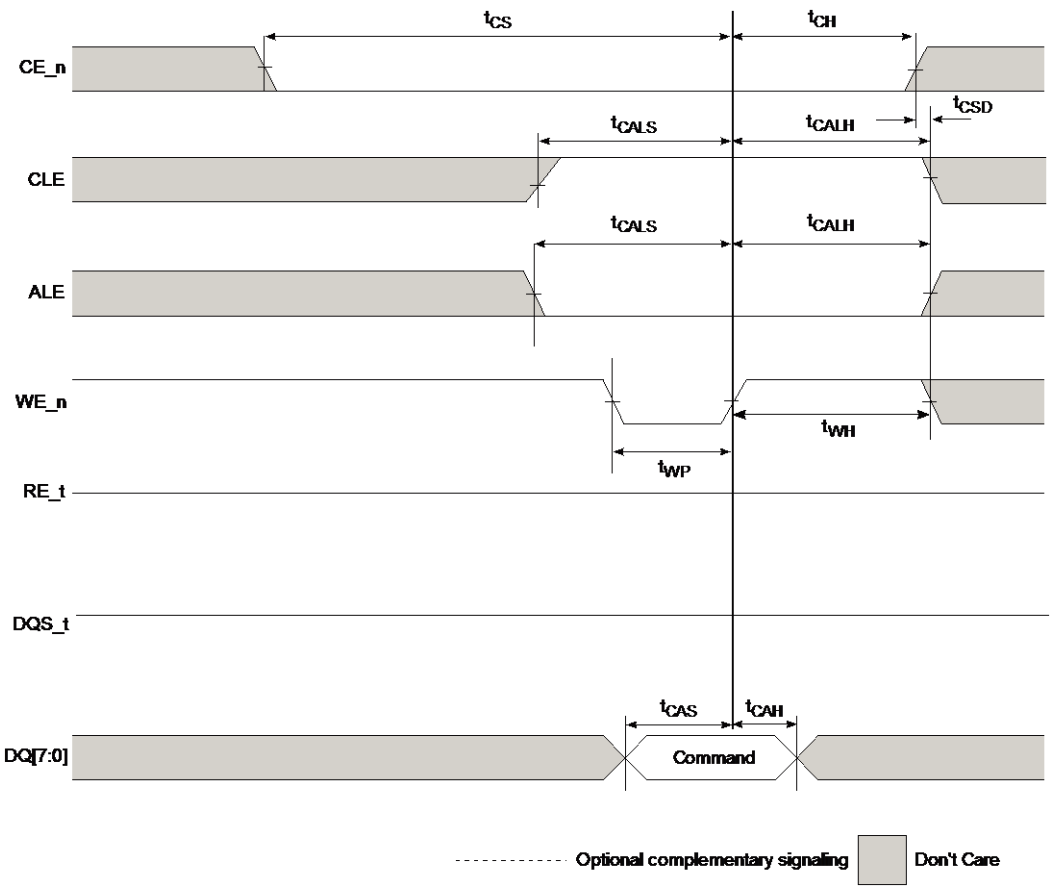
This figure shows the t_{ADL} timing.

Figure 33. t_{ADL} timing



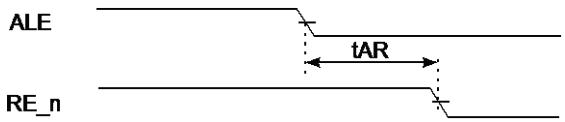
This figure shows the command cycle.

Figure 34. Command cycle



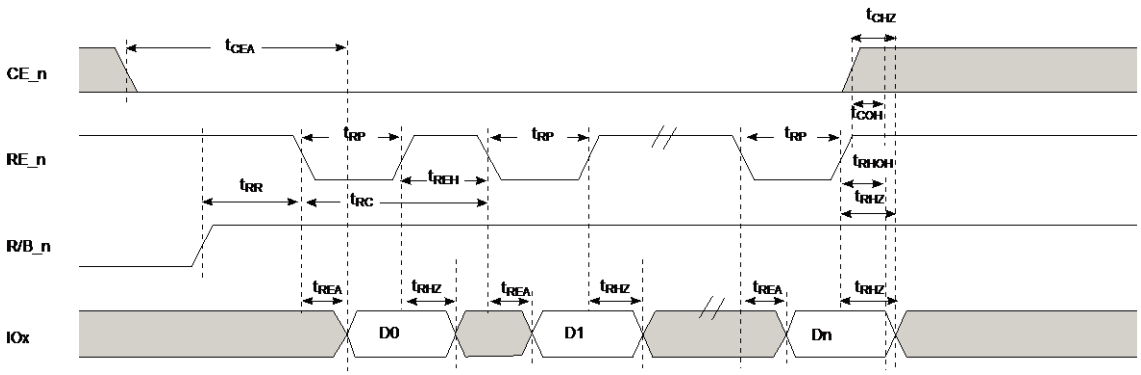
This figure shows the t_{AR} timings.

Figure 35. tAR timings



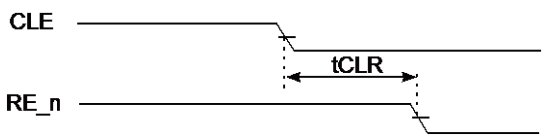
This figure shows the data input cycle timings.

Figure 36. Data input cycle timings



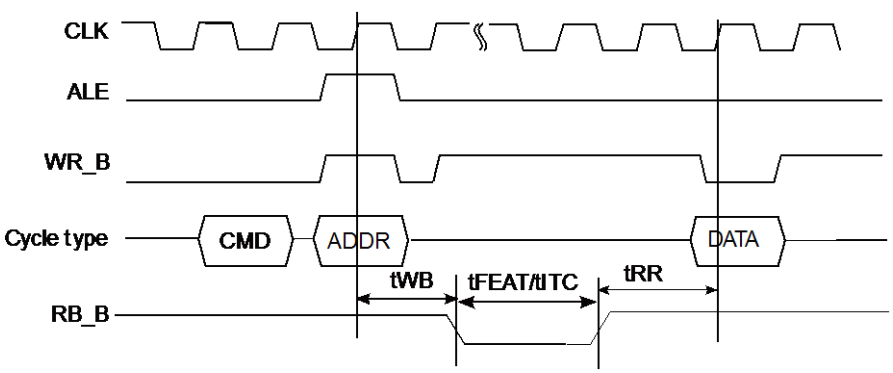
This figure shows the t_{CLR} timings.

Figure 37. tCLR timings



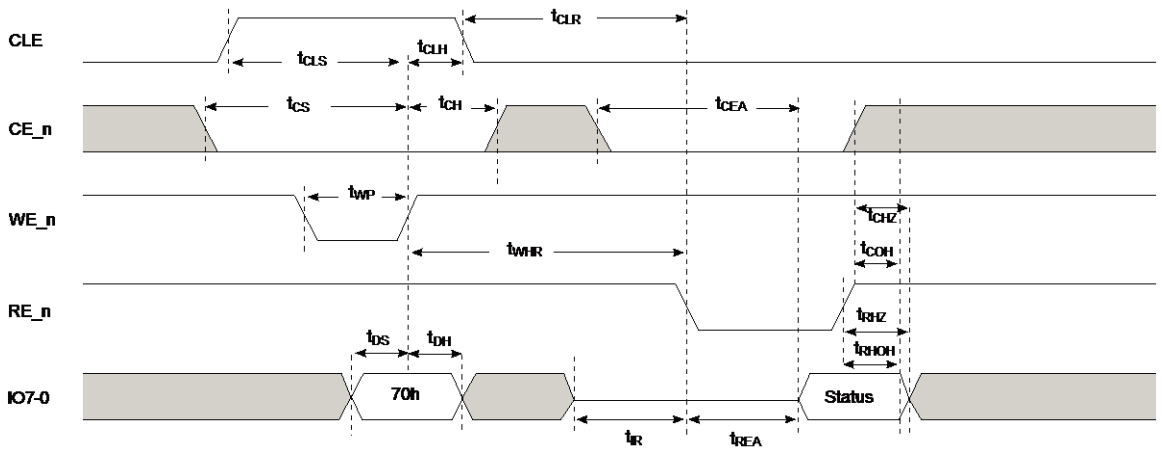
This figure shows the t_{WB}, t_{FEAT}, t_{ITC}, and t_{RR} timings.

Figure 38. t_{WB}, t_{FEAT}, t_{ITC}, and t_{RR} timings



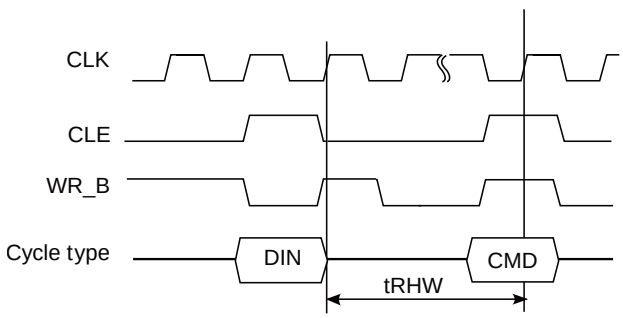
This figure shows the read status timings.

Figure 39. Read status timings



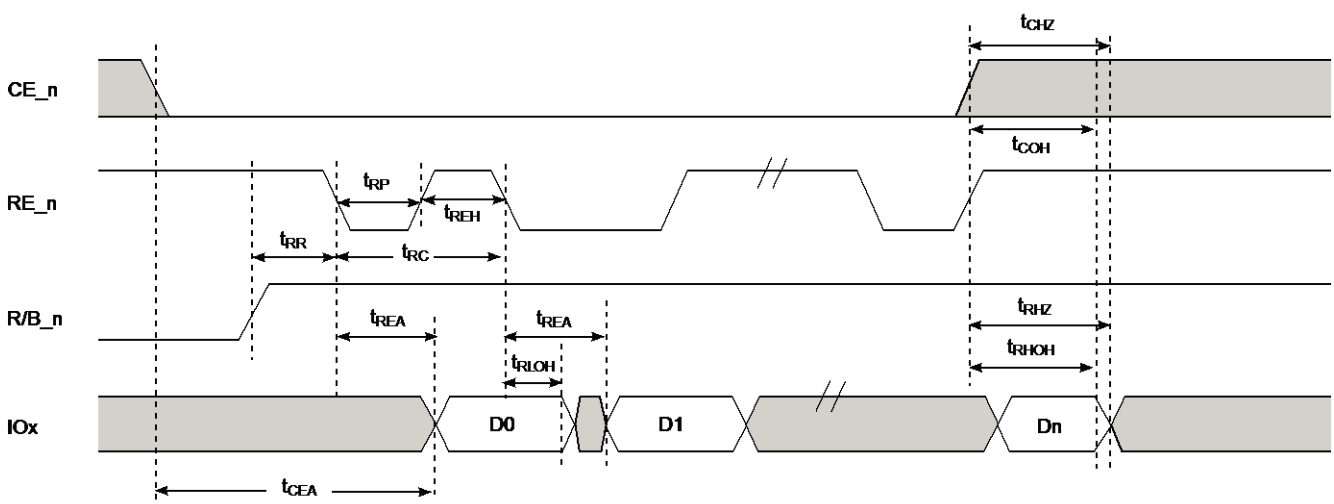
This figure shows the t_{RHW} timings.

Figure 40. t_{RHW} timings



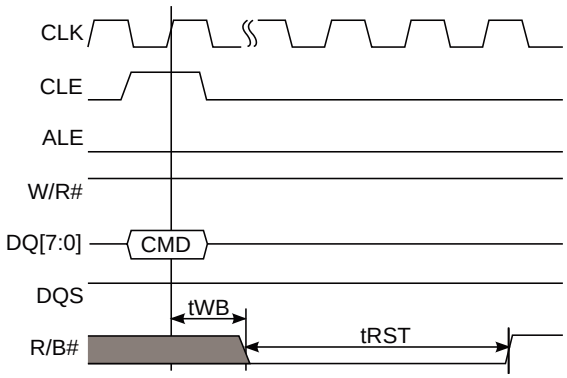
This figure shows the EDO mode data input cycle timings.

Figure 41. EDO mode data input cycle timings



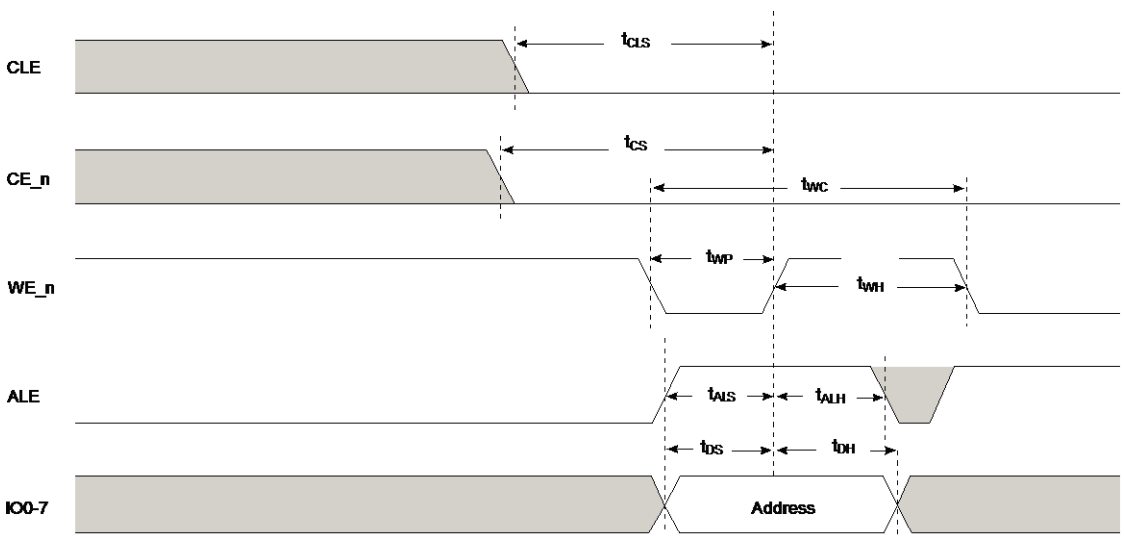
This figure shows the t_{WB} and t_{RST} timings.

Figure 42. t_{WB} and t_{RST} timings



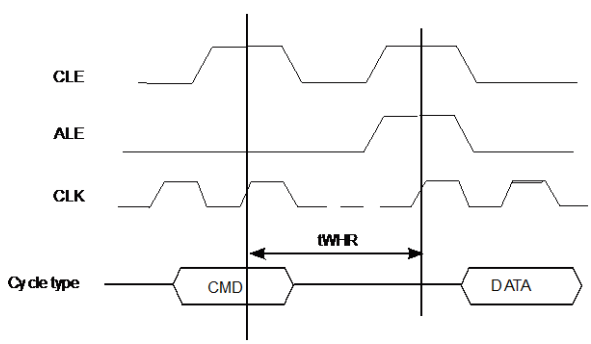
This figure shows the address latch timings.

Figure 43. Address latch timings



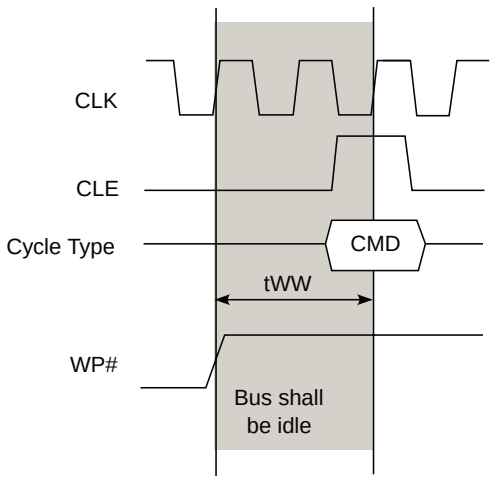
This figure shows the tWHR timings.

Figure 44. t_{WHR} timings



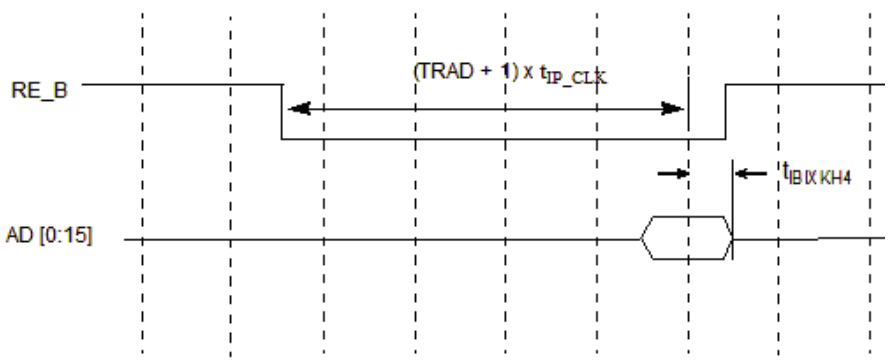
This figure shows the t_{WW} timings.

Figure 45. t_{ww} timings



This figure shows the $t_{IBIXKH4}$ timings.

Figure 46. $t_{IBIXKH4}$ timings



3.13.2.6 IFC-NAND NVDDR AC timing specification

The table below describes the AC timing specifications for the IFC-NAND NVDDR interface. These specifications are compliant to NVDDR mode of ONFI specification revision 3.0.

Table 78. Integrated flash controller IFC-NAND NVDDR interface AC timing specifications (OVDD = 1.8 V)

Parameter	Symbol	I/O	Min	Max	Unit	Notes
Access window of DQ[7:0] from CLK	t_{AC}	I	3 - 150 (ps)	20 + 150 (ps)	ns	Figure 50
Address cycle to data loading time	t_{ADL}	I	TADL	-	t_{IP_CLK}	Figure 51
Command, Address, Data delay (command to command, address to address, command to address, address to command, command/ address to start of data) Fast	tCADf	O	TCAD - 150 (ps)	TCAD + 150 (ps)	t_{IP_CLK}	Figure 47
Command, Address, Data delay (command to command, address to address, command to address, address to command, command/ address to start of data) slow	tCADs	O	TCAD - 150 (ps)	TCAD + 150 (ps)	t_{IP_CLK}	Figure 47
Command/address DQ hold time	t_{CAH}	O	2 + 150 (ps)	-	ns	Figure 47
CLE and ALE hold time	t_{CALH}	O	2 + 150 (ps)	-	ns	Figure 47
CLE and ALE setup time	t_{CALS}	O	2 + 150 (ps)	-	ns	Figure 47
Command/address DQ setup time	t_{CAS}	O	2 + 150 (ps)	-	ns	Figure 47
CE# hold time	t_{CH}	O	2 + 150 (ps)	-	ns	Figure 47
Average clock cycle time, also known as tCK	t_{CK}(avg) or t_{CK}	O	10	-	ns	Figure 47
Absolute clock period, measured from rising edge to the next consecutive rising edge	t_{CK}(abs)	O	tCK(avg) + tJIT(per) min	tCK(avg) + tJIT(per) max	ns	Figure 47
Clock cycle high	t_{CKH}(abs)	O	0.45	0.55	tCK	Figure 47
Clock cycle low	t_{CKL}(abs)	O	0.45	0.55	tCK	Figure 47
Data input end to W/R# high B16	t_{CKWR}	O	TCKWR - 150 (ps)	TCKWR + 150 (ps)	t_{IP_CLK}	Figure 50
CE# setup time	t_{CS}	O	TCS - 150 (ps)	TCS + 150 (ps)	t_{IP_CLK}	Figure 49
Data DQ hold time	t_{DH}	O	1050	-	ps	Figure 49
Access window of DQS from CLK	t_{DQSCK}	I	-	20 + 150 (ps)	ns	Figure 50
W/R# low to DQS/DQ driven by device	t_{DQSD}	I	-150 (ps)	18 + 150 (ps)	ns	Figure 50
DQS output high pulse width	t_{DQSH}	O	0.45	0.55	tCK	Figure 49

Parameter	Symbol	I/O	Min	Max	Unit	Notes
W/R# high to DQS/DQ tri-state by device	t_{DQSHZ}	O	RHZ - 150 (ps)	RHZ + 150 (ps)	t_{IP_CLK}	Figure 47
DQS output low pulse width	t_{DQSL}	O	0.45	0.55	tCK	Figure 49
DQS-DQ skew, DQS to last DQ valid, per access	t_{DQSQ}	I	-	1000	ps	Figure 50
Data output to first DQS latching transition	t_{DQSS}	O	0.75 + 150 (ps)	1.25 - 150 (ps)	tCK	Figure 49
Data DQ setup time	t_{DS}	O	1050	-	ps	Figure 49
DQS falling edge to CLK rising - hold time	t_{DSH}	O	0.2 + 150 (ps)	-	tCK	Figure 49
DQS falling edge to CLK rising - setup time	t_{DSS}	O	0.2 + 150 (ps)	-	tCK	Figure 49
Input data valid window	t_{DVW}	I	tDVW = tQH - tDQSQ	-	ns	Figure 50
Busy time for Set Features and Get Features	t_{FEAT}	I	-	FTOCNT	t_{IP_CLK}	Figure 52
Half-clock period	t_{HP}	O	tHP = min(tCKL, tCKH)	-	ns	Figure 50
Interface and Timing Mode Change time	t_{ITC}	I	-	FTOCNT	t_{IP_CLK}	Figure 52
The deviation of a given tCK(abs) from tCK(avg)	t_{JIT}(per)	O	-0.5	0.5	ns	NA
DQ-DQS hold, DQS to first DQ to go non-valid, per access	t_{QH}	I	tQH = tHP - tQHS	-	t_{IP_CLK}	Figure 50
Data input cycle to command, address, or data output cycle	t_{RHW}	O	TRHW	-	t_{IP_CLK}	Figure 53
Ready to data input cycle (data only)	t_{RR}	I	TRR	-	t_{IP_CLK}	Figure 52
Device reset time, measured from the falling edge of R/B# to the rising edge of R/B#.	t_{RST} (raw NAND)	O	FTOCNT	FTOCNT	t_{IP_CLK}	Figure 54
Device reset time, measured from the falling edge of R/B# to the rising edge of R/B#.	t_{RST2} (EZ NAND)	O	FTOCNT	FTOCNT	t_{IP_CLK}	Figure 54
CLK rising edge to SR[6] low	t_{WB}	O	TWB - 150 (ps)	TWB + 150 (ps)	t_{IP_CLK}	Figure 54
Command, address or data output cycle to data input cycle	t_{WHR}	O	TWHR	-	t_{IP_CLK}	Figure 55
DQS write preamble	t_{WPRE}	O	1.5	-	tCK	Figure 49
DQS write postamble	t_{WPST}	O	1.5	-	tCK	Figure 49

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Parameter	Symbol	I/O	Min	Max	Unit	Notes
W/R# low to data input cycle	t_{WRCK}	I	TWRCK – 150 (ps)	TWRCK + 150 (ps)	t_{IP_CLK}	Figure 50
WP# transition to command cycle	t_{WW}	O	TWW - 150 (ps)	TWW + 150 (ps)	t_{IP_CLK}	Figure 56

Note:

1. t_{IP_CLK} is the clock period of IP clock (on which IFC IP is running). Note that the IFC IP clock does not come out of device.

The following diagrams show the AC timing for the IFC-NAND NVDDR interface.

Figure 47. Command cycle

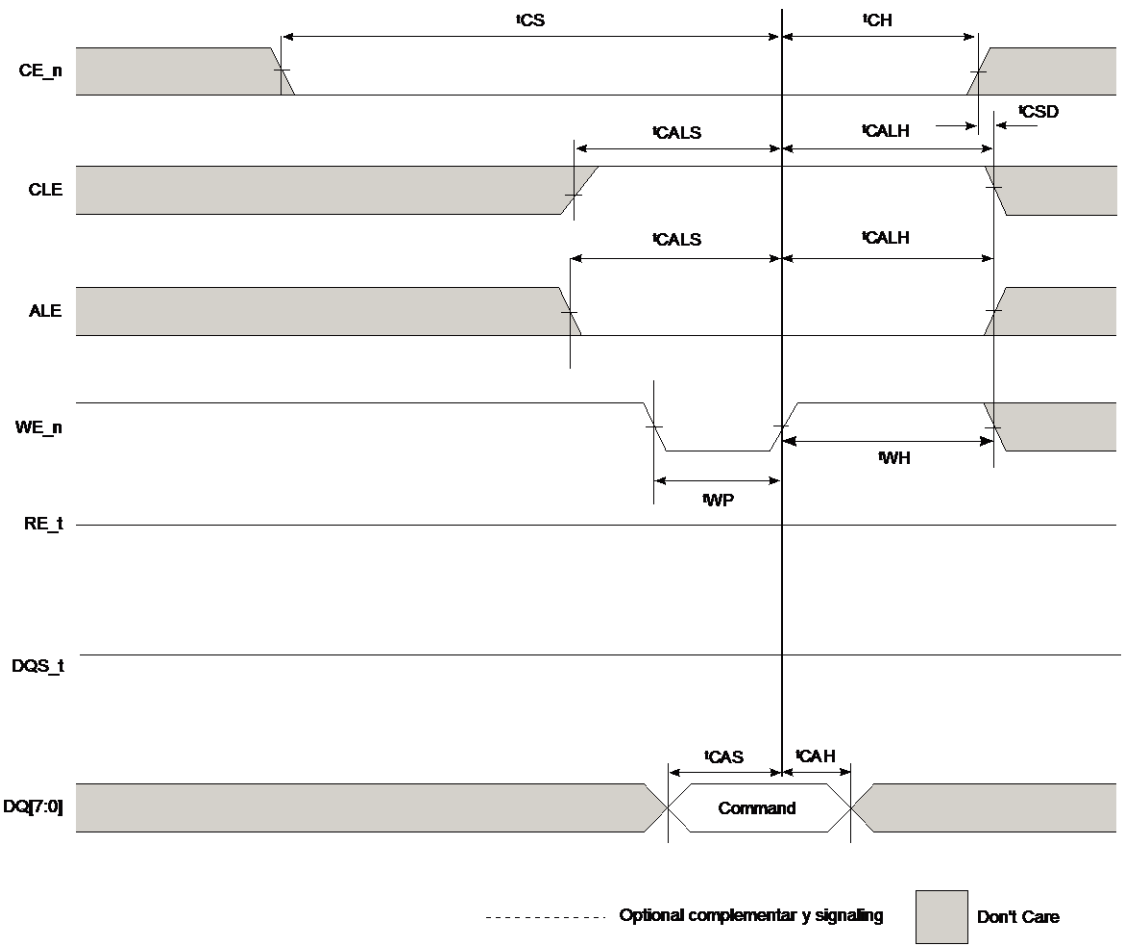


Figure 48. Address cycle

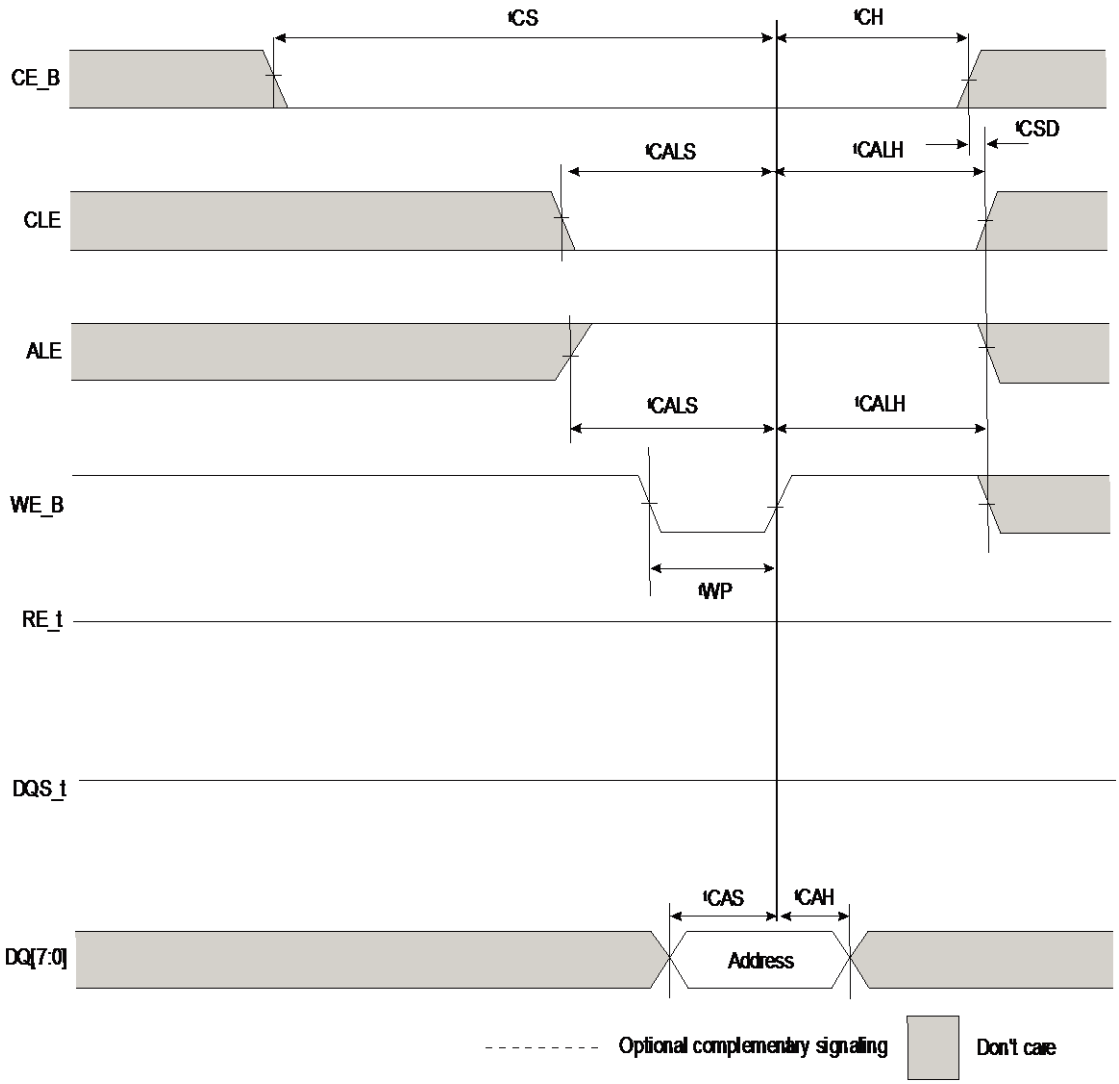


Figure 49. Write cycle

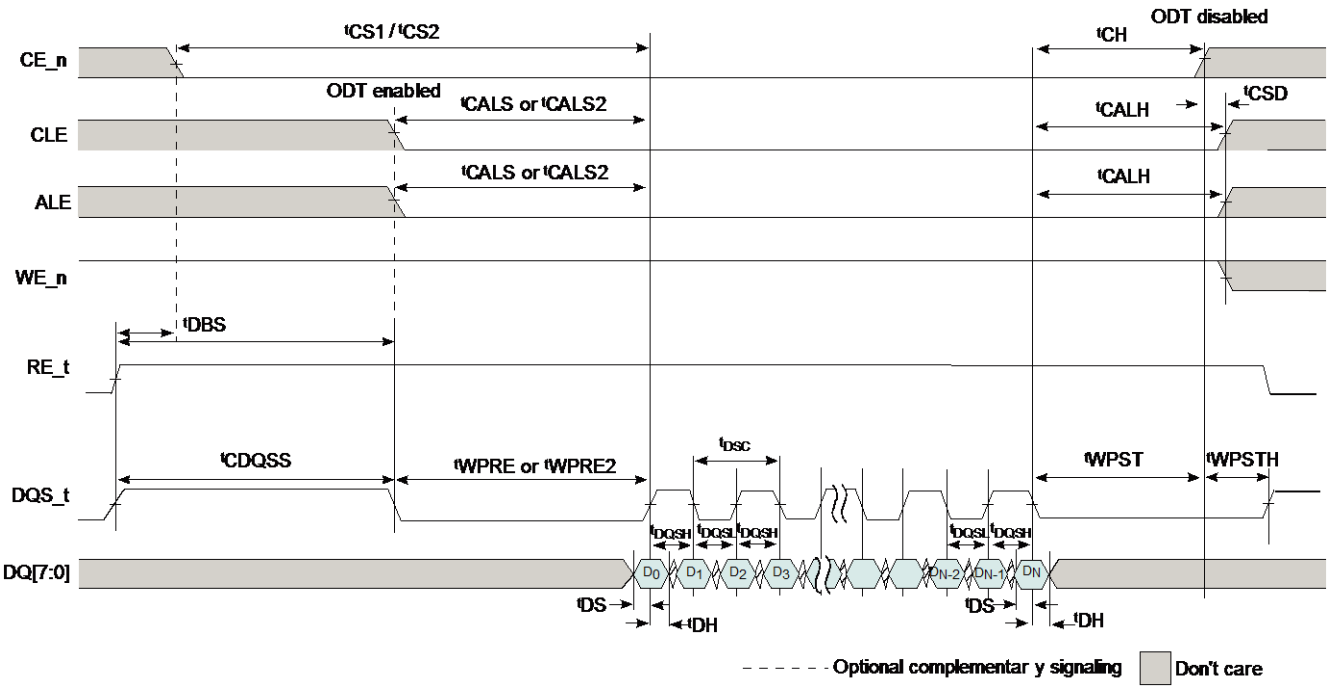


Figure 50. Read cycle

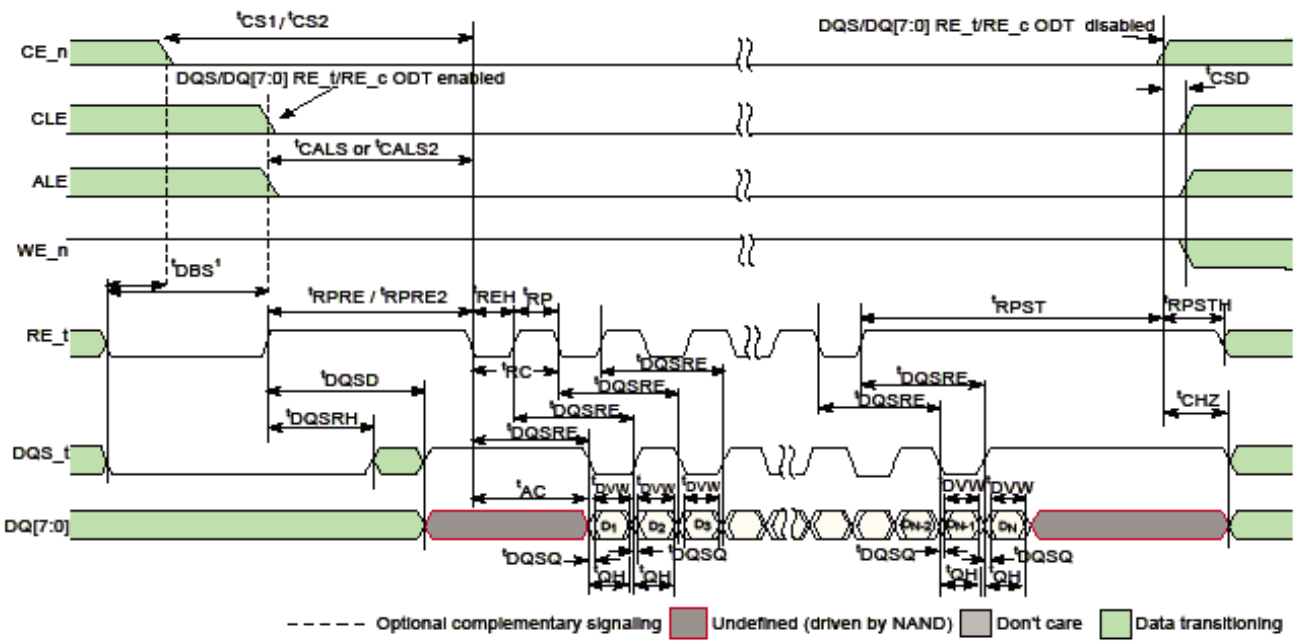


Figure 51. t_{ADL} timings

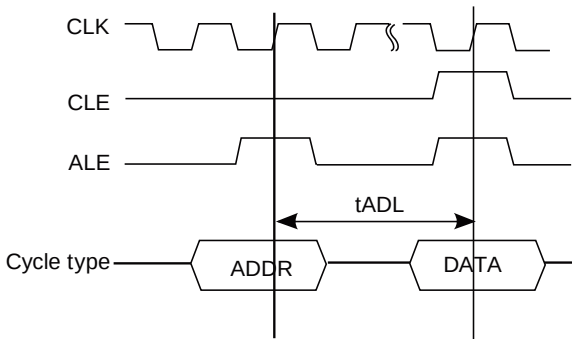


Figure 52. t_{WB}, t_{FEAT}, t_{ITC}, t_{RR} timings

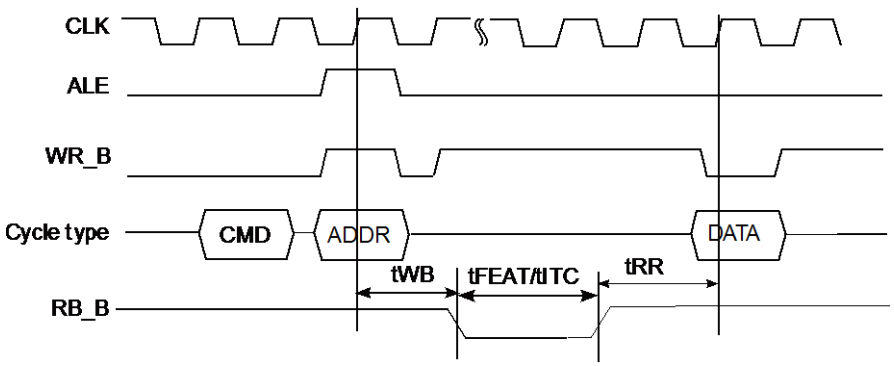


Figure 53. t_{RHW} timings

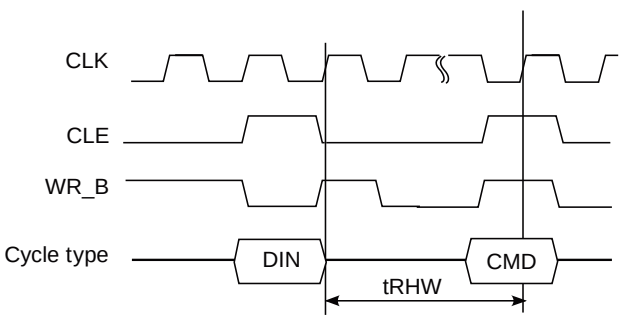


Figure 54. t_{WB} and t_{RST} timings

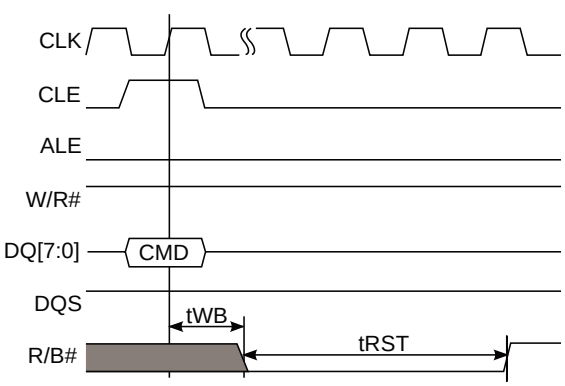


Figure 55. tWHR timings

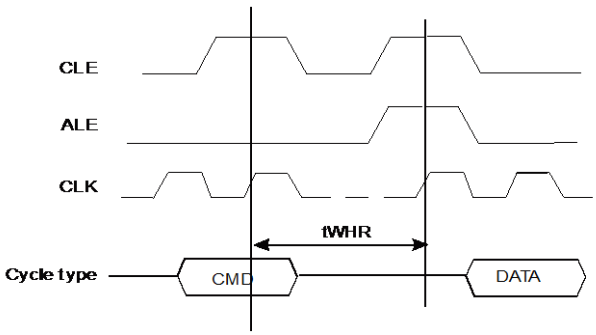
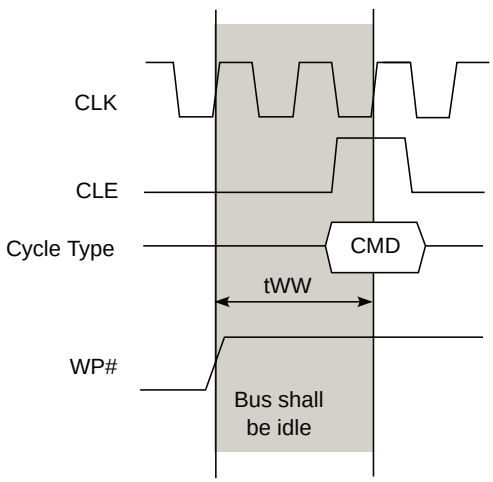


Figure 56. tWW timings



3.14 LPUART interface

This section describes the DC and AC electrical specifications for the LPUART interface.

3.14.1 LPUART DC electrical characteristics

This table provides the DC electrical characteristics for the LPUART interface when operating at DV_{DD}/EV_{DD} = 3.3 V.

Table 79. LPUART DC electrical characteristics (DV_{DD}/EV_{DD} = 3.3 V)[2]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x D/ EV_{DD}	–	V	1
Input low voltage	V_{IL}	–	0.2 x D/EV_{DD}	V	1
Input current (D/EV_{IN} = 0 V or D/EV_{IN} = D/EV_{DD})	I_{IN}	–	±50	μA	–
Output high voltage (I_{OH} = -2.0 mA)	V_{OH}	2.4	–	V	–
Output low voltage (I_{OL} = 2.0 mA)	V_{OL}	–	0.4	V	–

Notes:
1. The min V_{IL} and max V_{IH} values are based on the min and max D/EV_{DD} respective values found in Table 4.
2. For recommended operating conditions, see Table 4.

This table provides the DC electrical characteristics for the LPUART interface when operating at EV_{DD}/ DV_{DD} = 1.8 V.

Table 80. LPUART DC electrical characteristics (1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x E/ DV_{DD}	–	V	1
Input low voltage	V_{IL}	–	0.2 x E/DV_{DD}	V	1
Input current (E/DV_{IN} = 0 V or E/DV_{IN} = E/DV_{DD})	I_{IN}	–	±50	μA	2
Output high voltage (E/DV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	–	V	–
Output low voltage (DV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	–	0.4	V	–

Notes:
1. The min V_{IL} and max V_{IH} values are based on the min and max E/DV_{DD} respective values found in Table 4.
2. The symbol E/DV_{IN} represents the input voltage of the supply referenced in Table 4.
3. For recommended operating conditions, see Table 4.

3.14.2 LPUART AC timing specifications

This table provides the AC timing specifications for the LPUART interface.

Table 81. LPUART AC timing specifications

Parameter	Value	Unit	Notes
Minimum baud rate	$f_{PLAT}/(2 \times 32 \times 8192)$	baud	1, 3, 4
Maximum baud rate	$f_{PLAT}/(2 \times 4)$	baud	1, 2, 4

Notes:
1. f_{PLAT} refers to the internal platform clock.
2. The actual attainable baud rate is limited by the latency of interrupt processing.
3. Every bit can be over sampled with a sample clock rate of 8 and 64 times (software configurable) and each bit is the majority of the values sampled at the sample rate divided by two, (sample rate/2)+1 and (sample rate/2)+2.
4. The 1-to-0 transition during a data word can cause a resynchronization of the sample point.

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3.15 DUART interface

This section describes the DC and AC electrical specifications for the DUART interface.

3.15.1 DUART DC electrical characteristics

This table provides the DC electrical characteristics for the DUART interface at DV_{DD} = 3.3 V.

Table 82. DUART DC electrical characteristics (3.3 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	–	V	1
Input low voltage	V_{IL}	–	0.2 x DV_{DD}	V	1
Input current (DV_{IN} = 0 V or DV_{IN} = DV_{DD})	I_{IN}	–	±50	µA	2
Output high voltage (DV_{DD} = min, I_{OH} = -2.0 mA)	V_{OH}	2.4	–	V	–
Output low voltage (DV_{DD} = min, I_{OL} = 2.0 mA)	V_{OL}	–	0.4	V	–

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 4.
2. The symbol DV_{IN} represents the input voltage of the supply referenced in Table 4.
3. For recommended operating conditions, see Table 4.

This table provides the DC electrical characteristics for the DUART interface at DV_{DD} = 1.8 V.

Table 83. DUART DC electrical characteristics (1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	–	V	1
Input low voltage	V_{IL}	–	0.2 x DV_{DD}	V	1
Input current (DV_{IN} = 0 V or DV_{IN} = DV_{DD})	I_{IN}	–	±50	µA	2
Output high voltage (DV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	–	V	–
Output low voltage (DV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	–	0.4	V	–

Notes:
1. The min V_{IL} and max V_{IH} values are based on the min and max DV_{IN} respective values found in Table 4.
2. The symbol DV_{IN} represents the input voltage of the supply referenced in Table 44.
3. For recommended operating conditions, see Table 44.

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3.15.2 DUART AC timing specifications

This table provides the AC timing specifications for the DUART interface.

Table 84. DUART AC timing specifications

Parameter	Value	Unit	Notes
Minimum baud rate	f_{PLAT}/(2 x 1,048,576)	baud	1, 3
Maximum baud rate	f_{PLAT}/(2 x 16)	baud	1, 2

Notes:

1. f_{PLAT} refers to the internal platform clock.
2. The actual attainable baud rate is limited by the latency of interrupt processing.
3. The middle of a start bit is detected as the eighth sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16^{th} sample.

3.16 Flextimer interface

This section describes the DC and AC electrical characteristics for the Flextimer interface. There are Flextimer pins on various power supplies in this device.

3.16.1 Flextimer DC electrical characteristics

This table provides the DC electrical characteristics for Flextimer pins operating at DV_{DD}/EV_{DD} = 3.3 V.

Table 85. Flextimer DC electrical characteristics (DV_{DD}/EV_{DD} = 3.3 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x D/EV_{DD}	–	V	1
Input low voltage	V_{IL}	–	0.2 x D/EV_{DD}	V	1
Input current (V_{IN} = 0 V or V_{IN}= D/EV_{DD})	I_{IN}	–	±50	μA	2
Output high voltage (D/EV_{DD} = min, I_{OH} = -2 mA)	V_{OH}	2.4	–	V	–
Output low voltage (D/EV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	–	0.4	V	–

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN}/EV_{IN} values found in Table 4.
2. The symbol V_{IN}, in this case, represents the DV_{IN}/EV_{IN} symbol referenced in Table 4.
3. For recommended operating conditions, see Table 4.

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This table provides the DC electrical characteristics for Flextimer pins operating at $DV_{DD}/EV_{DD}/LV_{DD}/OV_{DD}$ = 1.8 V.

Table 86. Flextimer DC electrical characteristics ($DV_{DD}/EV_{DD}/LV_{DD}/OV_{DD}$ = 1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x D/E/L/ OV_{DD}	–	V	1
Input low voltage	V_{IL}	–	0.2 x D/E/L/V_{DD}	V	1
Input low voltage	V_{IL}	–	0.3 x OV_{DD}	V	1
Input current (V_{IN} = 0 V or V_{IN} = D/E/L/ OV_{DD})	I_{IN}	–	±50	µA	2
Output high voltage ($D/E/L/OV_{DD}$ = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	–	V	–
Output low voltage ($D/E/L/OV_{DD}$ = min, I_{OL} = 0.5 mA)	V_{OL}	–	0.4	V	–

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max $DV_{IN}/EV_{IN}/L/OV_{IN}$ values found in Table 4.
2. The symbol V_{IN}, in this case, represents the $DV_{IN}/EV_{IN}/L/OV_{IN}$ symbol referenced in Table 4.
3. For recommended operating conditions, see Table 4.

This table provides the DC electrical characteristics for Flextimer pins operating at LV_{DD} = 2.5 V.

Table 87. Flextimer DC electrical characteristics (LV_{DD}= 2.5 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x LVDD	–	V	1
Input low voltage	V_{IL}	–	0.2 x LVDD	V	1
Input current (V_{IN} = 0 V or V_{IN}= LV_{DD})	I_{IN}	–	±50	µA	2
Output high voltage (LV_{DD} = min, I_{OH} = -1 mA)	V_{OH}	2.0	–	V	–
Output low voltage (LV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	–	0.4	V	–

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 4.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 4.
3. For recommended operating conditions, see Table 4.

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3.16.2 Flextimer AC timing specifications

This table provides the Flextimer AC timing specifications.

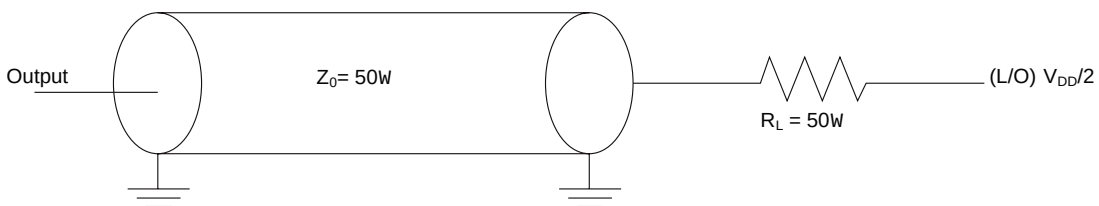
Table 88. Flextimer AC timing specifications[2]

Parameter	Symbol	Min	Unit	Notes
Flextimer inputs–minimum pulse width	t_{PIWID}	20	ns	1

Notes:
1. Flextimer inputs and outputs are asynchronous to any visible clock. Flextimer outputs should be synchronized before use by any external synchronous logic. Flextimer inputs are required to be valid for at least t_{PIWID} to ensure proper operation.
2. For recommended operating conditions, see Table 4.

This figure provides the AC test load for the Flextimer.

Figure 57. Flextimer AC test load



3.17 SPI interface

This section describes the DC and AC electrical characteristics for the SPI interface.

3.17.1 SPI DC electrical characteristics

This table provides the DC electrical characteristics for the SPI interface operating at OV_{DD} = 1.8 V.

Table 89. SPI DC electrical characteristics (1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	–	V	1
Input low voltage	V_{IL}	–	0.3 x OV_{DD}	V	1
Input current (V_{IN} = 0 V or V_{IN} = OV_{DD})	I_{IN}	–	±50	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	–	V	–
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	–	0.4	V	–

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 4.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 4.
3. For recommended operating conditions, see Table 4.

3.17.2 SPI AC timing specifications

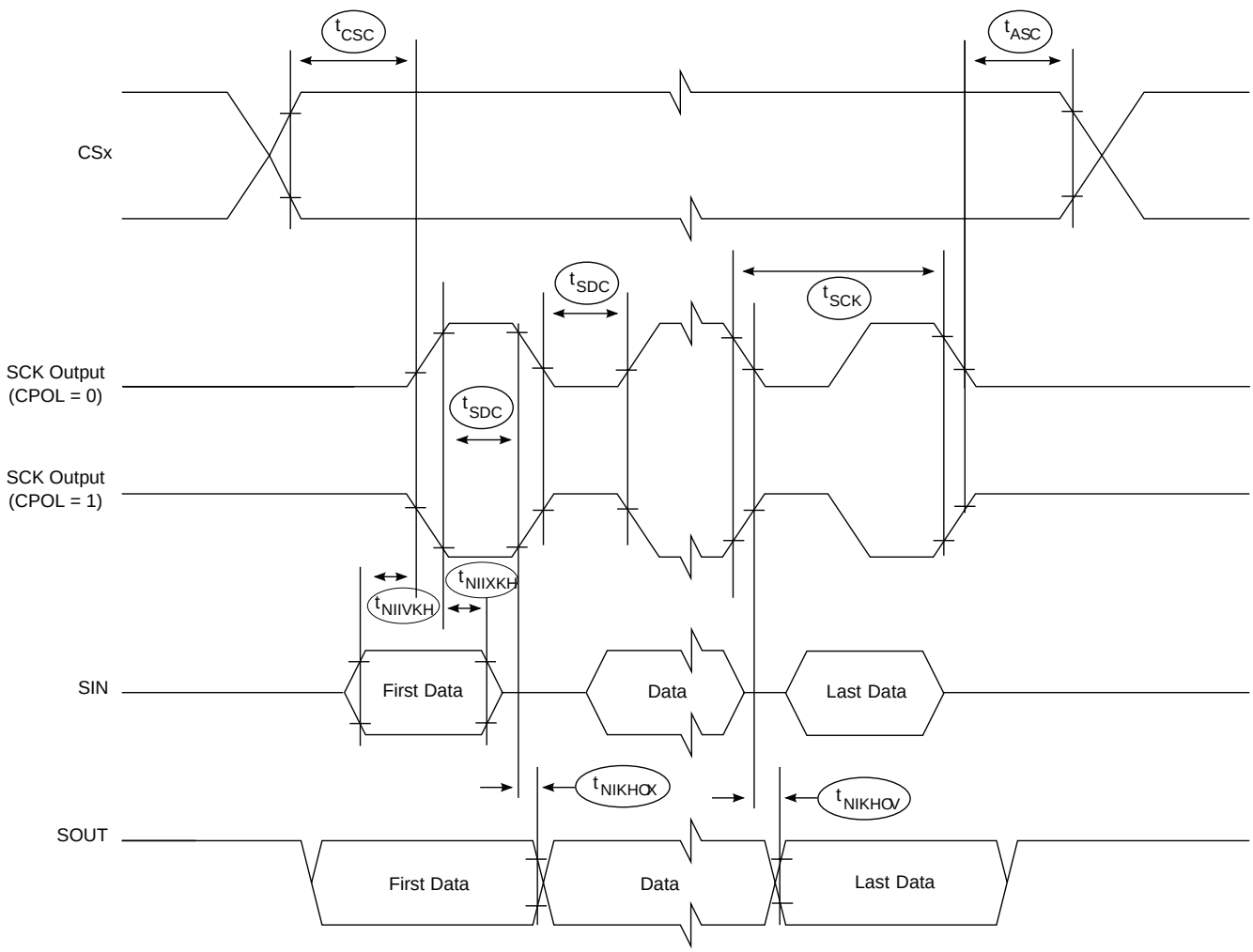
This table provides the SPI timing specifications.

Table 90. SPI AC timing specifications

Parameter	Symbol	Condition	Min	Max	Unit
SCK cycle time	t_{SCK}	–	t_{SYS} x 2	–	ns
SCK clock pulse width	t_{SDC}	–	40%	60%	t_{SCK}
CS to SCK delay	t_{CSC}	Master	16	–	ns
After SCK delay	t_{ASC}	Master	16	–	ns
Data setup time for inputs	t_{NIIVKH}	Master	9	–	ns
Data hold time for inputs	t_{NIIXKH}	Master	0	–	ns
Data valid (after SCK edge) for Outputs	t_{NIKHOV}	Master	–	5	ns
Data hold time for outputs	t_{NIKHOX}	Master	0	–	ns

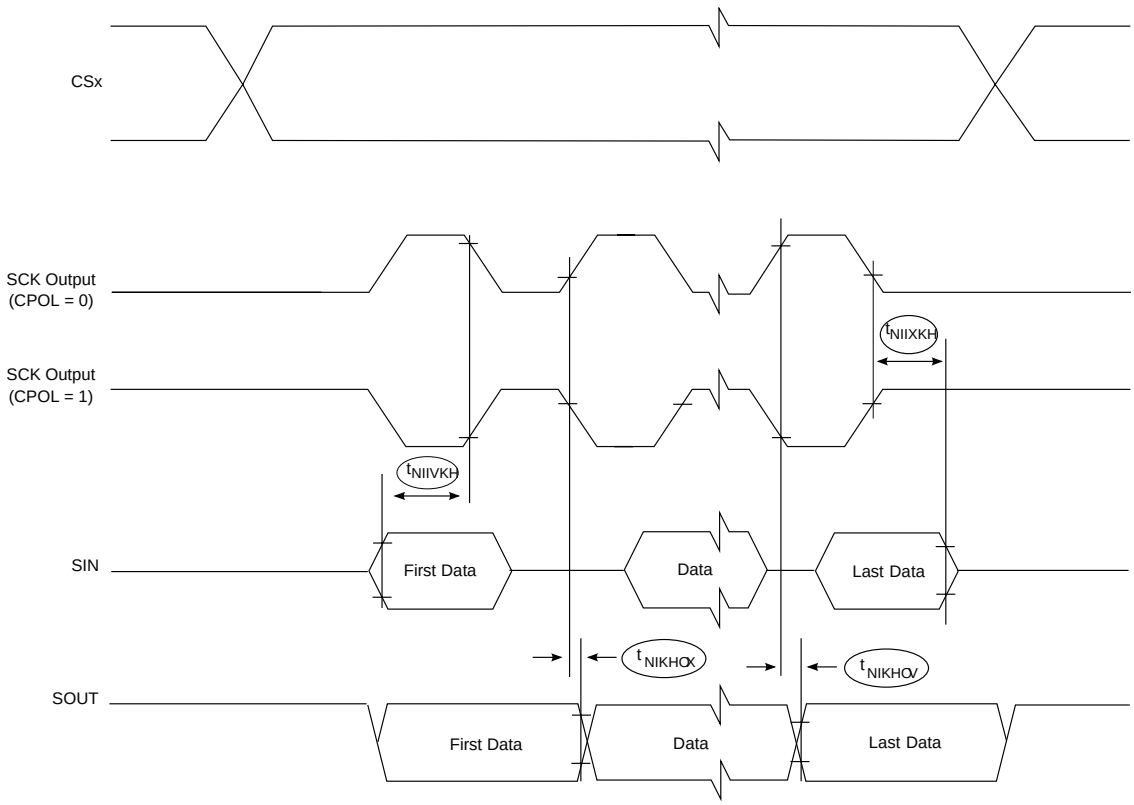
This figure shows the SPI timing master when CPHA = 0.

Figure 58. SPI timing master, CPHA = 0



This figure shows the SPI timing master when CPHA = 1.

Figure 59. SPI timing master, CPHA = 1



3.18 QSPI interface

This section describes the DC and AC electrical characteristics for the QSPI interface.

3.18.1 QSPI DC electrical characteristics

This table provides the DC electrical characteristics for the QSPI interface operating at OV_{DD} = 1.8 V.

Table 91. QSPI DC electrical characteristics (1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	–	V	1
Input low voltage	V_{IL}	–	0.3 x OV_{DD}	V	1
Input current (V_{IN} = 0 V or V_{IN} = OV_{DD})	I_{IN}	–	±50	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	OV_{DD} - 0.2	–	V	–
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	–	0.4	V	–

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 4.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 4.
3. For recommended operating conditions, see Table 4.

3.18.2 QSPI AC timing specifications

This section describes the QSPI timing specifications in SDR mode. All data is based on a negative edge data launch from the device and a positive edge data capture, as shown in the timing figures in this section.

3.18.2.1 QSPI timing SDR mode

This table provides the QSPI input and output timing in SDR mode.

Table 92. SDR mode QSPI input and output timing

Parameter	Symbol	Min	Max	Unit
Clock frequency	F_{SCK}	–	62.5	MHz
Clock rise/fall time	T_{RISE}/T_{FALL}	1	–	ns
CS output hold time	$t_{NIKHOX2}$	-3.4	–	ns
CS output delay	$t_{NIKHOV2}$	–	3.5	ns
Setup time for incoming data	t_{NIIVKH}	8.6	–	ns
Hold time requirement for incoming data	t_{NIIXKH}	0.4	–	ns
Output data valid	t_{NIKHOV}	–	4.5	ns
Output data hold	t_{NIKHOX}	-4.4	–	ns

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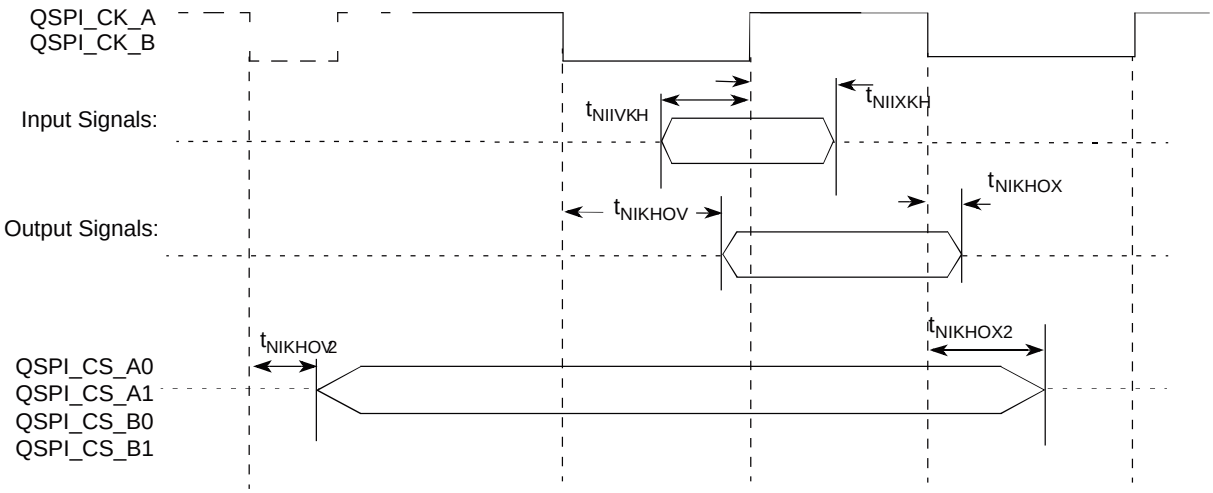
This figure shows the QSPI AC timing in SDR mode.

Figure 60. QSPI AC timing – SDR mode



3.19 Enhanced secure digital host controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC interface.

3.19.1 eSDHC DC electrical characteristics

This table provides the DC electrical characteristics for the eSDHC interface at D/EV_{DD} = 3.3 V.

Table 93. eSDHC interface DC electrical characteristics[2]

Characteristic	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x D/EV_{DD}	-	V	1
Input low voltage	V_{IL}	-	0.25 x D/EV_{DD}	V	1
Output high voltage (D/EV_{DD} = min, I_{OH} = -100 µA)	V_{OH}	0.75 x D/EV_{DD}	-	V	-
Output low voltage (D/EV_{DD} = min, I_{OL} = 100 µA)	V_{OL}	-	0.125 x D/EV_{DD}	V	-

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max D/EV_{IN} values found in Table 4 .
2. At recommended operating conditions with D/EV_{DD}= 3.3 V.

This table provides the DC electrical characteristics for the eSDHC interface at D/O/ EV_{DD} = 1.8 V.

Table 94. eSDHC interface DC electrical characteristics [3]

Characteristic	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x $D/O/EV_{DD}$	-	V	1
Input low voltage	V_{IL}	-	0.3 x $D/O/EV_{DD}$	V	1
Output high voltage ($D/O/EV_{DD}$= min, I_{OH} = -2mA)	V_{OH}	$D/O/EV_{DD}$ - 0.45	-	V	-
Output low voltage ($D/O/EV_{DD}$= min, I_{OL} = 2mA)	V_{OL}	-	0.45	V	-

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max $DV_{IN}/OV_{IN}/EV_{IN}$ values found in Table 4 .
2. At recommended operating conditions $DV_{DD}/OV_{DD}/EV_{DD}$= 1.8V.

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3.19.2 eSDHC AC timing specifications

This section provides the AC timing specifications.

This table provides the eSDHC AC timing specifications as defined in Figure 61, Figure 62, and Figure 63.

Table 95. eSDHC AC timing specifications (full-speed/high-speed mode)[6]

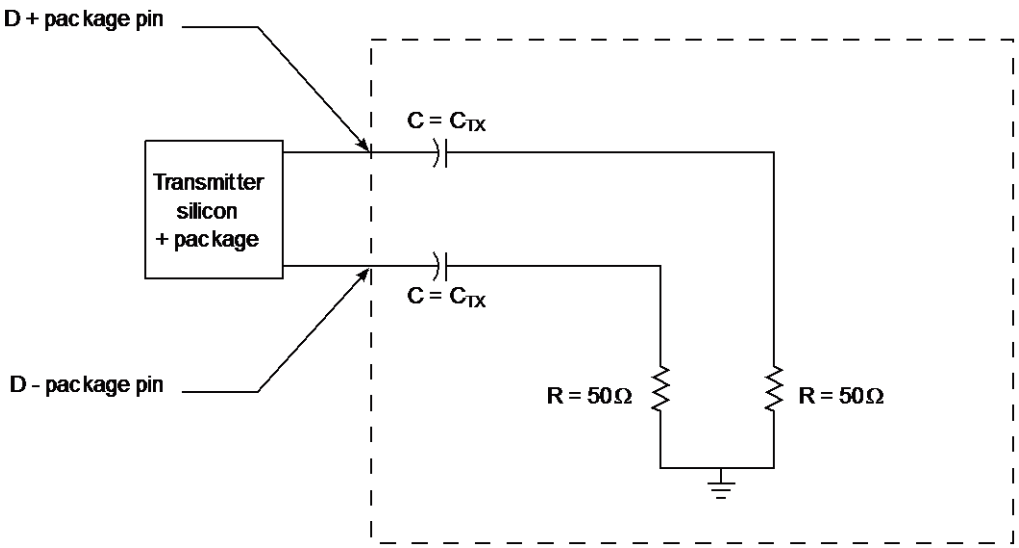
Parameter	Symbol[1]	Min	Max	Unit	Notes
SDHC_CLK clock frequency: SD/SDIO (full-speed/high-speed mode) eMMC (full-speed/high-speed mode)	f_{SHSCK}	0	25/50 26/52	MHz	2, 4
SDHC_CLK clock low time (full-speed/high-speed mode)	t_{SHSCKL}	10/7	-	ns	4
SDHC_CLK clock high time (full-speed/high-speed mode)	t_{SHSCKH}	10/7	-	ns	4
SDHC_CLK clock rise and fall times	t_{SHSCKR}/ t_{SHSCKF}	-	3	ns	4
Input setup times: SDHC_CMD, SDHC_DATx to SDHC_CLK	$t_{SHSIVKH}$	2.5	-	ns	3, 4, 5
Input hold times: SDHC_CMD, SDHC_DATx to SDHC_CLK	$t_{SHSIXKH}$	2.5	-	ns	4, 5
Output hold time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid	$t_{SHSKHOX}$	-3	-	ns	4, 5
Output delay time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid	$t_{SHSKHOV}$	-	3	ns	4, 5

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SHKHOX} symbolizes eSDHC high- speed mode device timing (SH) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. In full-speed mode, the clock frequency value can be 0-25MHz for an SD/SDIO card and 0-26MHz for an eMMC device. In high-speed mode, the clock frequency value can be 0-50MHz for an SD/SDIO card and 0-52MHz for an eMMC device.
3. SDHC_SYNC_OUT/IN loop back is recommended to compensate the clock delay. In case the SDHC_SYNC_OUT/IN loopback is not used, to satisfy setup timing, one-way board-routing delay between host and card, on SDHC_CLK, SDHC_CMD, and SDHC_DATx should not exceed 1ns for any high-speed MMC card. For any high-speed or default speed mode SD card, the one-way board-routing delay between host and card, on SDHC_CLK, SDHC_CMD, and SDHC_DATx should not exceed 1.5ns.
4. $C_{CARD} \leq 10$ pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 40$ pF.
5. The parameter values apply to both full-speed and high-speed modes.
6. At recommended operating conditions with EV_{DD}=1.8 V or 3.3V, see Table 4.

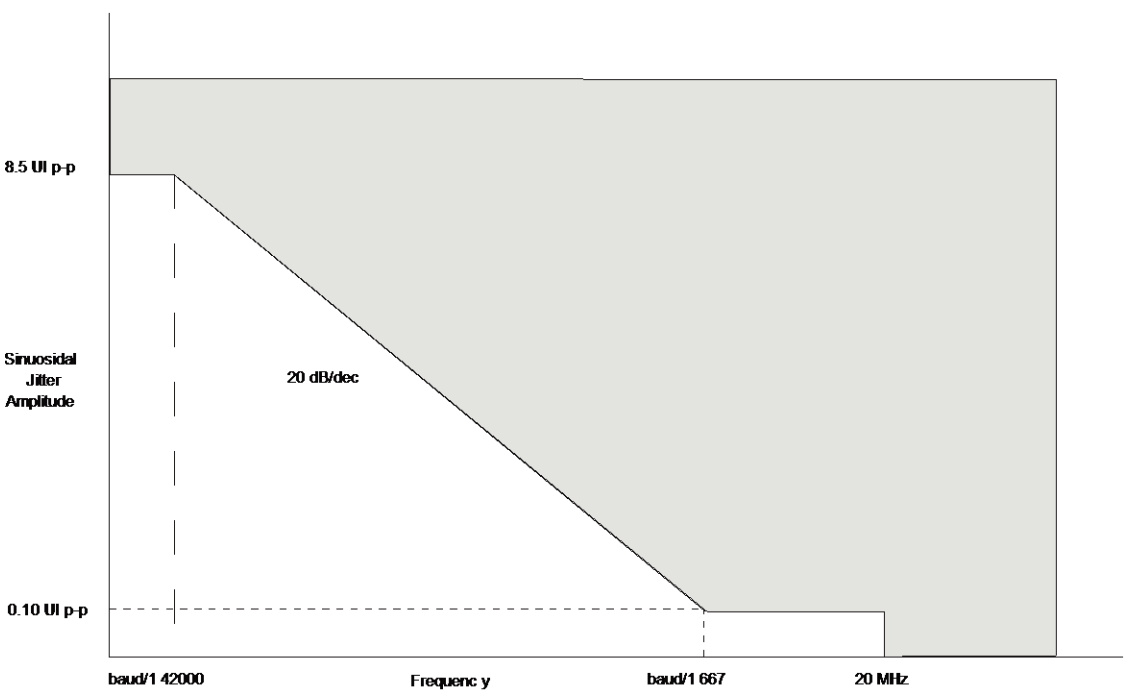
This figure provides the eSDHC clock input timing diagram.

Figure 61. eSDHC clock input timing diagram



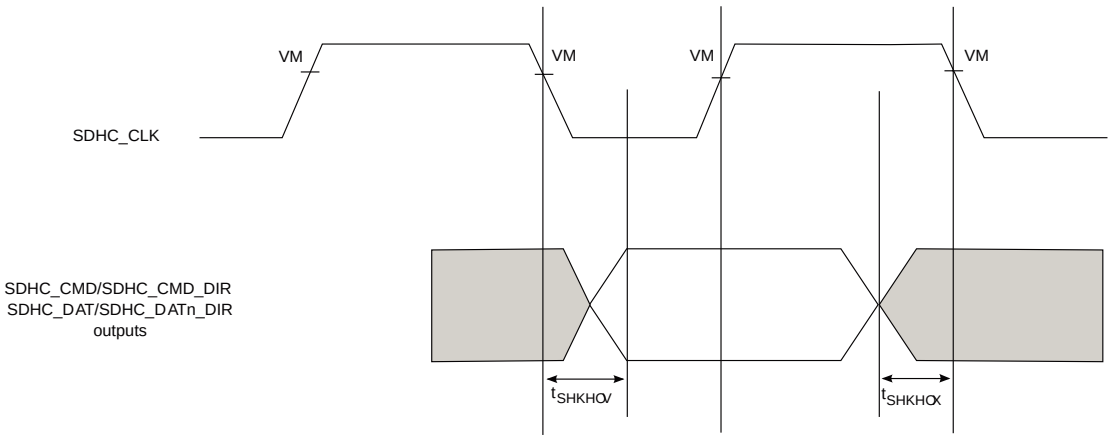
This figure provides the input AC timing diagram for high-speed mode.

Figure 62. eSDHC high-speed mode input AC timing diagram



This figure provides the output AC timing diagram for high-speed mode.

Figure 63. eSDHC high-speed mode output AC timing diagram



VM = Midpoint voltage (EV_{DD}/2)

This table provides the eSDHC AC timing specifications for SDR50 mode.

Table 96. eSDHC AC timing specifications (SDR 50 mode)

Parameter	Symbol	Min	Max	Unit	Notes
SDHC_CLK clock frequency:	f_{SHSCK}	0	90	MHz	
SDHC_CLK duty cycle	t_{SHSCKH}/ t_{SHSCK}	45	55	%	
SDHC_CLK clock rise and fall times	t_{SHSCKR}/ t_{SHSCKF}	-	2	ns	1
Skew between SD_CLK_SYNC_OUT and SD_CLK	-	-0.1	0.1	ns	1
Input setup times: SDHC_CMD, SDHC_DATx to SDHC_CLK_SYNC_IN	$t_{SHSIVKH}$	3.21	-	ns	2,1
Input hold times: SDHC_CMD, SDHC_DATx to SDHC_CLK_SYNC_IN	$t_{SHSIXKH}$	1.1	-	ns	2,1
Output hold time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid, SDHC_DATx_DIR, SDHC_CMD_DIR	$t_{SHSKHOX}$	1.7	-	ns	2,1
Output delay time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid, SDHC_DATx_DIR, SDHC_CMD_DIR	$t_{SHSKHOV}$	-	7.21	ns	2,1

Notes:

1. $C_{CARD} \leq 10$ pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 30$ pF
2. Without a voltage translator
3. At recommended operating conditions with EV_{DD}=1.8 V, see Table 4.

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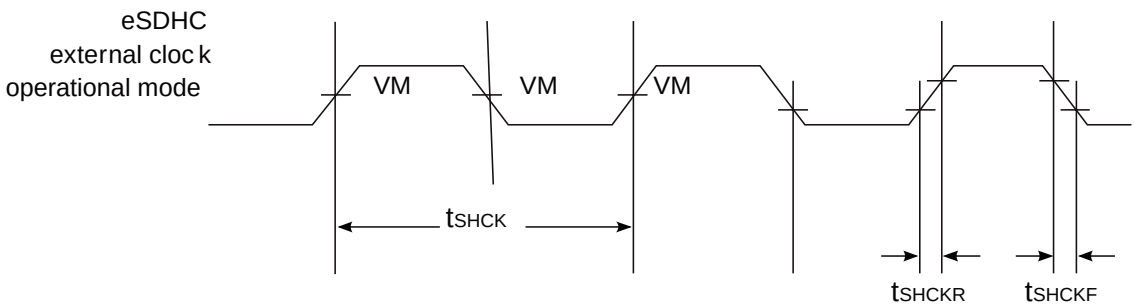
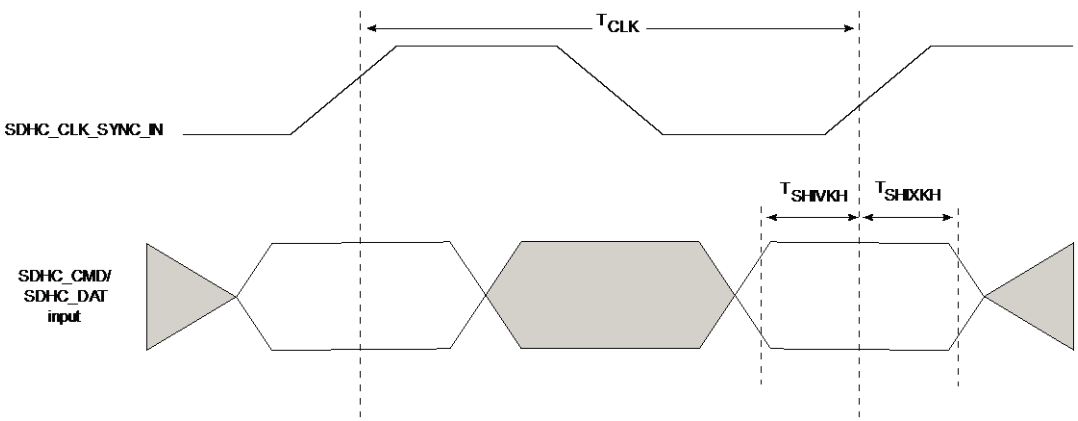
This figure provides the eSDHC clock input timing diagram for SDR50 mode.

Figure 64. eSDHC SDR50 mode clock input timing diagram



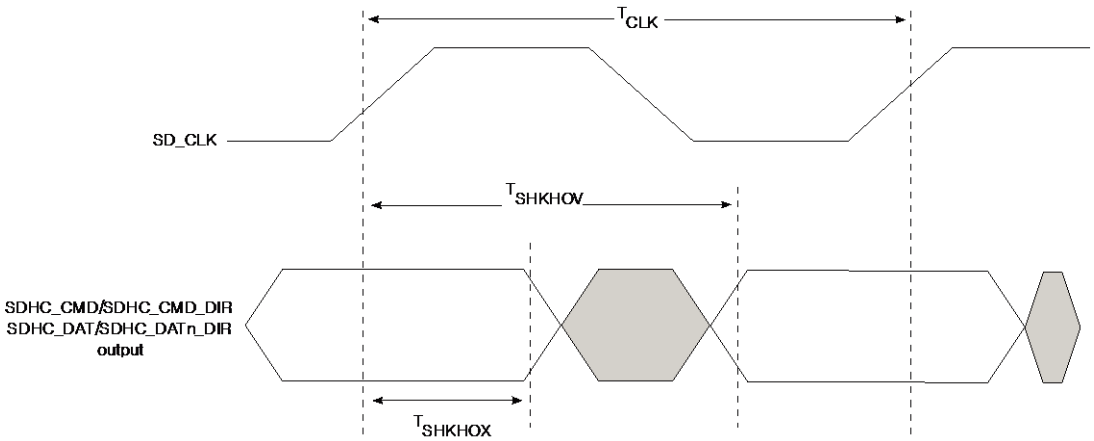
This figure provides the eSDHC input AC timing diagram for SDR50 mode.

Figure 65. eSDHC SDR50 mode input AC timing diagram



This figure provides the eSDHC output timing diagram for SDR50 mode.

Figure 66. eSDHC SDR50 mode output timing diagram



This table provides the eSDHC AC timing specifications for DDR50/DDR mode.

Table 97. eSDHC AC timing specifications (DDR50/DDR)[3]

Parameter	Symbol	Min	Max	Unit	Notes
SDHC_CLK clock frequency SD/SDIO DDR50 mode eMMC DDR mode	f_{SHCK}	-	- 50 52	MHz	-
SDHC_CLK duty cycle	t_{SHSCKH}/ t_{SHSCK}	47	53	%	
Skew between SDHC_CLK_SYNC_OUT and SDHC_CLK	-	-0.1	0.1	ns	-
SDHC_CLK clock rise and fall times SD/SDIO DDR50 mode eMMC DDR mode	t_{SHCKR}/ t_{SHCKF}	-	- 4 2	ns	1 2
Input setup times: SDHC_DATx to SDHC_CLK_SYNC_IN SD/SDIO DDR50 mode eMMC DDR mode	$t_{SHDIVKH}$	- 2.0 1.6	-	ns	1, 4 2
Input hold times: SDHC_DATx to SDHC_CLK_SYNC_IN SD/SDIO DDR50 mode eMMC DDR mode	$t_{SHDIXKH}$	- 1.1 1.1	-	ns	1 2
Output hold time: SDHC_CLK to SDHC_DATx valid, SDHC_DATx_DIR SD/SDIO DDR50 mode eMMC DDR mode	$t_{SHDKHOX}$	- 1.7 3.4	-	ns	1 2
Output delay time: SDHC_CLK to SDHC_DATx valid, SDHC_DATx_DIR	$t_{SHDKHOV}$	-	- 6.1	ns	1 2
SD/SDIO DDR50 mode eMMC DDR mode			6.2		
Input setup times: SDHC_CMD to SDHC_CLK_SYNC_IN SD/SDIO DDR50 mode eMMC DDR mode	$t_{SHCIVKH}$	- 5.3 4.5	-	ns	1 2
Input hold times: SDHC_CMD to SDHC_CLK_SYNC_IN		-	-	ns	1

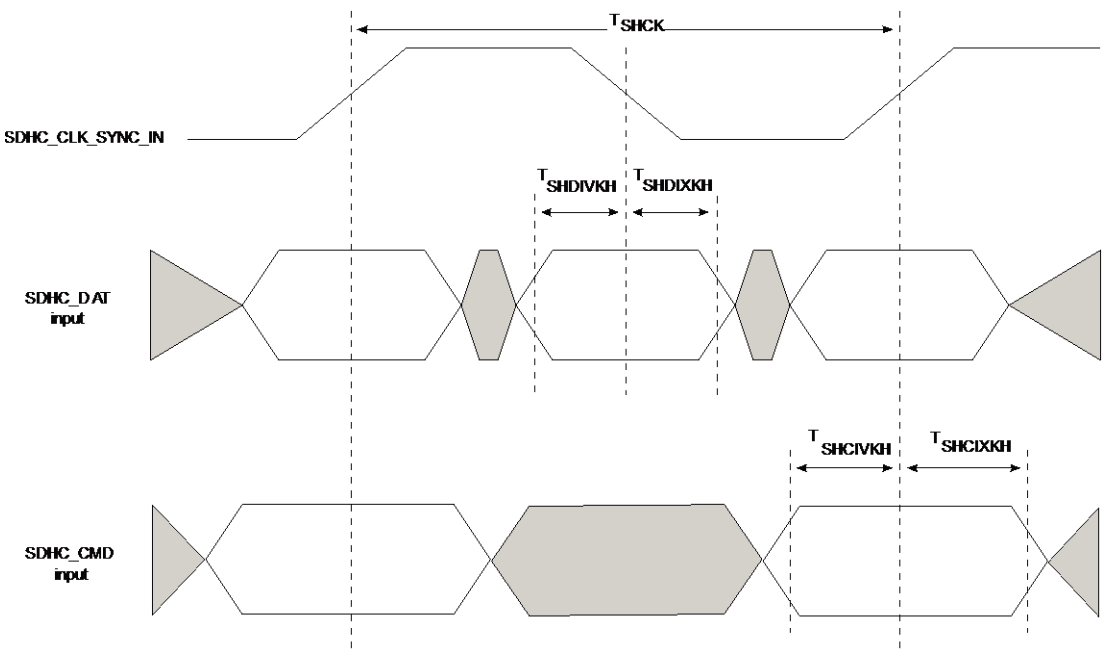
Parameter	Symbol	Min	Max	Unit	Notes
SD/SDIO DDR50 mode eMMC DDR mode	$t_{SHCIXKH}$	1.1 1.1			2
Output hold time: SDHC_CLK to SDHC_CMD valid, SDHC_CMD_DIR	$t_{SHCKHOX}$	-	-	ns	1
SD/SDIO DDR50 mode eMMC DDR mode		1.7 3.9			2
Output delay time: SDHC_CLK to SDHC_CMD valid, SDHC_CMD_DIR	$t_{SHCKHOV}$	-	- 13.1	ns	1
SD/SDIO DDR50 mode eMMC DDR mode			15.3		2

Notes:

1. CCARD ≤ 10 pF, (1 card).
2. CL = CBUS + CHOST + CCARD ≤ 20 pF for MMC, ≤ 25 pF for Input Data of DDR50, ≤ 30 pF for Input CMD of DDR50.
3. At recommended operating conditions with EVDD = 1.8 or 3.3 V for eMMC DDR mode, EVDD = 1.8 V for DDR50, see Table 4.

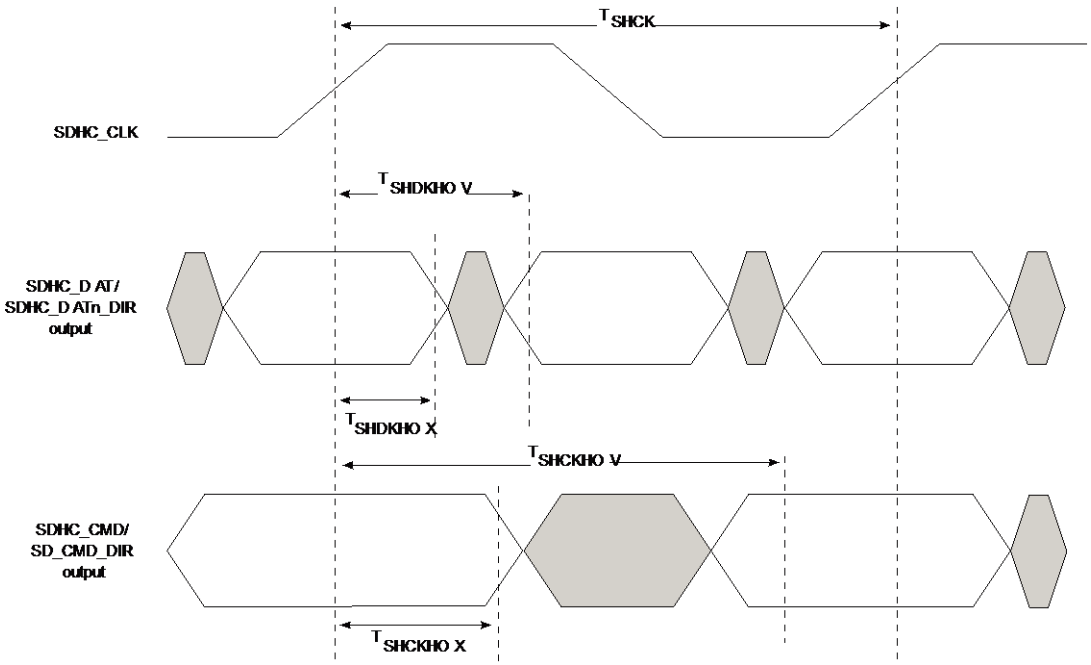
This figure provides the eSDHC DDR50/DDR mode input AC timing diagram.

Figure 67. eSDHC DDR50/DDR mode input AC timing diagram



This figure provides the eSDHC DDR50/DDR mode output AC timing diagram.

Figure 68. eSDHC DDR50/DDR mode output AC timing diagram


T SHCK
SDHC_CLK
T SHDKHO V
SDHC_D AT/
SDHC_D ATn_DIR
output
T SHDKHO X
T SHCKHO V
SDHC_CMD/
SD_CMD_DIR
output
T SHCKHO X

This table provides the eSDHC AC timing specifications for SDR104/eMMC HS200 mode.

Table 98. eSDHC AC timing specifications (SDR104/eMMC HS200)

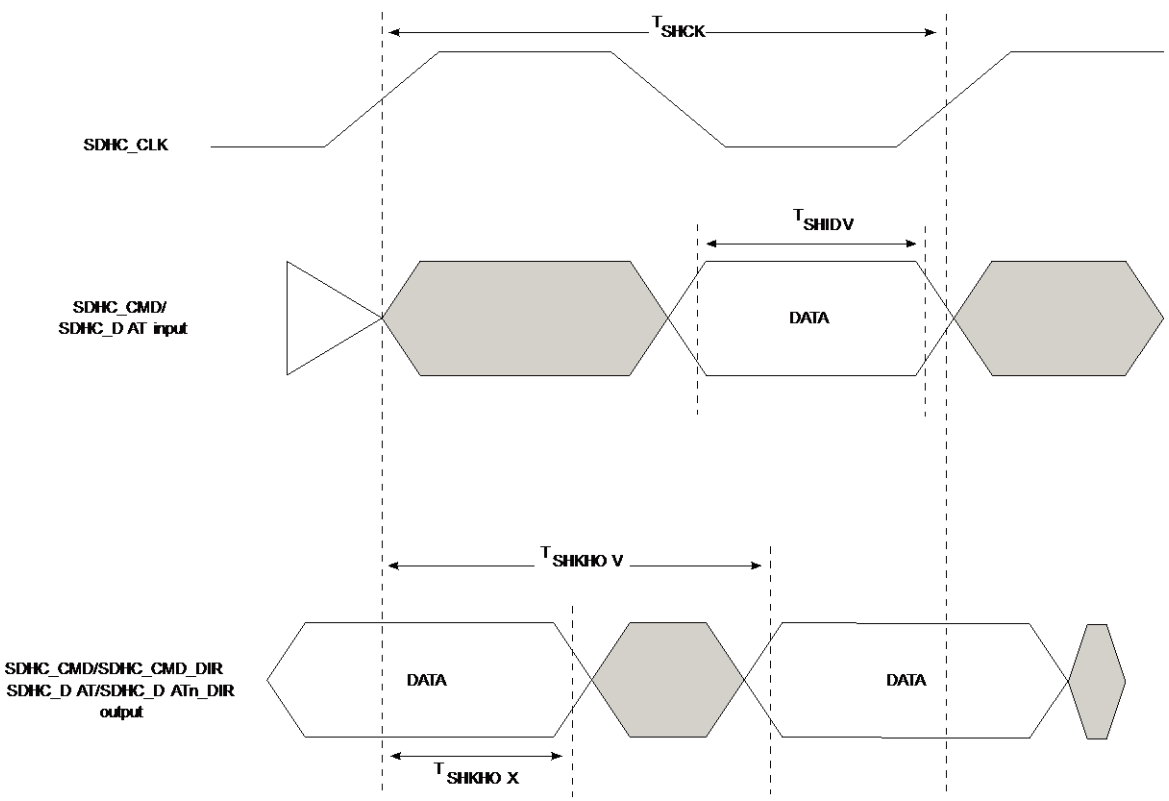
Parameter		Symbol[1]	Min	Max	Unit	Notes
SDHC_CLK clock frequency	SD/SDIO SDR104 mode	f_{SHCK}	-	167	MHz	1
	eMMC HS200 mode			167		-
SDHC_CLK duty cycle		t_{SHSCKH}/t_{SHSCK}	40	60	%	
SDHC_CLK clock rise and fall times		t_{SHCKR}/t_{SHCKF}	-	1	ns	1
Output hold time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid, SDHC_CMD_DIR, SDHC_DATx_DIR	SD/SDIO SDR104 mode	T_{SHKHOX}	1.58	-	ns	1
	eMMC HS200 mode		1.6			
Output delay time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid, SDHC_CMD_DIR, SDHC_DATx_DIR	SD/SDIO SDR104 mode	T_{SHKHOV}	-	3.94	ns	1
	eMMC HS200 mode			3.92		
Input data window (UI)	SD/SDIO SDR104 mode	t_{SHIDV}	0.5	-	Unit Interval	1
	eMMC HS200 mode		0.475			

Notes:

1. $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 15pF$.
2. At recommended operating conditions with EV_{DD} =1.8 V, see Table 4_bookmark40.

This figure provides the eSDHC SDR104/HS200 mode timing diagram.

Figure 69. eSDHC SDR104/HS200 mode timing diagram



3.20 JTAG controller

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface.

3.20.1 JTAG DC electrical characteristics

This table provides the JTAG DC electrical characteristics.

Table 99. JTAG DC electrical characteristics (OV_{DD} = 1.8V) (3)

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	–	V	1
Input low voltage	V_{IL}	–	0.3 x OV_{DD}	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	–	-100/+50	µA	2, 4
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	–	V	–
Output low voltage (OV_{DD} = min, I_{OL}= 0.5 mA)	V_{OL}	–	0.4	V	–

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 4.
2. The symbol V_{IN}, in this case, represents the O V_{IN} symbol found in Table 4.
3. For recommended operating conditions, see Table 4.
4. Per IEEE Std. 1149.1 specification, TDI, TMS, and TRST_B have internal pull-up.

3.20.2 JTAG AC timing specifications

This table provides the JTAG AC timing specifications as defined in Figure 70, Figure 71, Figure 72, and Figure 73.

Table 100. JTAG AC timing specifications(4)

Parameter		Symbol[1]	Min	Max	Unit	Notes
JTAG external clock frequency of operation		f_{JTG}	0	33.3	MHz	–
JTAG external clock cycle time		t_{JTG}	30	–	ns	–
JTAG external clock pulse width measured at 1.4 V		t_{JTKHK}L	15	–	ns	–
JTAG external clock rise and fall times		t_{JTGR}/t_{JTGF}	0	2	ns	–
TRST_B assert time		t_{TRST}	25	–	ns	2
Input setup times		t_{JTDVKH}	4	–	ns	–
Input hold times		t_{JTDXKH}	10	–	ns	–
Output valid times	Boundary-scan data	t_{JTKLDV}	–	15	ns	3
	TDO		–	10		
Output hold times		t_{JTKLDX}	0	–	ns	3

Notes:

1. The symbols used for timing specifications follow these patterns: $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals
2. (D) reaching the invalid state (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular function. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. TRST_B is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. All outputs are measured from the midpoint voltage of the falling edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
5. For recommended operating conditions, see Table 4.

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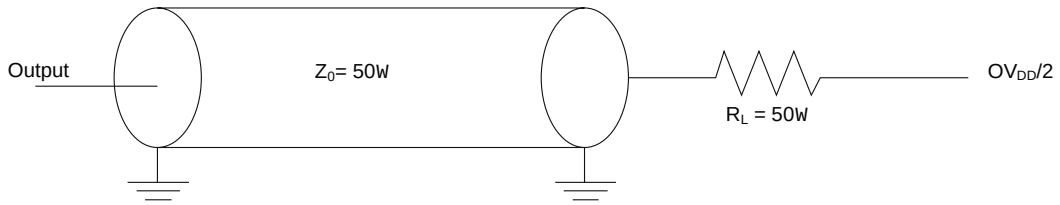
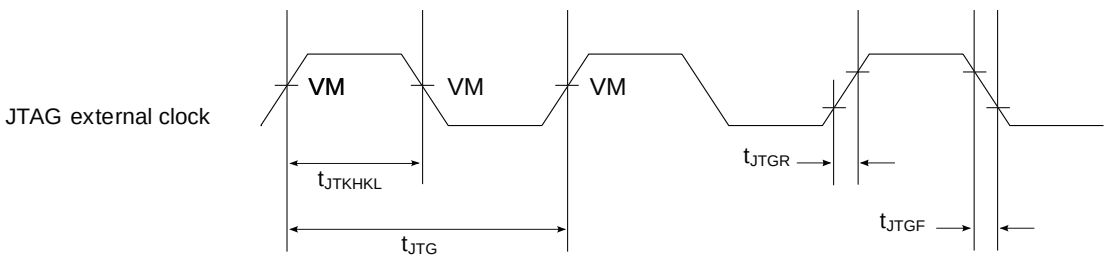
This figure shows the AC test load for TDO and the boundary-scan outputs of the device.

Figure 70. AC test load for the JTAG interface



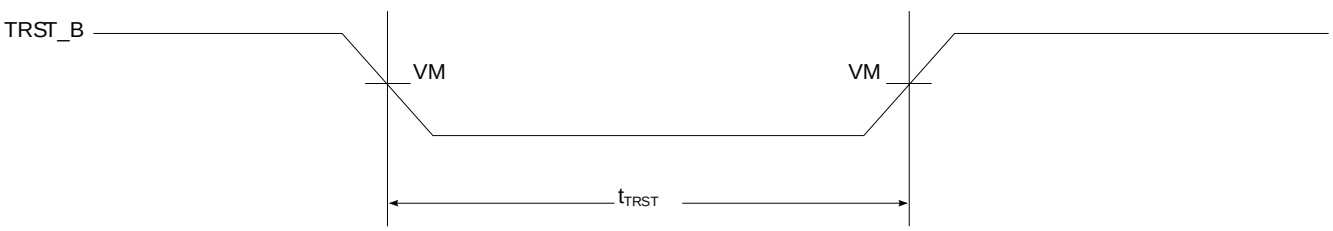
This figure shows the JTAG clock input timing diagram.

Figure 71. JTAG clock input timing diagram



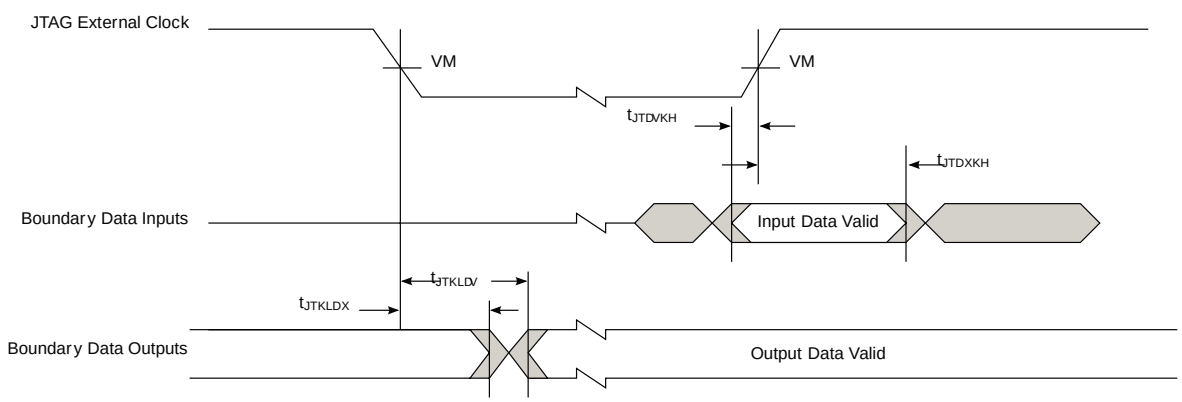
This figure shows the TRST_B timing diagram.

Figure 72. TRST_B timing diagram



This figure shows the boundary-scan timing diagram.

Figure 73. Boundary-scan timing diagram



3.21 I2C interface

This section describes the DC and AC electrical characteristics for the I^2C interfaces.

3.21.1 I^2C DC electrical characteristics

This table provides the DC electrical characteristics for the I^2C interfaces operating at DV_{DD} = 3.3 V.

Table 101. I^2C DC electrical characteristics (DV_{DD} = 3.3 V)[4]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	–	V	1
Input low voltage	V_{IL}	–	0.2 x DV_{DD}	V	1
Output low voltage (DV_{DD} = min, I_{OL} = 3 mA)	V_{OL}	–	0.4	V	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between 0.1 x DV_{DD} and 0.9 x DV_{DD}(max)	I_I	-50	50	µA	-
Capacitance for each I/O pin	C_I	–	10	pF	–

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 4.
2. The output voltage (open drain or open collector) condition = 3 mA sink current.
3. See the chip reference manual for information about the digital filter used.
4. For recommended operating conditions, see Table 4.

This table provides the DC electrical characteristics for the I^2C interfaces operating at DV_{DD} = 1.8 V.

Table 102. I^2C DC electrical characteristics (DV_{DD} = 1.8 V)[5]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	–	V	1
Input low voltage	V_{IL}	–	0.2 x DV_{DD}	V	1
Output low voltage (DV_{DD} = min, I_{OL} = 3 mA)	V_{OL}	0	0.36	V	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between 0.1 x DV_{DD} and 0.9 x DV_{DD}(max)	I_I	-50	50	µA	4
Capacitance for each I/O pin	C_I	–	10	pF	–

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 4.
2. The output voltage (open drain or open collector) condition = 3 mA sink current.
3. See the chip reference manual for information about the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if DV_{DD} is switched off.
5. For recommended operating conditions, see Table 4.

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3.21.2 I^2C AC timing specifications

This table provides the AC timing specifications for the I^2C interfaces.

Table 103. I^2C AC timing specifications[5]

Parameter		Symbol[1]	Min	Max	Unit	Notes
SCL clock frequency		f_{I2C}	0	400	kHz	2
Low period of the SCL clock		t_{I2CL}	1.3	–	µs	–
High period of the SCL clock		t_{I2CH}	0.6	–	µs	–
Setup time for a repeated START condition		t_{I2SVKH}	0.6	–	µs	–
Hold time (repeated) START condition (after this period, the first clock pulse is generated)		t_{I2SXKL}	0.6	–	µs	–
Data setup time		t_{I2DVKH}	100	–	ns	–
Data input hold time	CBUS compatible masters	t_{I2DXKL}	–	–	µs	3
	I^2C bus devices		0	–		
Data output delay time		t_{I2OVKL}	–	0.9	µs	4
Setup time for STOP condition		t_{I2PVKH}	0.6	–	µs	–
Bus free time between a STOP and START condition		t_{I2KHDX}	1.3	–	µs	–
Noise margin at the LOW level for each connected device (including hysteresis)		V_{NL}	0.1 x DV_{DD}	–	V	–
Noise margin at the HIGH level for each connected device (including hysteresis)		V_{NH}	0.2 x DV_{DD}	–	V	–
Capacitive load for each bus line		Cb	–	400	pF	–

Notes:

1. The symbols used for timing specifications herein follow these patterns: $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I^2C timing (I2) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I^2C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I^2C timing (I2) for the time that the data with respect to the STOP condition (P) reaches the valid state (V) relative
2. to the t_{I2C} clock reference (K) going to the high (H) state or setup time.
3. The requirements for I^2C frequency calculation must be followed. See *Determining the I^2C Frequency Divider Ratio for SCL* (AN2919).
4. As a transmitter, the chip provides a delay time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of a START or STOP condition. When the chip acts as the I^2C bus master while transmitting, it drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the chip does not generate an unintended START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for the chip as transmitter, see *Determining the I^2C Frequency Divider Ratio for SCL* (AN2919).
5. The maximum t_{I2OVKL} has to be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
6. For recommended operating conditions, see Table 4.

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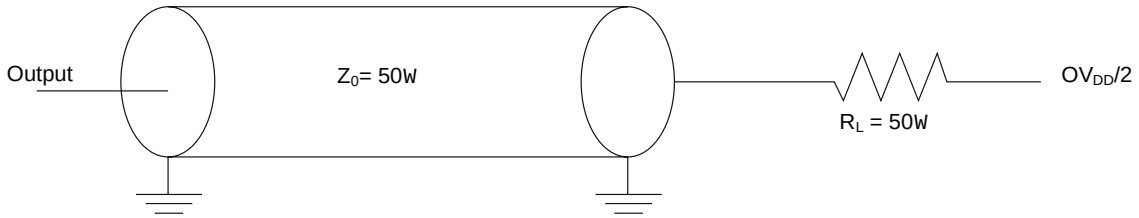
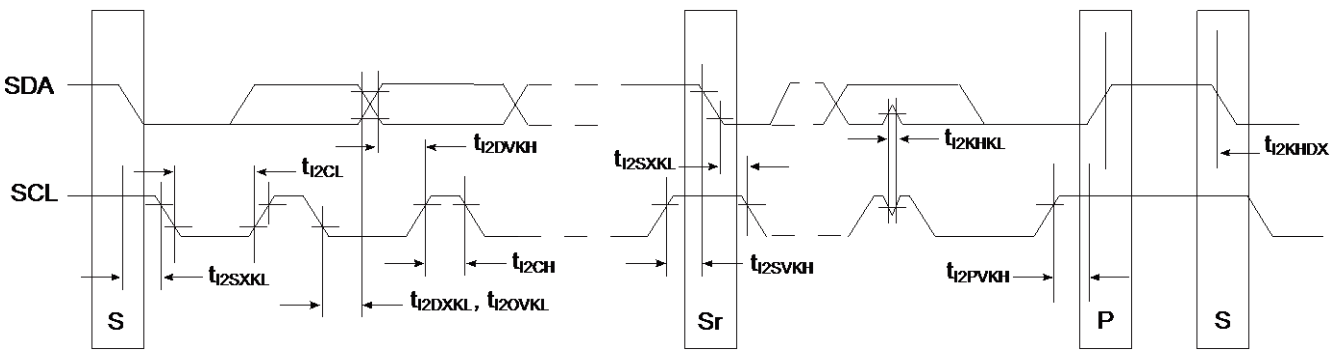
This figure shows the AC test load for the I^2C.

Figure 74. I^2C AC test load



This figure shows the AC timing diagram for the I^2C bus.

Figure 75. I^2C bus AC timing diagram



3.22 GPIO interface

This section describes the DC and AC electrical characteristics for the GPIO interface. There are GPIO pins on various power supplies in this device.

3.22.1 GPIO DC electrical characteristics

This table provides the DC electrical characteristics for GPIO pins operating at EV_{DD} = 3.3 V.

Table 104. GPIO DC electrical characteristics (EV_{DD} = 3.3 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x EV_{DD}	–	V	1
Input low voltage	V_{IL}	–	0.2 x EV_{DD}	V	1
Input current (V_{IN} = 0 V or V_{IN}= LV_{DD})	I_{IN}	–	±50	µA	2
Output high voltage (EV_{DD} = min, I_{OH} = -2 mA)	V_{OH}	2.4	–	V	–
Output low voltage (EV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	–	0.4	V	–

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max EV_{IN} values found in Table 4.
2. The symbol V_{IN}, in this case, represents the EV_{IN} symbol referenced in Table 4.
3. For recommended operating conditions, see Table 4.

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This table provides the DC electrical characteristics for GPIO pins operating at TV_{DD}/ LV_{DD} = 2.5 V.

Table 105. GPIO DC electrical characteristics (TV_{DD}/LV_{DD} = 2.5 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x T/LV_{DD}	–	V	1
Input low voltage	V_{IL}	–	0.2 x T/LV_{DD}	V	1
Input current (V_{IN} = 0 V or V_{IN}= T/LV_{DD})	I_{IN}	–	±50	µA	2
Output high voltage (T/LV_{DD} = min, I_{OH} = -2 mA)	V_{OH}	2.0	–	V	–
Output low voltage (T/LV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	–	0.4	V	–

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max L/TV_{IN} values found in Table 4.
2. The symbol V_{IN}, in this case, represents the L/TV_{IN} symbol referenced in Table 4.
3. For recommended operating conditions, see Table 4.

This table provides the DC electrical characteristics for GPIO pins operating at LV_{DD}/ EV_{DD}/DV_{DD}/TV_{DD}/OV_{DD} = 1.8 V.

Table 106. GPIO DC electrical characteristics (LV_{DD}/EV_{DD}/DV_{DD}/TV_{DD}/OV_{DD} = 1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x $L/E/D/T/OV_{DD}$	–	V	1
Input low voltage	V_{IL}	–	0.2 x $L/E/D/$ TV_{DD}	V	1
Input low voltage	V_{IL}	–	0.3 x OV_{DD}	V	1
Input current (V_{IN} = 0 V or V_{IN} = $/E/D/T/OV_{DD}$)	I_{IN}	–	±50	µA	2
Output high voltage ($L/E/D/T/OV_{DD}$ = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	–	V	–
Output low voltage ($L/E/D/T/OV_{DD}$ = min, I_{OL} = 0.5 mA)	V_{OL}	–	0.4	V	–

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max $LV_{IN}/EV_{IN}/DV_{IN}/TV_{IN}/OV_{IN}$ values found in Table 4.
2. The symbol V_{IN}, in this case, represents the $LV_{IN}/EV_{IN}/DV_{IN}/TV_{IN}/OV_{IN}$ symbol referenced in Table 4.
3. For recommended operating conditions, see Table 4.

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This table provides the DC electrical characteristics for GPIO pins operating at TV_{DD} = 1.2 V.

Table 107. GPIO DC electrical characteristics (TV_{DD} = 1.2 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x TV_{DD}	–	V	
Input low voltage	V_{IL}	–	0.2 x TV_{DD}	V	
Output low current current (V_{OL}= 0.2 V)	I_{OL}	4		mA	
Output high voltage (TV_{DD} = min, I_{OH} = -100uA)	V_{OH}	1.0	–	V	–
Output low voltage (TV_{DD} = min, I_{OL} = 100uA)	V_{OL}	–	0.2	V	–
Input Capacitance	C_{IN}	–	10	pF	–

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max TV_{IN} values found in Table 4.
2. The symbol V_{IN}, in this case, represents the TV_{IN} symbol referenced in Table 4.
3. For recommended operating conditions, see Table 4.

3.22.2 GPIO AC timing specifications

This table provides the GPIO input and output AC timing specifications.

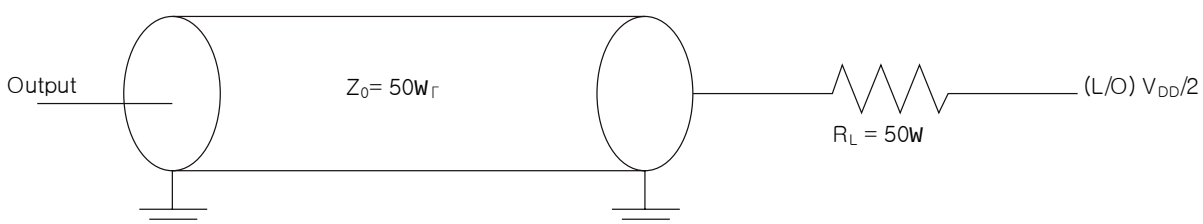
Table 108. GPIO Input AC timing specifications

Parameter	Symbol	Min	Unit	Notes
GPIO inputs-minimum pulse width	t_{PIWID}	20	ns	1

Notes:
1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least tPIWID to ensure proper operation.
2. For recommended operating conditions, see Table 4.

This figure provides the AC test load for the GPIO.

Figure 76. GPIO AC test load



3.23 GIC interface

This section describes the DC and AC electrical characteristics for the GIC interface.

3.23.1 GIC DC electrical characteristics

This table provides the DC electrical characteristics for GIC pins operating at DV_{DD} = 3.3 V.

Table 109. GIC DC electrical characteristics (DV_{DD} = 3.3 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	–	V	1
Input low voltage	V_{IL}	–	0.2 x DV_{DD}	V	1
Input current (V_{IN} = 0 V or V_{IN}= DV_{DD})	I_{IN}	–	±50	µA	2
Output high voltage (DV_{DD} = min, I_{OH} = -2 mA)	V_{OH}	2.4	–	V	–
Output low voltage (DV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	–	0.4	V	–

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 4.
2. The symbol V_{IN}, in this case, represents the DV_{IN} symbol referenced in Table 4.
3. For recommended operating conditions, see Table 4.

This table provides the GIC DC electrical characteristics when LV_{DD} = 2.5 V.

Table 110. GIC DC electrical characteristics (LV_{DD} = 2.5 V)[4]

Parameters	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x LV_{DD}	–	V	1
Input low voltage	V_{IL}	–	0.2 x LV_{DD}	V	1
Input current (LV_{IN} = 0 or LV_{IN} = LV_{DD})	I_{IN}	–	±50	µA	2, 3
Output high voltage (LV_{DD} = min, I_{OH} = -1.0 mA)	V_{OH}	2.00	–	V	–
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	–	0.40	V	–

Notes:
1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 4.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbols referenced in Table 4.
3. The symbol LV_{DD}, in this case, represents the LV_{DD} symbols referenced in Table 4.
4. For recommended operating conditions, see Table 4.

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This table provides the GIC DC electrical characteristics when $LV_{DD}/DV_{DD}/OV_{DD}$ = 1.8 V.

Table 111. GIC DC electrical characteristics (LV_{DD}/ DV_{DD}/ OV_{DD} = 1.8 V)[4]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x $L/D/OV_{DD}$	–	V	1
Input low voltage	V_{IL}	–	0.2 x L/DV_{DD}	V	1
Input low voltage	V_{IL}	–	0.3 x OV_{DD}	V	1
Input current ($L/D/OV_{IN}$ = 0 V or L/D/ OV_{IN} = $L/D/OV_{DD}$)	I_{IN}	–	±50	µA	2, 3
Output high voltage ($L/D/OV_{DD}$ = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	–	V	3
Output low voltage ($L/D/OV_{DD}$ = min, I_{OL} = 0.5 mA)	V_{OL}	–	0.4	V	3

Notes:

5. The min $V_{IL}$and max V_{IH} values are based on the min and max $L/D/OV_{IN}$ respective values found in Table 4_bookmark40.
6. The symbol $L/D/OV_{IN}$ represents the $L/D/OV_{IN}$ symbols referenced in Table 4.
7. The symbol $L/D/OV_{DD}$, in this case, represents the $L/D/OV_{DD}$ symbols referenced in Table 4.
8. For recommended operating conditions, see Table 4.

3.23.2 GIC AC timing specifications

This table provides the GIC input and output AC timing specifications.

Table 112. GIC input AC timing specifications[2]

Characteristic	Symbol	Min	Max	Unit	Notes
GIC inputs-minimum pulse width	t_{PIWID}	3	-	SYSCLKs	1

1. GIC inputs and outputs are asynchronous to any visible clock. GIC outputs must be synchronized before use by any external synchronous logic. GIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.
2. For recommended operating conditions, see Table 4.

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3.24 High-speed serial interfaces (HSSI)

The chip features a Serializer/Deserializer (SerDes) interface to be used for high-speed serial interconnect applications. The SerDes interface can be used for PCI Express, SGMII, and serial ATA (SATA) data transfers.

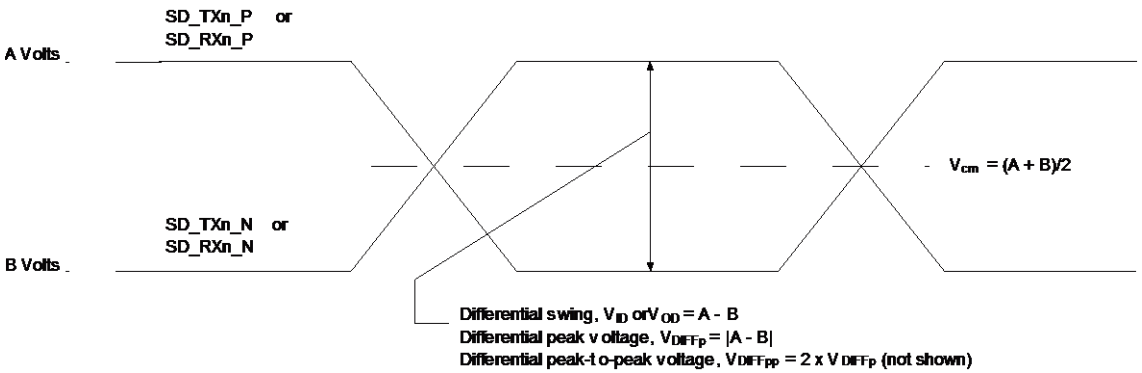
This section describes the most common portion of the SerDes DC electrical specifications: the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter (Tx) and receiver (Rx) reference circuits are also described.

3.24.1 Signal terms definitions

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines the terms that are used in the description and specification of differential signals.

This figure shows how the signals are defined. For illustration purposes only, one SerDes lane is used in the description. This figure shows the waveform for either a transmitter output (SD_TX*n*_P and SD_TX*n*_N) or a receiver input (SD_RX*n*_P and SD_RX*n*_N). Each signal swings between A volts and B volts where A > B.

Figure 77. Differential voltage definitions for transmitter or receiver



Using this waveform, the definitions are as described in the following list. To simplify the illustration, the definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment:

Single-Ended Swing

The transmitter output signals and the receiver input signals SD_TX*n*_P, SD_TX*n*_N, SD_RX*n*_P and SD_RX*n*_N each have a peak-to-peak swing of A - B volts. This is also referred to as each signal wire's single-ended swing.

Differential Output Voltage, V_{OD} (or Differential Output Swing)

The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complementary output voltages: $V_{SD\_TXn\_P} - V_{SD\_TXn\_N}$. The V_{OD} value can be either positive or negative.

Differential Input Voltage, V_{ID} (or Differential Input Swing)

The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complementary input voltages: $V_{SD\_RXn\_P} - V_{SD\_RXn\_N}$. The V_{ID} value can be either positive or negative.

Differential Peak Voltage, V_{DIFFp}

The peak value of the differential transmitter output signal or the differential receiver input signal is defined as the differential peak voltage, V_{DIFFp} = |A - B| volts.

Differential Peak-to-Peak, $V_{DIFFp-p}$

Because the differential output signal of the transmitter and the differential input signal of the receiver each range from A - B to -(A - B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2 \times V_{DIFFp} = 2 \times |(A - B)|$ volts, which is twice the differential swing in amplitude, or twice the differential peak. For example, the output differential peak-to-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2 \times |V_{OD}|$.

Differential Waveform

The differential waveform is constructed by subtracting the inverting signal (SD_TX*n*_N, for example) from the non-inverting signal (SD_TX*n*_P, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. See Figure 82 as an example for differential waveform.

Common Mode Voltage, V_{cm}

The common mode voltage is equal to half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm\_out} = (V_{SD\_TXn\_P} + V_{SD\_TXn\_N}) \div 2 = (A + B) \div 2$, which is the arithmetic mean of the two complementary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. It may be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset on some occasions.

To illustrate these definitions using real values, consider the example of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and outputs, TD and TD_B. If these outputs have a swing from 2.0 V to 2.5 V, the peak-to-peak voltage swing of each signal (TD or TD_B) is 500 mV p-p, which is referred to as the single-ended swing for each signal. Because the differential signaling environment is fully symmetrical in this example, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and -500 mV. In other words, V_{OD} is 500 mV in one phase and -500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

3.24.2 SerDes reference clocks

The SerDes reference clock inputs are applied to an internal phase-locked loop (PLL) whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD*n*_REF_CLK[1:2]_P and SD*n*_REF_CLK[1:2]_N.

SerDes may be used for various combinations of the following IP block based on the RCW Configuration field SRDS_PRTCLn:

- SGMII (1.25 Gbit/s or 3.125 Gbit/s), QSGMII (5 Gbit/s)
- XFI (10 Gbit/s)
- PCIe (2.5 Gbit/s, 5 Gbit/s, and 8 Gbit/s)
- SATA (1.5 Gbit/s, 3.0 Gbit/s, and 6.0 Gbit/s)

The following sections describe the SerDes reference clock requirements and provide application information.

3.24.2.1 SerDes spread-spectrum clock source recommendations

SD*n*_REF_CLK*n*_P and SD*n*_REF_CLK*n*_N are designed to work with spread-spectrum clocking for the PCI Express protocol only with the spreading specification defined in Table 113. When using spread-spectrum clocking for PCI Express, both ends of the link partners should use the same reference clock. For best results, a source without significant unintended modulation must be used.

The SerDes transmitter does not support spread-spectrum clocking for the SATA protocol. The SerDes receiver does support spread-spectrum clocking on receive, which means the SerDes receiver can receive data correctly from a SATA serial link partner using spread-spectrum clocking.

Spread-spectrum clocking cannot be used if the same SerDes reference clock is shared with other non-spread-spectrum-supported protocols. For example, if spread-spectrum clocking is desired on a SerDes reference clock for the PCI Express protocol and the same reference clock is used for any other protocol, such as SATA or SGMII because of the SerDes lane usage mapping option, spread-spectrum clocking cannot be used at all.

This table provides the source recommendations for SerDes spread-spectrum clocking.

Table 113. SerDes spread-spectrum clock source recommendations [1]

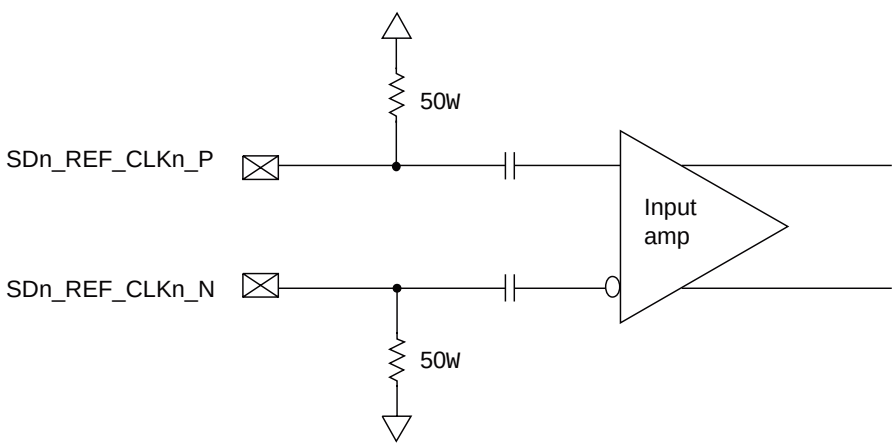
Parameter	Min	Max	Unit	Notes
Frequency modulation	30	33	kHz	–
Frequency spread	+0	-0.5	%	2

Notes:
1. At recommended operating conditions. See Table 4.
2. Only down-spreading is allowed.

3.24.2.2 SerDes reference clock receiver characteristics

This figure shows a receiver reference diagram of the SerDes reference clocks.

Figure 78. Receiver of SerDes reference clocks



The characteristics of the clock signals are as follows:

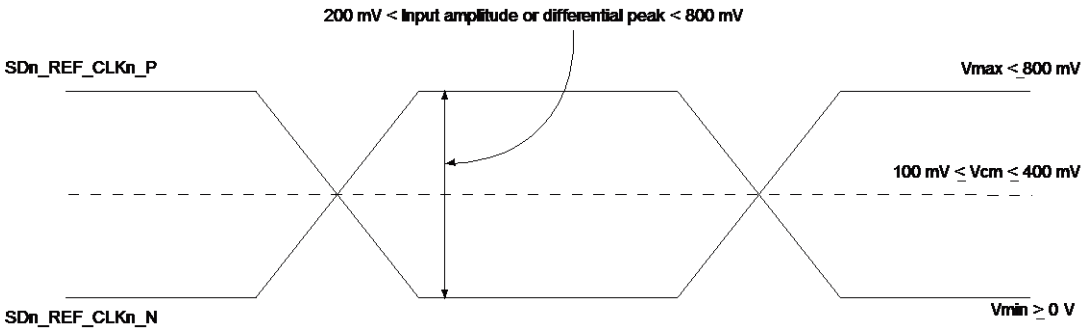
- The SerDes receiver's core power supply voltage requirements ($SV_{DD}n$) are as specified in Table 4.
- The SerDes reference clock receiver reference circuit structure is as follows:
  - The SD*n*_REF_CLKn_P and SD*n*_REF_CLKn_N are internally AC-coupled differential inputs as shown in Figure 78. Each differential clock input (SD*n*_REF_CLKn_P or SD*n*_REF_CLKn_N) has on-chip 50-Ω termination to SGNDn followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. See the differential mode and single-ended mode descriptions in Signal terms definitions for detailed requirements.
- The maximum average current requirement also determines the common mode voltage range.
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA because the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V ÷ 50 = 8 mA) while the minimum common mode input level is 0.1 V above SGND*n*. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0-0.8 V), such that each phase of the differential input has a single- ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  - If the device driving the SD*n*_REF_CLK*n*_P and SD*n*_REF_CLK*n*_N inputs cannot drive 50 Ω to SGND*n* DC or the drive strength of the clock driver chip exceeds the maximum input current limitations, it must be AC-coupled off-chip.
- The input amplitude requirement is described in detail in the following sections.

3.24.2.3 DC-level requirements for SerDes reference clocks

The DC-level requirements for the SerDes reference clock inputs are different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs, as described below:

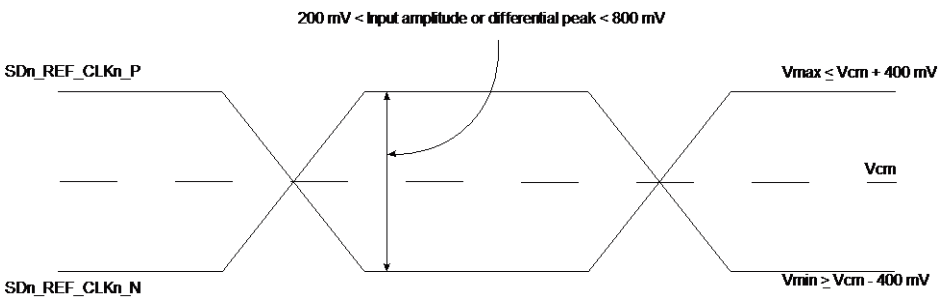
- Differential Mode
  - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-to-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing of less than 800 mV and greater than 200 mV. This requirement is same for both external DC-coupled or AC-coupled connection.
  - For an external DC-coupled connection, as described in Figure 78, the maximum average current requirements set the requirement for average voltage (common mode voltage) as between 100 mV and 400 mV.
  - This figure shows the SerDes reference clock input requirement for a DC- coupled connection scheme.

Figure 79. Differential reference clock input DC requirements (external DC-coupled)



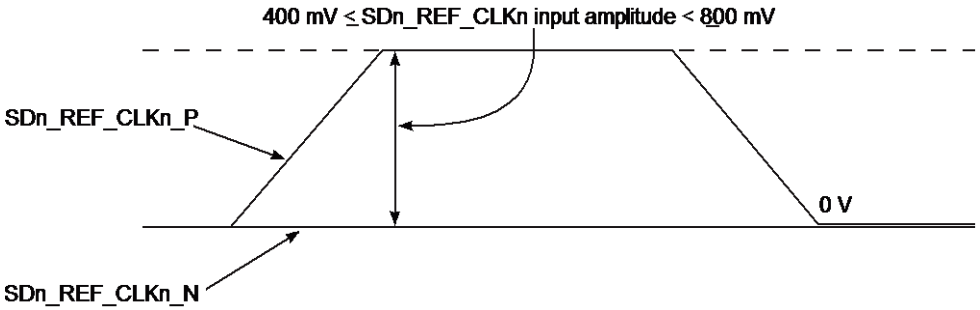
- For an external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Because the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different common mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND*n*. Each signal wire of the differential inputs is allowed to swing below and above the common mode voltage (SGND*n*).
- This figure shows the SerDes reference clock input requirement for an AC- coupled connection scheme.

Figure 80. Differential reference clock input DC requirements (external AC-coupled)



- Single-ended mode
  - The reference clock can also be single-ended. The SD*n*_REF_CLK*n*_P input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-to- peak (from V_{MIN} to V_{MAX}) with SD*n*_REF_CLK*n*_N either left unconnected or tied to ground.
  - To meet the input amplitude requirement, the reference clock inputs may need to be externally DC- or AC-coupled. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase (SD*n*_REF_CLK*n*_N) through the same source impedance as the clock input (SD*n*_REF_CLK*n*_P) in use.
  - The SD*n*_REF_CLK*n*_P input average voltage must be between 200 and 400 mV.
  - This figure shows the SerDes reference clock input requirement for single-ended signaling mode.

Figure 81. Single-ended reference clock input DC requirements



3.24.2.4 AC requirements for SerDes reference clocks

This table provides the AC requirements for SerDes reference clocks for PCI Express protocols running at data rates up to 5 Gbit/s.

This includes PCI Express (2.5 GT/s and 5 GT/s), SGMII (1.25 Gbit/s), and SATA (1.5 Gbit/s, 3.0 Gbit/s, and 6.0 Gbit/s). SerDes reference clocks need to be verified by the customer's application design.

Table 114. SD*n*_REF_CLK*n*_P and SD*n*_REF_CLK*n*_N input clock requirements 1

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SD*n*_REF_CLK*n*_P/ SD*n*_REF_CLK*n*_N frequency range	t_{CLK_REF}	–	100/125/156.25	–	MHz	2
SD*n*_REF_CLK*n*_P/ SD*n*_REF_CLK*n*_N clock frequency tolerance	t_{CLK_TOL}	-300	–	300	ppm	3
SD*n*_REF_CLK*n*_P/ SD*n*_REF_CLK*n*_N clock frequency tolerance	t_{CLK_TOL}	-100	–	100	ppm	4
SD*n*_REF_CLK*n*_P/ SD*n*_REF_CLK*n*_N reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	5
SD*n*_REF_CLK*n*_P/ SD*n*_REF_CLK*n*_N max deterministic peak-to-peak jitter at 10^{-6} BER	t_{CLK_DJ}	–	–	42	ps	–
SD*n*_REF_CLK*n*_P/ SD*n*_REF_CLK*n*_N total reference clock jitter at 10^{-6} BER (peak-to-peak jitter at refClk input)	t_{CLK_TJ}	–	–	86	ps	6
SD*n*_REF_CLK*n*_P/ SD*n*_REF_CLK*n*_N 10 kHz to 1.5 MHz RMS jitter	$t_{REFCLK\text{-}LF\text{-}RMS}$	–	–	3	ps RMS	7
SD*n*_REF_CLK*n*_P/ SD*n*_REF_CLK*n*_N > 1.5 MHz to Nyquist RMS jitter	$t_{REFCLK\text{-}HF\text{-}RMS}$	–	–	3.1	ps RMS	7
SD*n*_REF_CLK*n*_P/ SD*n*_REF_CLK*n*_N RMS reference clock jitter	$t_{REFCLK\text{-}RMS\text{-}DC}$	–	–	1	ps RMS	8
SD*n*_REF_CLK*n*_P/ SD*n*_REF_CLK*n*_N rising/ falling edge rate	t_{CLKRR}/t_{CLKFR}	0.6	–	4	V/ns	9
Differential input high voltage	V_{IH}	150	–	–	mV	5
Differential input low voltage	V_{IL}	–	–	-150	mV	5
Rising edge rate (SD*n*_REF_CLK*n*_P) to falling edge rate (SD*n*_REF_CLK*n*_N) matching	Rise-Fall Matching	–	–	20	%	10, 11

Notes:

1. For recommended operating conditions, see Table 4.
2. Caution: Only 100 and 125 have been tested. In-between values do not work correctly with the rest of the system.
3. For PCI Express (2.5, 5 and 8 GT/s).
4. For SGMII, 2.5GSGMII and QSGMII.
5. Measurement taken from differential waveform.
6. Limits from PCI Express CEM Rev 2.0.

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7. For PCI Express 5 GT/s, per PCI Express base specification Rev 3.0.
8. For PCI-Express-8 GT/s, per PCI-Express base specification rev 3.0
9. Measured from -150 mV to +150 mV on the differential waveform (derived from SD*n*_REF_CLK*n*_P minus SD*n*_REF_CLK*n*_N). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing. See Figure 82.
10. Measurement taken from single-ended waveform.
11. Matching applies to rising edge for SD*n*_REF_CLK*n*_P and falling edge rate for SD*n*_REF_CLK*n*_N. It is measured using ±75 mV window centered on the median cross point where SD*n*_REF_CLK*n*_P rising meets SD*n*_REF_CLK*n*_N falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SD*n*_REF_CLK*n*_P must be compared to the fall edge rate of SD*n*_REF_CLK*n*_N, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 83.

This table lists the AC requirements for SerDes reference clocks for protocols running at data rates greater than 8 GBaud.

This includes XFI (10.3125 GBaud), SerDes reference clocks to be guaranteed by the customer's application design.

Table 115. SD1_REF_CLKn_P/ SD1_REF_CLKn_N input clock requirements [1]

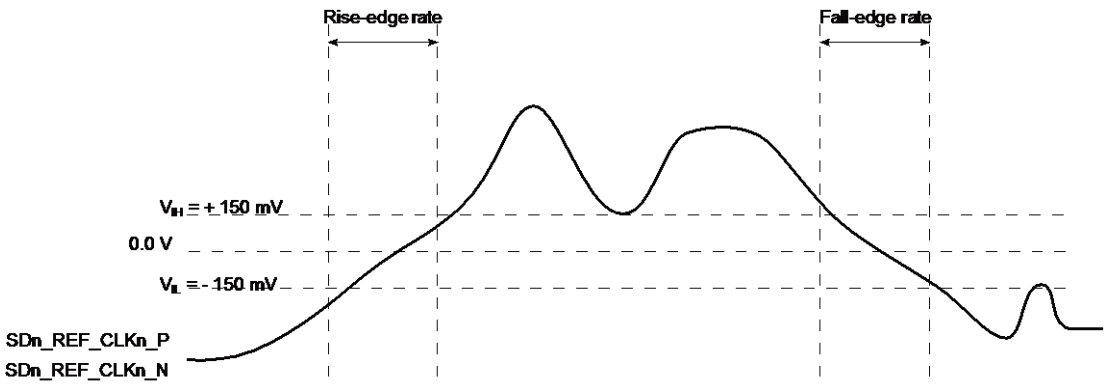
Parameter	Symbol	Min	Typ	Max	Unit	Notes
SD1_REF_CLKn_P/ SD1_REF_CLKn_N frequency range	t_{CLK_REF}	-	156.25	-	MHz	2
SD1_REF_CLKn_P/ SD1_REF_CLKn_N clock frequency tolerance	t_{CLK_TOL}	-100	-	100	ppm	-
SD1_REF_CLKn_P/ SD1_REF_CLKn_N reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	3
SD1_REF_CLKn_P/ SD1_REF_CLKn_N single side band noise	@1 kHz	-	-	-85	dBC/Hz	4
SD1_REF_CLKn_P/ SD1_REF_CLKn_N single side band noise	@10 kHz	-	-	-108	dBC/Hz	4
SD1_REF_CLKn_P/ SD1_REF_CLKn_N single side band noise	@100 kHz	-	-	-128	dBC/Hz	4
SD1_REF_CLKn_P/ SD1_REF_CLKn_N single side band noise	@1 MHz	-	-	-138	dBC/Hz	4
SD1_REF_CLKn_P/ SD1_REF_CLKn_N single side band noise	@10MHz	-	-	-138	dBC/Hz	4
SD1_REF_CLKn_P/ SD1_REF_CLKn_N random jitter (1.2 MHz to 15 MHz)	t_{CLK_RJ}	-	-	0.8	ps	-
SD1_REF_CLKn_P/ SD1_REF_CLKn_N total reference clock jitter at 10^{-12} BER (1.2 MHz to 15 MHz)	t_{CLK_TJ}	-	-	11	ps	-
SD1_REF_CLKn_P/ SD1_REF_CLKn_N spurious noise (1.2 MHz to 15 MHz)	-	-	-	-75	dBC	-

Notes:

1. For recommended operating conditions, see Table 4.
2. Caution: Only 156.25 have been tested. In-between values do not work correctly with the rest of the system.
3. Measurement taken from differential waveform.
4. Per XFP Spec. Rev 4.5, the Module Jitter Generation spec at XFI Optical Output is 10mUI (RMS) and 100 mUI (p-p). In the CDR mode the host is contributing 7 mUI (RMS) and 50 mUI (p-p) jitter.

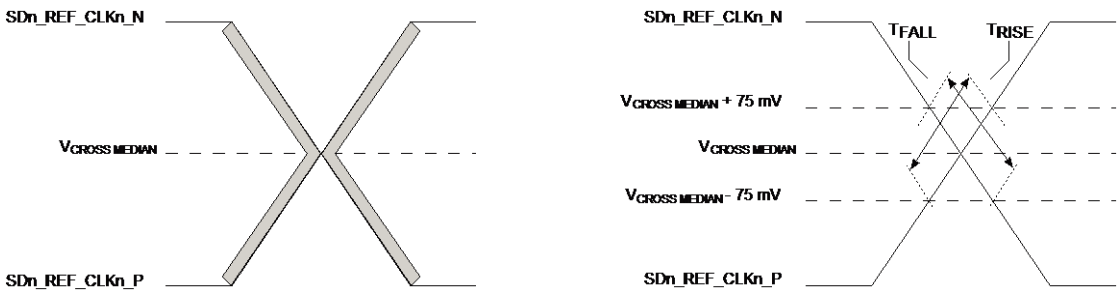
This figure shows the differential measurement points for rise and fall time.

Figure 82. Differential measurement points for rise and fall time



This figure shows the single-ended measurement points for rise and fall time matching.

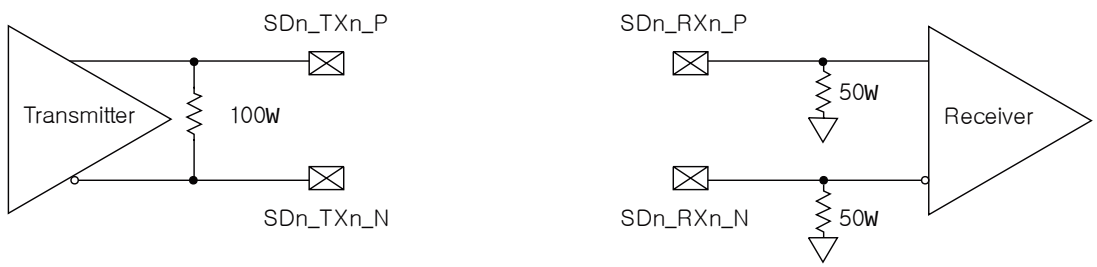
Figure 83. Single-ended measurement points for rise and fall time matching



3.24.3 SerDes transmitter and receiver reference circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.

Figure 84. SerDes transmitter and receiver reference circuits



The DC and AC specifications of the SerDes data lanes are defined in each interface protocol section below based on the application usage:

- PCI Express
- Serial ATA (SATA) interface
- SGMII interface
- XFI interface

Note that an external AC-coupling capacitor is required for the above serial transmission protocols with the capacitor value defined in the specification of each protocol section.

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3.24.4 PCI Express

This section describes the clocking dependencies, as well as the DC and AC electrical specifications for the PCI Express bus.

3.24.4.1 Clocking dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 ppm of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.The platform clock frequency must be greater than or equal to 400 MHz for PCI Express Gen2. For more details, see 5.2 Minimum platform frequency requirements for high-speed interfaces.

3.24.4.2 PCI Express DC physical layer specifications

This section contains the DC specifications for the physical layer of PCI Express on this chip.

3.24.4.2.1 PCI Express DC physical layer transmitter specifications

This section discusses the PCI Express DC physical layer transmitter specifications for 2.5 GT/s, 5 GT/s, and 8 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 116. PCI Express 2.0 (2.5 GT/s) differential transmitter output DC specifications (XV_{DD} = 1.35 V)[1]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential peak-to-peak output voltage	$V_{TX-DIFFp-p}$	800	1000	1200	mV	VTX-DIFFp-p = 2 x | VTX-D+ - VTX-D- |
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.
DC differential transmitter impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	Transmitter DC differential mode low Impedance
Transmitter DC impedance	Z_{TX-DC}	40	50	60	Ω	Required transmitter D+ as well as D- DC Impedance during all states

Note:

1. . For recommended operating conditions, see Table 4.

This table defines the PCI Express 2.0 (5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 117. PCI Express 2.0 (5 GT/s) differential transmitter output DC specifications (XV_{DD} = 1.35 V)[1]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential peak-to-peak output voltage	$V_{TX-DIFFp-p}$	800	1000	1200	mV	$V_{TX-DIFFp-p} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$
Low-power differential peak-to-peak output voltage	$V_{TX-DIFFp-p\_low}$	400	500	1200	mV	$V_{TX-DIFFp-p} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-3.5dB}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.
DC differential transmitter impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	Transmitter DC differential mode low impedance
Transmitter DC Impedance	Z_{TX-DC}	40	50	60	Ω	Required transmitter D+ as well as D- DC impedance during all states

1. For recommended operating conditions, see Table 4.

This table defines the PCI Express 3.0 (8 GT/s) DC characteristics for the differential output at all transmitters. The parameters are specified at the component pins.

Table 118. PCI Express 3.0 (8 GT/s) differential transmitter output DC characteristics (XV_{DD} = 1.35 V) (3)

Parameter	Symbol	Min	Typical	Max	Units	Notes
Full swing transmitter voltage with no TX Eq	$V_{TX-FS-NO-EQ}$	800	–	1300	mVp-p	See Note 1
Reduced swing transmitter voltage with no TX Eq	$V_{TX-RS-NO-EQ}$	400	–	1300	mV	See Note 1
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-3.5dB}$	3.0	3.5	4.0	dB	–
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	–
Minimum swing during EIEOS for full swing	$V_{TX-EIEOS-FS}$	250	–	–	mVp-p	See Note 2
Minimum swing during EIEOS for reduced swing	$V_{TX-EIEOS-RS}$	232	–	–	mVp-p	See Note 2
DC differential transmitter impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	Transmitter DC differential mode low impedance
Transmitter DC Impedance	Z_{TX-DC}	40	50	60	Ω	Required transmitter D+ as well as D- DC impedance during all states

Notes:

1. Voltage measurements for $V_{TX-FS-NO-EQ}$ and $V_{TX-RS-NO-EQ}$ are made using the 64-zeroes/64-ones pattern in the compliance pattern.
2. Voltage limits comprehend both full swing and reduced swing modes. The transmitter must reject any changes that would violate this specification. The maximum level is covered in the $V_{TX-FS-NO-EQ}$ measurement which represents the maximum peak voltage the transmitter can drive. The $V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ voltage limits are imposed to guarantee the EIEOS threshold of 175 mV_{P-P} at the receiver pin. This parameter is measured using the actual EIEOS pattern that is part of the compliance pattern and then removing the ISI contribution of the breakout channel.
3. For recommended operating conditions, see Table 4.

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3.24.4.2.2 PCI Express DC physical layer receiver specifications

This section discusses the PCI Express DC physical layer receiver specifications for 2.5 GT/s, 5 GT/s, and 8 GT/s.

This table defines the DC specifications for the PCI Express 2.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 119. PCI Express 2.0 (2.5 GT/s) differential receiver input DC specifications (4)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Differential input peak-to-peak voltage	$V_{RX-DIFFp-p}$	120	1000	1200	mV	$V_{RX-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ See Note 1
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	Receiver DC differential mode impedance. See Note 2
DC input impedance	Z_{RX-DC}	40	50	60	Ω	Required receiver D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	-	-	kΩ	Required receiver D+ as well as D- DC Impedance when the receiver terminations do not have power. See Note 3.
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	-	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ Measured at the package pins of the receiver

Notes:

1. Measured at the package pins with a test load of 50Ω to GND on each pin.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
3. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the receiver ground.
4. For recommended operating conditions, see Table 4.

This table defines the DC specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 120. PCI Express 2.0 (5 GT/s) differential receiver input DC specifications (4)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Differential input peak-to-peak voltage	$V_{RX-DIFFp-p}$	120	1000	1200	mV	$V_{RX-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ See Note 1.
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	Receiver DC differential mode impedance. See Note 2
DC input impedance	Z_{RX-DC}	40	50	60	Ω	Required receiver D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	-	-	kΩ	Required receiver D+ as well as D- DC Impedance when the receiver terminations do not have power. See Note 3.
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	-	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ Measured at the package pins of the receiver

Notes:

1. Measured at the package pins with a test load of 50 Ω to GND on each pin.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.

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3. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the receiver ground.
4. For recommended operating conditions, see Table 4.

This table defines the DC characteristics for the PCI Express 3.0 (8 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 121. PCI Express 3.0 (8 GT/s) differential receiver input DC characteristics (6)

Characteristic	Symbol	Min	Typ	Max	Units	Notes
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	Receiver DC differential mode impedance. See Note 2
DC input impedance	Z_{RX-DC}	40	50	60	Ω	Required receiver D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	–	–	kΩ	Required receiver D+ as well as D- DC Impedance when the receiver terminations do not have power. See Note 3
Generator launch voltage	$V_{RX-LAUNCH-8G}$	–	800	–	mV	Measured at TP1 per PCI Express base spec. rev 3.0
Eye height (-20dB Channel)	$V_{RX-SV-8G}$	25	–	–	mV	Measured at TP2P per PCI Express base spec. rev 3.0. See Notes 4, 5
Eye height (-12dB Channel)	$V_{RX-SV-8G}$	50	–	–	mV	Measured at TP2P per PCI Express base spec. rev 3.0. See Notes 4, 5
Eye height (-3dB Channel)	$V_{RX-SV-8G}$	200	–	–	mV	Measured at TP2P per PCI Express base spec. rev 3.0. See Notes 4, 5
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	–	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX^-D-} \rvert$ Measured at the package pins of the receiver

Notes:

1. Measured at the package pins with a test load of 50 Ω to GND on each pin.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
3. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the receiver ground.
4. $V_{RX-SV-8G}$ is tested at three different voltages to ensure the receiver device under test is capable of equalizing over a range of channel loss profiles. The "SV" in the parameter names refers to stressed voltage.
5. $V_{RX-SV-8G}$ is referenced to TP2P and is obtained after post processing data captured at TP2.
6. For recommended operating conditions, see Table 4.

3.24.4.3 PCI Express AC physical layer specifications

This section describes the AC specifications for the physical layer of PCI Express on this device.

3.24.4.3.1 PCI Express AC physical layer transmitter specifications

This section describes the PCI Express AC physical layer transmitter specifications for 2.5 GT/s, 5 GT/s, and 8 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 122. PCI Express 2.0 (2.5 GT/s) differential transmitter output AC specifications (4)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit interval	UI	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Minimum transmitter eye width	T_{TX-EYE}	0.75	-	-	UI	The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.25$ UI. Does not include spread-spectrum or RefCLK jitter. Includes device random jitter at 10^{-12}. See Notes 1 and 2.
Maximum time between the jitter median and maximum deviation from the median	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	-	-	0.125	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p} = 0$ V) in relation to a recovered transmitter UI. A recovered transmitter UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the transmitter UI. See Notes 1 and 2.
AC coupling capacitor	C_{TX}	75	-	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 3.

Notes:

1. Specified at the measurement point into a timing and voltage test load as shown in Figure 86 and measured over any 250 consecutive transmitter UIs.
2. A $T_{TX-EYE} = 0.75$ UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX} = 0.25$ UI for the transmitter collected over any 250 consecutive transmitter UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total transmitter jitter budget collected over any 250 consecutive transmitter UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
3. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.
4. For recommended operating conditions, see Table 4.

This table defines the PCI Express 2.0 (5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 123. PCI Express 2.0 (5 GT/s) differential transmitter output AC specifications[3]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	199.94	200.00	200.06	ps	Each UI is 200 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Minimum transmitter eye width	T_{TX-EYE}	0.75	-	-	UI	The maximum transmitter jitter can be derived as: $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.25$ UI. See Note 1.
Transmitter deterministic jitter > 1.5 MHz	$T_{TX-HF-DJ-DD}$	-	-	0.15	UI	-
Transmitter RMS jitter < 1.5 MHz	$T_{TX-LF-RMS}$	-	3.0	-	ps	Reference input clock RMS jitter (< 1.5 MHz) at pin < 1 ps
AC coupling capacitor	C_{TX}	75	-	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 2.

Notes:

1. Specified at the measurement point into a timing and voltage test load as shown in Figure 86 and measured over any 250 consecutive transmitter UIs.
2. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.
3. For recommended operating conditions, see Table 4.

This table defines the PCI Express 3.0 (8 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 124. PCI Express 3.0 (8 GT/s) differential transmitter output AC specifications[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	124.9625	125.00	125.0375	ps	Each UI is 125 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Transmitter uncorrelated total jitter	T_{TX-UTJ}	–	–	31.25	ps p-p	–
Transmitter uncorrelated deterministic jitter	$T_{TX-UDJ-DD}$	–	–	12	ps p-p	–
Total uncorrelated pulse width jitter (PWJ)	$T_{TX-UPW-TJ}$	–	–	24	ps p-p	See Note 1, 2
Deterministic data dependent jitter (DjDD) uncorrelated pulse width jitter (PWJ)	$T_{TX-UPW-DJDD}$	–	–	10	ps p-p	See Note 1, 2
Data dependent jitter	T_{TX-DDJ}	–	–	18	ps p-p	See Note 2
AC coupling capacitor	C_{TX}	176	–	265	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 3.

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Notes:
1. PWJ parameters shall be measured after data dependent jitter (DDJ) separation.
2. Measured with optimized preset value after de-embedding to transmitter pin.
3. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.
4. For recommended operating conditions, see Table 4.

3.24.4.3.2 PCI Express AC physical layer receiver specifications

This section discusses the PCI Express AC physical layer receiver specifications for 2.5 GT/s, 5 GT/s, and 8 GT/s.

This table defines the AC specifications for the PCI Express 2.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 125. PCI Express 2.0 (2.5 GT/s) differential receiver input AC specifications[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	399.88	400.00	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Minimum receiver eye width	T_{RX-EYE}	0.4	-	-	UI	The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See Notes 1 and 2.
Maximum time between the jitter median and maximum deviation from the median.	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	-	-	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to a recovered transmitter UI. A recovered transmitter UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the transmitter UI. See Notes 1, 2 and 3.

Notes:
1. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 86 must be used as the receiver device when taking measurements. If the clocks to the receiver and transmitter are not derived from the same reference clock, the transmitter UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
2. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The TRX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive transmitter UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the receiver and transmitter are not derived from the same reference clock, the transmitter UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
3. It is recommended that the recovered transmitter UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.
4. For recommended operating conditions, see Table 4.

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This table defines the AC specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 126. PCI Express 2.0 (5 GT/s) differential receiver input AC specifications[1]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	199.94	200.00	200.06	ps	Each UI is 200 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Max receiver inherent timing error	$T_{RX-TJ-CC}$	-	-	0.4	UI	The maximum inherent total timing error for common RefClk receiver architecture
Max receiver inherent deterministic timing error	$T_{RX-DJ-DD-CC}$	-	-	0.30	UI	The maximum inherent deterministic timing error for common RefClk receiver architecture

Note:

1. For recommended operating conditions, see Table 4.

This table defines the AC specifications for the PCI Express 3.0 (8 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 127. PCI Express 3.0 (8 GT/s) differential receiver input AC specifications[5]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	124.9625	125.00	125.0375	ps	Each UI is 125 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations. See Note 1.
Eye Width at TP2P	$T_{RX-SV-8G}$	0.3	–	0.35	UI	See Note 1
Differential mode interference	$V_{RX-SV-DIFF-8G}$	14	–	–	mV	Frequency = 2.1GHz. See Note 2.
Sinusoidal Jitter at 100 MHz	$T_{RX-SV-SJ-8G}$	–	–	0.1	UI p-p	Fixed at 100 MHz. See Note 3.
Random Jitter	$T_{RX-SV-RJ-8G}$	–	–	2.0	ps RMS	Random jitter spectrally flat before filtering. See Note 4.

Notes:

1. $T_{RX-SV-8G}$ is referenced to TP2P and obtained after post processing data captured at TP2. $T_{RX-SV-8G}$ includes the effects of applying the behavioral receiver model and receiver behavioral equalization.
2. $V_{RX-SV-DIFF-8G}$ voltage may need to be adjusted over a wide range for the different loss calibration channels.
3. The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency as shown in Figure 85.
4. Random jitter (Rj) is applied over the following range: The low frequency limit may be between 1.5 and 10 MHz, and the upper limit is 1.0 GHz. See Figure 85 for details. Rj may be adjusted to meet the 0.3 UI value for $T_{RX-SV-8G}$.
5. For recommended operating conditions, see Table 4.

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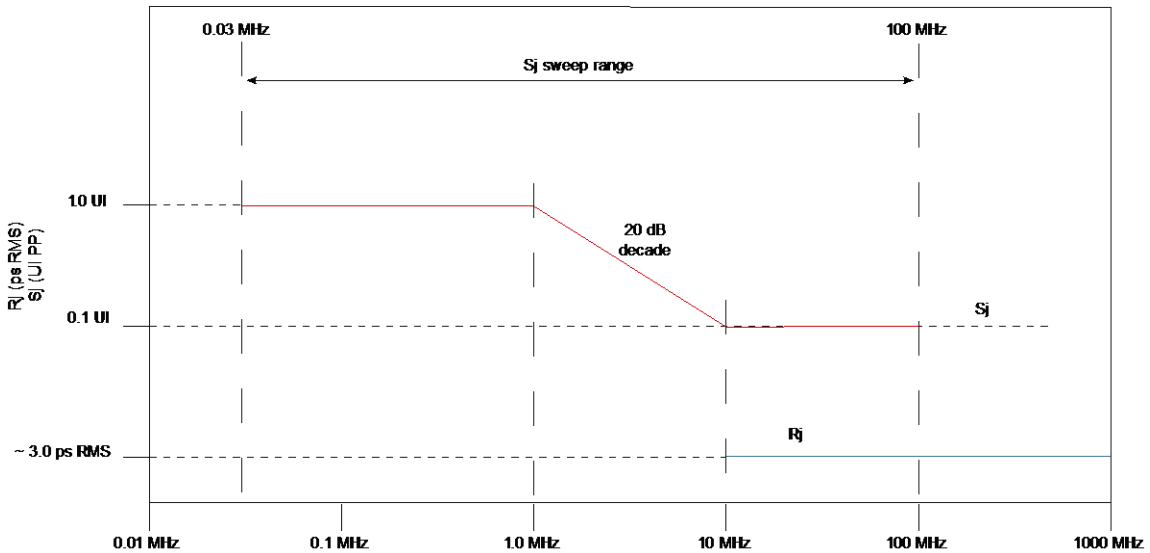
Figure 85. Swept sinusoidal jitter mask



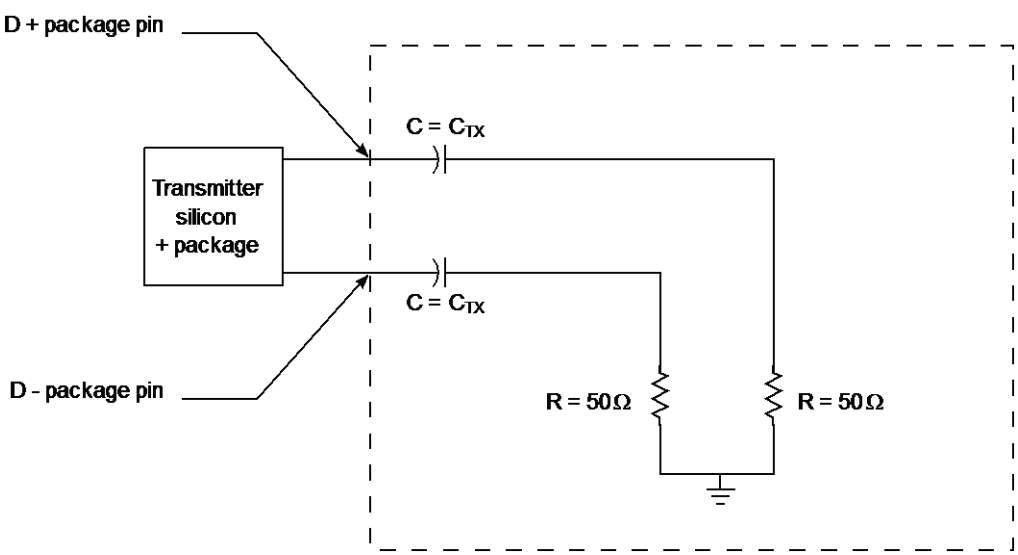
3.24.4.3.3 Test and measurement load

The AC timing and voltage parameters must be verified at the measurement point. The package pins of the device must be connected to the test/measurement load within 0.2 inches of that load, as shown in the following figure.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/ board routing may benefit from D+ and D- not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D- package pins.

Figure 86. Test and measurement load



3.24.5 Serial ATA (SATA) interface

This section describes the DC and AC electrical specifications for the SATA interface.

3.24.5.1 SATA DC electrical characteristics

This section describes the DC electrical characteristics for SATA.

3.24.5.1.1 SATA DC transmitter output characteristics

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen1i/1m or 1.5 Gbit/s transmission.

Table 128. Gen1i/1m 1.5 G transmitter DC specifications (XV_{DD} = 1.35 V)[3]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Tx differential output voltage	VSATA_TXDIFF	400	500	600	mV p-p	1
Tx differential pair impedance	ZSATA_TXDIFFIM	85	100	115	Ω	2

Notes:
1. Terminated by 50 Ω load.
2. DC impedance.
3. For recommended operating conditions, see Table 4.

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen2i/2m or 3.0 Gbit/s transmission.

Table 129. Gen 2i/2m 3 G transmitter DC specifications (XV_{DD} = 1.35 V)[2]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Transmitter differential output voltage	V_{SATA_TXDIFF}	400	–	700	mV p-p	1
Transmitter differential pair impedance	$Z_{SATA\_TXDIFFIM}$	85	100	115	Ω	–

Notes:
1. Terminated by 50 Ω load.
2. For recommended operating conditions, see Table 4.

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen 3i transmission.

Table 130. Gen 3i transmitter DC specifications (XV_{DD} = 1.35 V)[2]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Transmitter differential output voltage	VSATA_TXDIFF	240	–	900	mV p-p	1
Transmitter differential pair impedance	ZSATA_TXDIFFIM	85	100	115	Ω	–

Notes:
1. Terminated by 50 Ω load.
2. For recommended operating conditions, see Table 4.

3.24.5.1.2 SATA DC receiver input characteristics

This table provides the Gen1i/1m or 1.5 Gbit/s differential receiver input DC characteristics for the SATA interface.

Table 131. Gen1i/1m 1.5 G receiver input DC specifications (3)

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input voltage	V_{SATA_RXDIFF}	240	500	600	mV p-p	1
Differential receiver input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	2
OOB signal detection threshold	V_{SATA_OOB}	50	120	240	mV p-p	–

Notes:
1. Voltage relative to common of either signal comprising a differential pair.
2. DC impedance.
3. For recommended operating conditions, see Table 4.

This table provides the Gen2i/2m or 3 Gbit/s differential receiver input DC characteristics for the SATA interface.

Table 132. Gen2i/2m 3 G receiver input DC specifications (3)

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input voltage	V_{SATA_RXDIFF}	240	–	750	mV p-p	1
Differential receiver input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	2
OOB signal detection threshold	V_{SATA_OOB}	75	120	240	mV p-p	2

Notes:
1. Voltage relative to common of either signal comprising a differential pair.
2. DC impedance.
3. For recommended operating conditions, see Table 4.

This table provides the Gen 3i differential receiver input DC characteristics for the SATA interface.

Table 133. Gen 3i receiver input DC specifications (3)

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input voltage	V_{SATA_RXDIFF}	240	–	1000	mV p-p	1
Differential receiver input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	2
OOB signal detection threshold	–	75	120	200	mV p-p	–

Notes:
1. Voltage relative to common of either signal comprising a differential pair.
2. DC impedance.
3. For recommended operating conditions, see Table 4.

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3.24.5.2 SATA AC timing specifications

This section describes the SATA AC timing specifications.

3.24.5.2.1 AC requirements for SATA REF_CLK

This table provides the AC requirements for the SATA reference clock. These requirements must be guaranteed by the customer's application design.

Table 134. SATA reference clock input requirements (6)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SD*n*_REF_CLK1_P/SD*n*_REF_CLK1_N frequency range	t_{CLK_REF}	–	100/125	–	MHz	1
SD*n*_REF_CLK1_P/SD*n*_REF_CLK1_N clock frequency tolerance	t_{CLK_TOL}	-350	–	+350	ppm	–
SD*n*_REF_CLK1_P/SD*n*_REF_CLK1_N reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	5
SD*n*_REF_CLK1_P/SD*n*_REF_CLK1_N cycle- to-cycle clock jitter (period jitter)	t_{CLK_CJ}	–	–	100	ps	2
SD*n*_REF_CLK1_P/SD*n*_REF_CLK1_N total reference clock jitter, phase jitter (peak-to-peak)	t_{CLK_PJ}	-50	–	+50	ps	2, 3, 4

Notes:

1. Caution: Only 100 and 125 MHz have been tested. In-between values do not work correctly with the rest of the system.
2. At RefClk input.
3. In a frequency band from 150 kHz to 15 MHz at BER of 10^{-12}.
4. Total peak-to-peak deterministic jitter must be less than or equal to 50 ps.
5. Measurement taken from differential waveform.
6. For recommended operating conditions, see Table 4.

3.24.5.2.2 AC transmitter output characteristics

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen 1i/1m or 1.5 Gbit/s transmission. The AC timing specifications do not include RefClk jitter.

Table 135. Gen 1i/1m 1.5 G transmitter AC specifications (2)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Channel speed	t_{CH_SPEED}	–	1.5	–	Gbit/s	–
Unit interval	T_{UI}	666.4333	666.6667	670.2333	ps	–
Total jitter data-data 5 UI	$U_{SATA\_TXTJ5UI}$	–	–	0.355	UI p-p	1
Total jitter, data-data 250 UI	$U_{SATA\_TXTJ250UI}$	–	–	0.47	UI p-p	1
Deterministic jitter, data-data 5 UI	$U_{SATA\_TXDJ5UI}$	–	–	0.175	UI p-p	1
Deterministic jitter, data-data 250 UI	$U_{SATA\_TXDJ250UI}$	–	–	0.22	UI p-p	1

Notes:

1. Measured at transmitter output pins peak-to-peak phase variation; random data pattern.
2. For recommended operating conditions, see Table 4.

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This table provides the differential transmitter output AC characteristics for the SATA interface at Gen 2i/2m or 3.0 Gbit/s transmission. The AC timing specifications do not include RefClk jitter.

Table 136. Gen 2i/2m 3 G transmitter AC specifications (2)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Channel speed	t_{CH_SPEED}	–	3.0	–	Gbit/s	–
Unit Interval	T_{UI}	333.2167	333.3333	335.1167	ps	–
Total jitter $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_TXTJfB/500}$	–	–	0.37	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_TXTJfB/1667}$	–	–	0.55	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div$	$U_{SATA\_TXDJfB/500}$	–	–	0.19	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div$	$U_{SATA\_TXDJfB/1667}$	–	–	0.35	UI p-p	1

Notes:
1. Measured at transmitter output pins peak-to-peak phase variation; random data pattern.
2. For recommended operating conditions, see Table 4.

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen 3i transmission. The AC timing specifications do not include RefClk jitter.

Table 137. Gen 3i transmitter AC specifications (1)

Parameter	Symbol	Min	Typ	Max	Units
Speed	–	–	6.0	–	Gbit/s
Total jitter before and after compliance interconnect channel	J_T	–	–	0.52	UI p-p
Random jitter before compliance interconnect channel	J_R	–	–	0.18	UI p-p
Unit interval	UI	166.6083	166.6667	167.5583	ps

Note:
1. For recommended operating conditions, see Table 4.

3.24.5.2.3 AC differential receiver input characteristics

This table provides the Gen1i/1m or 1.5 Gbit/s differential receiver input AC characteristics for the SATA interface. The AC timing specifications do not include RefClk jitter.

Table 138. Gen 1i/1m 1.5 G receiver AC specifications (2)

Parameter	Symbol	Min	Typical	Max	Units	Notes
Unit Interval	T_{UI}	666.4333	666.6667	670.2333	ps	–
Total jitter data-data 5 UI	$U_{SATA\_RXTJ5UI}$	–	–	0.43	UI p-p	1
Total jitter, data-data 250 UI	$U_{SATA\_RXTJ250UI}$	–	–	0.60	UI p-p	1
Deterministic jitter, data-data 5 UI	$U_{SATA\_RXDJ5UI}$	–	–	0.25	UI p-p	1
Deterministic jitter, data-data 250 UI	$U_{SATA\_RXDJ250UI}$	–	–	0.35	UI p-p	1

Notes:
1. Measured at the receiver.
2. For recommended operating conditions, see Table 4.

This table provides the differential receiver input AC characteristics for the SATA interface at Gen2i/2m or 3.0 Gbit/s transmission. The AC timing specifications do not include RefClk jitter.

Table 139. Gen 2i/2m 3 G receiver AC specifications (2)

Parameter	Symbol	Min	Typical	Max	Units	Notes
Unit Interval	T_{UI}	333.2167	333.3333	335.1167	ps	–
Total jitter $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_RXTJfB/500}$	–	–	0.60	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_RXTJfB/1667}$	–	–	0.65	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_RXDJfB/500}$	–	–	0.42	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div$	$U_{SATA\_RXDJfB/1667}$	–	–	0.35	UI p-p	1

Notes:

1. Measured at the receiver.
2. For recommended operating conditions, see Table 4.

This table provides the differential receiver input AC characteristics for the SATA interface at Gen 3i transmission. The AC timing specifications do not include RefClk jitter.

Table 140. Gen 3i receiver AC specifications (2)

Parameter	Symbol	Min	Typical	Max	Units	Notes
Total jitter after compliance interconnect channel	J_T	–	–	0.60	UI p-p	1
Random jitter before compliance interconnect channel	J_R	–	–	0.18	UI p-p	1
Unit interval: 6.0 Gb/s	UI	166.6083	166.6667	167.5583	ps	–

Notes:

1. Measured at the receiver.
2. The AC specifications do not include RefClk jitter.

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4 SECURITY FUSE PROCESSOR

This chip implements the QorIQ platform's trust architecture, supporting capabilities such as secure boot. Use of the trust architecture feature is dependent on programming fuses in the Security Fuse Processor (SFP). The details of the trust architecture and SFP can be found in the chip reference manual.

To program SFP fuses, the user is required to supply 1.8 V to the TA_PROG_SFP pin per Power sequencing. TA_PROG_SFP should only be powered for the duration of the fuse programming cycle, with a per device limit of six fuse programming cycles. All other times, TA_PROG_SFP should be connected to GND. The sequencing requirements for raising and lowering TA_PROG_SFP are shown in Figure 9. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Table 4.

NOTE

Users not implementing the QorIQ platform's trust architecture features should connect TA_PROG_SFP to GND.

5 HARDWARE DESIGN CONSIDERATIONS

5.1 Clock ranges

This table provides the clocking specifications for the processor core, platform, memory, and integrated flash controller.

Table 141. Processor, platform, and memory clocking specifications

Characteristic	Maximum processor core frequency								Unit	Notes
	1200 MHz		1400 MHz		1600 MHz		1800 MHz			
	Min	Max	Min	Max	Min	Max	Min	Max		
Core cluster group PLL frequency	1000	1200	1000	1400	1000	1600	1000	1800	MHz	1, 2
Platform clock frequency	400	400	400	600	400	700	400	700	MHz	1, 3
Memory Bus Clock Frequency (DDR4)	650	800	650	1050	650	1050	650	1050	MHz	1, 4, 5
IFC clock frequency	-	100	-	100	-	100	-	100	MHz	
FMan	400	600	400	600	400	800	400	800	MHz	

1. Caution: The platform clock to SYSCLK ratio and core to SYSCLK ratio settings must be chosen such that the resulting SYSCLK frequency, core frequency, and platform clock frequency do not exceed their respective maximum or minimum operating frequencies.
2. The memory bus clock speed is half the DDR4 data rate. The DDR4 memory bus clock frequency is limited to min = 650 MHz.
3. The memory bus clock speed is dictated by its own PLL.
4. The integrated flash controller (IFC) clock speed on IFC_CLK[0:1] is determined by the IFC module input clock (platform clock / 2) divided by the IFC ratio programmed in CCR[CLKDIV]. See the chip reference manual for more information.
5. The minimum platform frequency should meet the requirements in Minimum platform frequency requirements for high-speed interfaces.
6. For supported voltage/frequency options, see the orderable part list of QorIQ QLS1046A and QLS1026A Multicore Communications Processors at www.Teledyne e2v.com.

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5.1.1 DDR clock ranges

The DDR memory controller can run only in asynchronous mode, where the memory bus is clocked with the clock provided on the DDRCLK input pin, which has its own dedicated PLL.

This table provides the clocking specifications for the memory bus.

Table 142. Memory bus clocking specifications

Characteristic	Min Freq.(MHz)	Max Freq.(MHz)	Min Data Rate (MT/s)	Max Data Rate (MT/s)	Notes
Memory bus clock frequency and data rate for DDR4	650	1050	1300	2100	1, 2, 3

Notes:

1. Caution: The platform clock to SYSCLK ratio, core to SYSCLK ratio and DDR to SYSCLK (or DDRCLK) ratio settings must be chosen such that the resulting platform frequency, core frequency and DDRCLK frequency do not exceed their respective maximum or minimum operating frequencies.
2. The memory bus clock refers to the chip's memory controllers' Dn_MCK[0:1] and Dn_MCK[0:1] output clocks, running at half of the DDR data rate.
3. The memory bus clock speed is dictated by its own PLL.
4. For supported voltage/frequency options, see the orderable part list of QorIQ QLS1046A and QLS1026A Multicore Communications Processors at www.Teledyne e2v.com.

5.2 Minimum platform frequency requirements for high-speed interfaces

The platform clock frequency must be considered for proper operation of high-speed interfaces as described below. For proper PCI Express operation, the platform clock frequency must be greater than or equal to:

Figure 87. Gen 1 PEX minimum platform frequency

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{16}$$

Figure 88. Gen 2 PEX minimum platform frequency

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{8}$$

Figure 89. Gen 3 PEX minimum platform frequency

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{4}$$

See section "Link Width," in the chip reference manual for PCI Express interface width details. Note that "PCI Express link width" in the above equation refers to the negotiated link width as the result of PCI Express link training, which may or may not be the same as the link width POR selection. It refers to the widest port in use, not the combined width of the number ports in use.

5.3 Minimum DPAA frequency requirements

The minimum DPAA frequency of 533 MHz is required for 10 G operations.

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6 THERMAL

This table shows the thermal characteristics for the chip. Note that these numbers are based on design estimates and are preliminary.

Table 143. Package thermal characteristics (for LS1046 stand-alone)

Rating	Board	Symbol	Value	Unit	Notes
Junction-to-ambient, natural convection	Single-layer board (1s)	$R_{\Theta JA}$	25.18	°C/W	1
Junction-to-ambient, natural convection	Four-layer board (2s2p)	$R_{\Theta JA}$	14.35	°C/W	1
Junction-to-ambient, moving air (1 m/s)	Single-layer board (1s)	$R_{\Theta JMA}$	15.47	°C/W	1
Junction-to-ambient, moving air (1 m/s)	Four-layer board (2s2p)	$R_{\Theta JMA}$	9.35	°C/W	1
Junction-to-board	-	$R_{\Theta JB}$	4.66	°C/W	2
Junction-to-case (top)	-	$R_{\Theta JC}$	0.71	°C/W	3
Junction-to-lid top	-	$R_{\Theta JLT}$	0.36	°C/W	4

Notes:

1. Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-2A and JESD51-6 (moving air). Thermal test board meets JEDEC specification for this package (JESD51-9).
2. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
3. Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
4. Junction-to-lid-top thermal resistance is determined using the MIL-STD 883 Method 1012.1. However, instead of the cold plate, the lid top temperature is used here for the reference case temperature. Reported value does not include the thermal resistance layer between the package and cold plate.
5. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a specific standardized environment. It is not meant to predict the performance of a package in an application-specific environment.

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Table 144. Thermal resistance with heat sink in open flow (for LS1046 stand-alone)

Heat sink with thermal grease	Air flow	Thermal resistance (°C/W)
Wakefield 53 x 53 x 25 mm Pin Fin	Natural Convection	6.5
Wk698	0.5 m/s	4.0
	1 m/s	2.9
	2 m/s	2.4
	4 m/s	2.1
Aavid 35x31x23 mm Pin Fin	Natural Convection	8.8
av10563	0.5 m/s	5.3
	1 m/s	4.2
	2 m/s	3.9
	4 m/s	3.3
Aavid 30x30x9.4 mm Pin Fin	Natural Convection	12.5
Av 3358	0.5 m/s	8.9
	1 m/s	6.7
	2 m/s	5.1
	4 m/s	4.1
Aavid 43x41x16.5 mm Pin Fin	Natural Convection	9.0
Av 2332	0.5 m/s	5.8
	1 m/s	4.3
	2 m/s	3.2
	4 m/s	2.7

Notes:

1. Simulations with heat sinks were done with the package mounted on the 2s2p thermal test board.
2. The thermal interface material was a typical thermal grease such as Dow Corning 340 or Wakefield 120 grease.
3. See Thermal management information, for additional details.

6.1 Recommended thermal model

Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local Teledyne e2v sales office.

6.2 Temperature diode

The chip has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461A). These devices feature series resistance cancellation using three current measurements, where up to 1.5 kΩ of resistance can be automatically cancelled from the temperature result, allowing noise filtering and a more accurate reading.

The following are the specifications of the chip's on-board temperature diode:

- Operating range: Operating range: 10 - 230µA
- Ideality factor over 13.5 - 220 µA
- Temperature range: 80°C - 105°C: n = 1.004 ± 0.008

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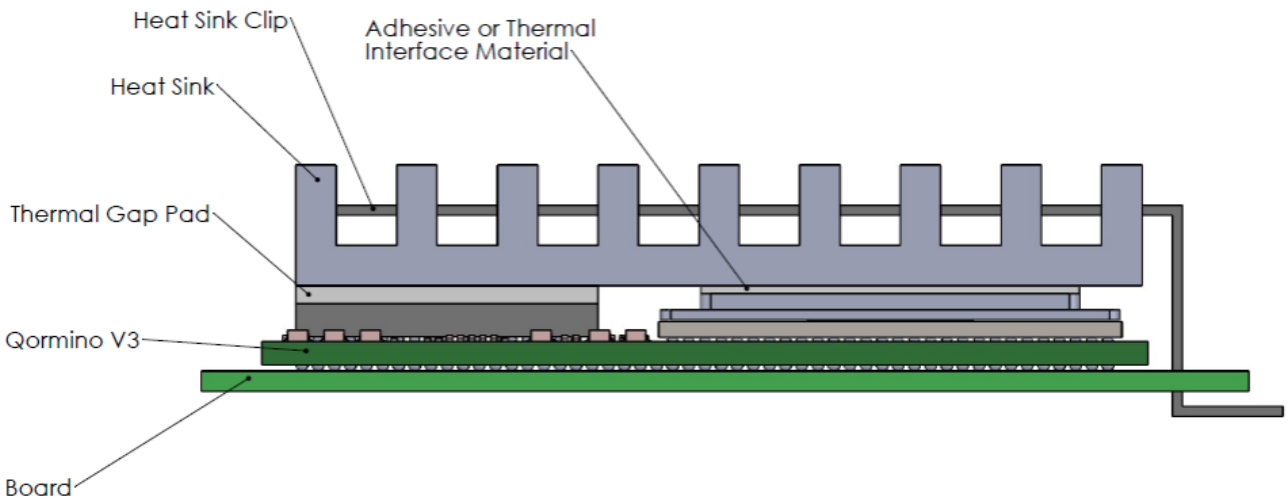
6.3 Thermal management information

This section provides thermal management information for the flip-chip, plastic-ball, grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design-the heat sink, airflow, and thermal interface material.

The recommended attachment method to the heat sink is illustrated in Figure 90. The heat sink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 15 pounds force (65 N).

Figure 90. Package exploded, cross-sectional view-FC-PBGA



The system board designer can choose between several types of heat sinks to place on the device. There are several commercially available thermal interfaces to choose from in the industry. Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

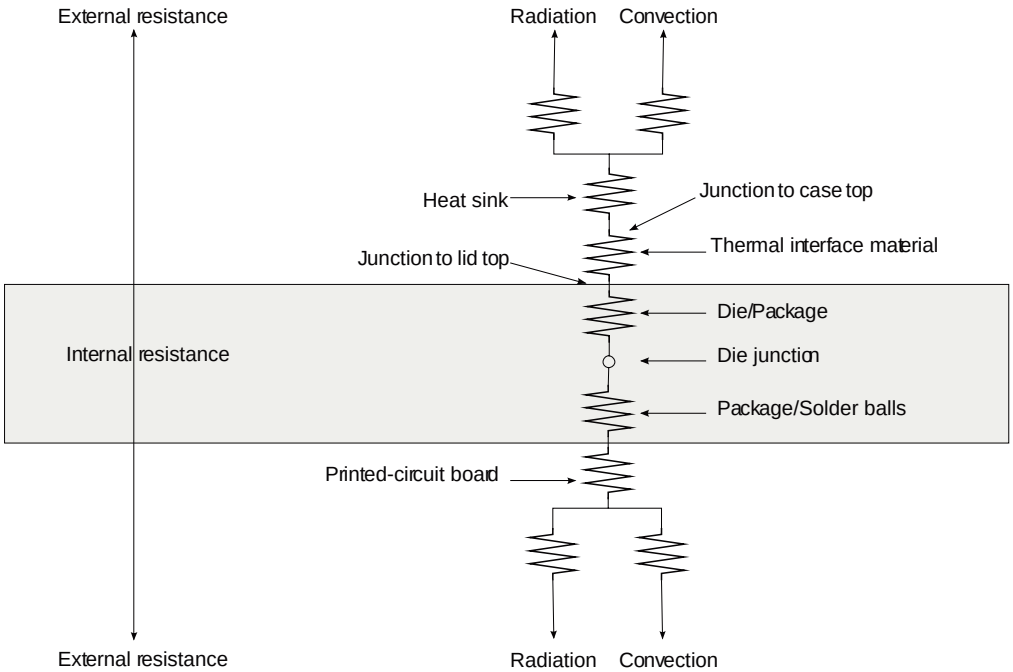
6.3.1 Internal package conduction resistance (for LS1046 stand-alone)

For the package, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-lid-top thermal resistance
- The die junction-to-board thermal resistance

This figure shows the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

Figure 91. Package with heat sink mounted to a printed-circuit board



(Note the internal versus external package resistance)

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

6.3.2 Thermal interface materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. The performance of thermal interface materials improves with increasing contact pressure; this performance characteristic chart is generally provided by the thermal interface vendor. The recommended method of mounting heat sinks on the package is by means of a spring clip attachment to the printed-circuit board (see Figure 90).

The system board designer can choose among several types of commercially available thermal interface materials.

7 PACKAGE INFORMATION

7.1 Package parameters for the FC-PBGA

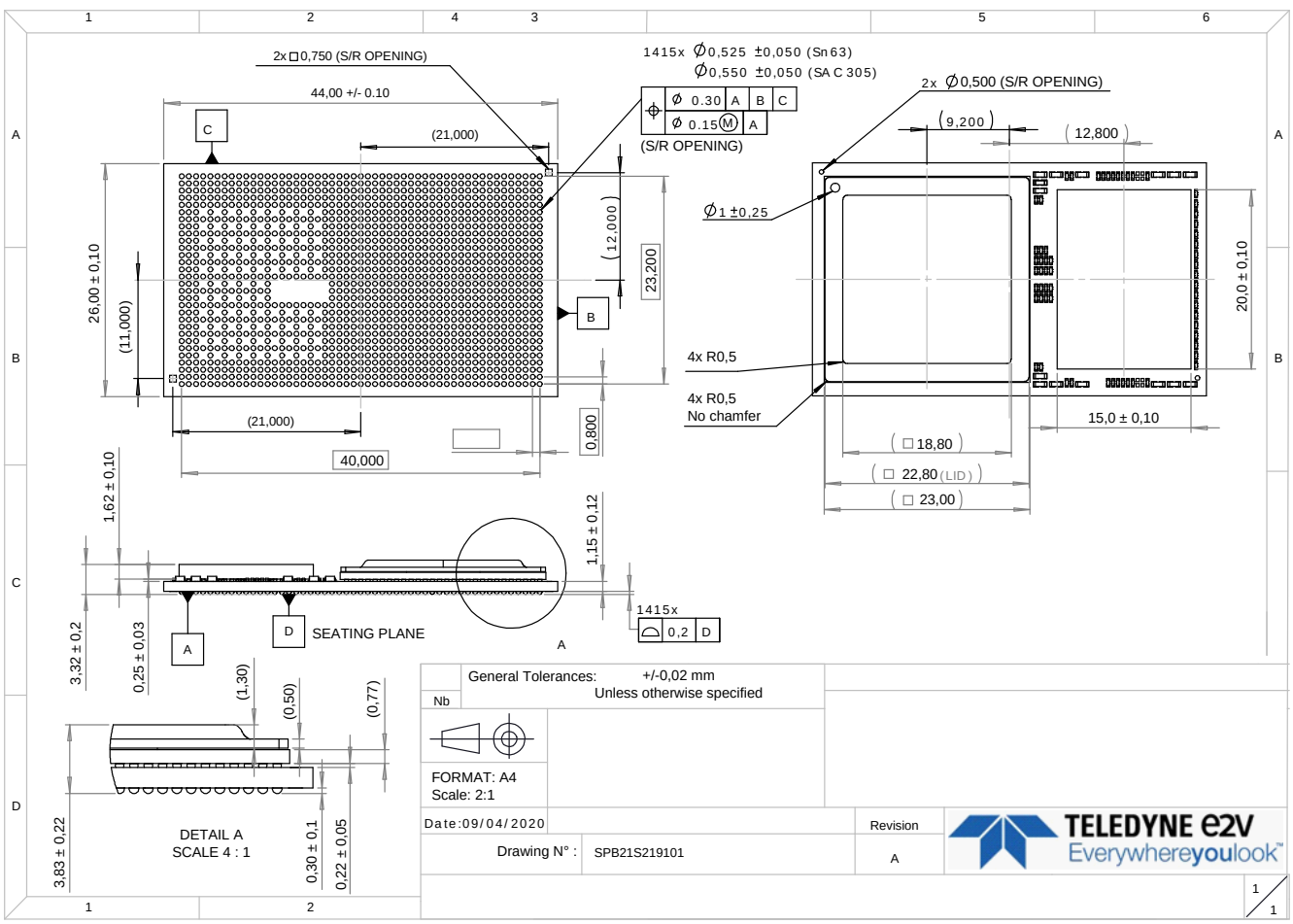
The package parameters are as provided in the following list. The package type is 26 mm x 44 mm, 1415 flip-chip, plastic-ball, grid array.

- Package outline - 26 mm x 44 mm
- Interconnects - 1415
- Ball Pitch - 0.8 mm
- Ball Diameter (nominal) - 0.45 mm
- Ball Height (nominal) - 0.3 mm
- Solder Balls Composition - 96.5% Sn, 3% Ag, and 0.5% Cu
- Solder Balls Composition - 63% Sn, 37% Pb
- Module height 3.83 mm typ (3.61 mm to 4.05 mm)

7.2 Mechanical dimensions of the FC-PBGA

This figure shows the mechanical dimensions and bottom surface nomenclature of the chip.

Figure 92. Mechanical dimensions of the FC-PBGA



1. All dimensions are in millimeters.

2. Dimensions and tolerances per ASME Y14.5M-1994.

8 ORDERING INFORMATION

This table provides the Teledyne e2v QorIQ platform part numbering nomenclature.

8.1 Part numbering nomenclature

This table provides the NXP QorIQ platform part numbering nomenclature.

Table 145. Part numbering nomenclature

Generation	Performance Level	Number of Virtual cores	Unique ID	Temperature Range	Encryption	Package Type	CPU Speed (3)	DDR Data Rate	DDR Size	Memory Type	Product Revision
QLS(X) (2) = Layer scape	1	04 = four cores 02 = two cores	6	A = Automotive -40°C – 105°C F = -40°C – 125°C M = Military -55°C – 125°C	E = Encryption N = Non-Encryption	1(3) = FCPBGA with L1, L2/SnPb CMS/Pbfree 3 = FCPBGA L2/SnPb L1, CMS/Pbfree 8 = FCPBGA L1, L2, CMS/Pbfree	P = 1400 MHz Q = 1600 MHz T = 1800 MHz	1 = 2100 MHz	4 = 4GB 8 = 8GB	4 = DDR4	A = Rev 1.0 B = Rev 2.0

Notes:

1. For availability of the different versions, contact your local Teledyne e2v sales office.
2. The letter X in the part number designates a "Prototype" product that has not been qualified by Teledyne e2v. Reliability of a PCX part number is not guaranteed, and such part-number shall not be used in Flight Hardware. Product changes may still occur while shipping prototypes.
3. For the QLS1046A and QLS1026A family of devices, parts marked with "M" CPU speed require 0.9 V operating voltage. ‘1’ means everything is SnPb, except for the passives which are RoHs finish but assembled with SnPb solder paste.

9 REVISION HISTORY

This table summarizes revisions to this document.

Issue	Date	Comments
DS 60S 217489(G)	12/23	Update power consumption with DDR4_8GB data Update ordering information with DDR4_8GB
DS 60S 217489(E-F)	03/23	Delete TBD Add DDR4 power consumption Add ref AN 60S 223060 (available on the product webpage)
DS 60S 217489(D)	01/22	Chap 6 descriptions for LS1046 stand-alone Removal of Preliminary Deleting M version and features at 0.9V, Table 4, Table 8, Table 9 and Table 145. For the QLS1046A family of devices, only parts marked with “P”, “Q” and “T” support extended temperature range, parts marked “M” CPU speed supports 0°C – 105°C range only. In Table 4 - Updated recommended value of USB_SVIN from "0.3 to USB_SVDD" to "GND to USB_SVDD" Removed input signals from Table 5 as they are irrelevant for output drive capability Removed typo "PORESET_B assertion" from step2 of secure boot fuse programming in Power sequencing

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		In Table 8 and Table 9 - Added note 9 regarding power numbers applicability - Added power numbers for 1200MHz at 1.0V - Added note 10 regarding power numbers applicability for 1200MHz at 1.0V Chap 3.5 consumption values for 2100MHz Chap 3.10.1 power sequence 64ms=>3s In Table 11 Values for x64 at 2100 MHz only
DS 60S 217489(C)	08/21	Table 146. Part numbering nomenclature: Removed column “core type” Removed jitter spec for ECn_GTX_CLK125 in Table 19
DS 60S 217489(B)	05/20	Table 9.1: Added line “Iddinit: DDR4 initialization current” Updated Figure 93. Mechanical dimensions of the FC-PBGA
DS 60S 217489(A)	01/19	Initial revision

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